Gate Driver - Soft turn-off

Romeo Fan, FAE
2019/04/09
IGBT is shut off slowly

- The soft turn-off was reducing the turn-off overvoltage even more than expected
  - Due to the presence of the parasitic inductance in the loop, turning the power switch off too quickly under a high fault current condition can generate a high voltage spike at the power switch collector.
  - The IC activates additionally a soft turn-off sequence, if a turn-off is initiated due to a desaturation condition on terminal DESAT.

- Common Description
  - soft shutdown
  - soft turn-off
  - "softly” turn-off
Comparison

- **Infineon**
  - Two-level turn-off
    - Zener diode controls the level, & TLSET pin set timing

- **TI**
  - Three discharged timings
    - Zener diode controls the level, & resistor set timing

- **Silicon Labs**
  - Two discharged timings
    - Internal resistor set timing & External Resistor can increase discharged time

- **Avago**
  - Two discharged timings
    - Internal MOSFET’s $R_{ds(on)}$ resistor set timing
  - One discharged timing
    - External Soft Shutdown Resistor set timing

- **PI**
  - Two discharged timings
    - Time constant
  - One discharged timing
    - Time constant
Infineon (EiceDRIVER™)

- The IGBT can be turned off smoothly via an external higher-ohmic gate resistor attached to terminal SOFF. The soft turn-off speed can be adjusted by selecting the appropriate resistor value. The soft turn-off reduces the voltage overshoot considerably and may be used in combination with the two-level turn-off function of the IC.
The Two-Level Turn-Off introduces an additional turn off voltage level $V_{ZDIODE}$ (as shown in Figure 10) at the driver output in between ON- and OFF-level. This additional level ensures lower VCE overshoots at turn off by reducing gate emitter voltage of the IGBT in short circuits. The lowered VGE level is limiting the current of the IGBT during the additional level interval $T_{TLSET}$, the required timing value is depending on stray inductance and di/dt at beginning of two level turn off interval.

![Two-Level Turn-Off switching behaviour](image-url)

**Figure 10 Two-Level Turn-Off switching behaviour**
Two-Level Turn-Off (1ED020I12BT only)

- The additional turn off voltage level $V_{ZDOIODE}$ and hold up time $T_{TLSET}$ could be adjusted at $T_{LSET}$ pin. The $V_{ZDOIODE}$ is set by the external Zener diode $D_{TLSET}$ connected between pin $T_{LSET}$ and GND2. The interval $T_{TLSET}$ is set by the external capacitor $C_{TLSET\_ext}$ connected to the same pin $T_{LSET}$ and GND2.
The VCE of the IGBT is monitored during ON time to detect overcurrent conditions, which will make the IGBT get into a linear mode of operation. On detecting VCE higher than a DESAT threshold, the IGBT is shut off slowly (soft turnoff) to limit the VCE overshoot.

A soft turn-off is done by increasing the gate voltage discharge time during turn-off to reduce the di/dt after a DESAT fault condition.

Two functions
- One is to discharge the gate capacitance until it reaches 2 V and then to strongly apply –8 V to the gate to keep the IGBT turned off.
After the DESAT-DETECT signal goes high, Q9 turns on and causes Q2 to turn on, which engages the Zener and resistor to discharge the gate. Once the gate voltage reduces to 2 V, the clamp circuit (Q8 and Q7) is activated. Q8 is used as a comparator by comparing the gate voltage with the base emitter saturation voltage ($V_{BE_{sat}}$) of 0.85 V.

Design Processes

Flexible High Current IGBT Gate Driver With Reinforced Digital Isolator
To avoid the high turn-off voltage spike, only the soft shutdown NMOS is turned on under DSAT shutdown (while the VL NMOS is kept in the off state). The gate capacitance of the power switch is discharged through the $R_H$ and the internal $R_{ss}$ at a much lower rate to allow the power switch to dissipate residual energy. ([AN1009](#))

The internal $R_{ss}$ (30 Ω) and a $R_H = 20$ Ω provide a typical soft shutdown duration of 2 μs (for 250 nC of total gate charge, $Q_g$.) If a longer soft shutdown period is required, steering diode (ES1B or similar) can be added to the VH pin to allow installation of a larger external soft shutdown resistor (see figure below).
If the voltage on the DSAT pin exceeds 7 V during on-time, the Si828x shuts down the output (turn off VH PMOS after $t_{FLT}$ delay) and initiates soft shutdown (after $t_{DSAT \rightarrow SS}$ delay) to protect the power switch.
A “soft” shutdown sequence, reducing the IGBT current to zero in a controlled manner to avoid potential IGBT damage from inductive overvoltages.

When a DESAT fault is detected, $V_{OUT}(V_{GE})$ is slowly brought low in order to “softly” turn-off the IGBT and prevent large $di/dt$ induced voltages.
When a desaturation fault is detected, a weak pull-down device in the ACPL-332J output drive stage will turn on to ‘softly’ turn off the IGBT. This device slowly discharges the IGBT gate to prevent fast changes in drain current that could cause damaging voltage spikes due to lead and wire inductance. During the slow turn off, the large output pull-down device remains off until the output voltage falls below VEE + 2 Volts, at which time the large pull down device clamps the IGBT gate to VEE.
When a DESAT fault is detected, VGMOS switches from low to high, turning on an external MN2 pull down switcher. MN2 slowly discharges the IGBT gate at a decay rate corresponding to the RC constant of $R_S$ and $C_{IN}$ (IGBT input capacitance).
PI (SSD Soft Shut Down)

- T1 $\Rightarrow$ IGBT desaturates
- T1-T2 $\Rightarrow$ short circuit detection
- T2 $\Rightarrow$ gate-emitter voltage decreases from 15V to approx 10V in defined time of 2μs
- T3 $\Rightarrow$ gate emitter voltage is stabiles on approx 10V, Scale™-2 measures gate current
- T4 $\Rightarrow$ at end of T3 the gate current was nearly zero, gate – emitter voltage decreases with defined speed to approx. 5V
- T5 $\Rightarrow$ Scale™-2 applies negative voltage
**ASSD – Advance Soft Shut Down**

- **Key parameters:**
  - $t_{\text{FSSD1}}$ – first decrease in VGE
  - $t_{\text{FSSD2}}$ – first decrease in VGE

Those two timings combined with voltage levels are responsible for temporary $V_{\text{CE}}$ overvoltage.

Voltage sense / Measurement (GH)

Gate current sink (GL)

ASSD功能用GH腳檢測Gate電位, 用GL腳對門極進行放電; 全過程的時間被Scale iDriver控制住

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Gate Driver - Timing

Romeo Fan, FAE
2019/04/09
Driver Timing
## Driver Timing

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