Design Example Report

Title	*15 W Constant Voltage / Constant Current (CV / CC), Isolated Flyback Converter Using InnoSwitch™-CE INN2124K*
Specification	85 VAC – 265 VAC Input; 5.3 V, 3 A Output
Application	Adapter
Author	Applications Engineering Department
Document Number	DER-471
Date	August 15, 2016
Revision	1.3

Summary and Features

- InnoSwitch-CE - Industry first AC/DC ICs with isolated, safety rated integrated feedback
- All the benefits of secondary side control with the simplicity of primary side regulation
  - ±3% CV, ±5% CC regulation
  - Insensitive to transformer variation
  - Transient response independent of load timing
  - Smaller, lower cost output capacitors
  - <25 mW no-load input power at 230 VAC
  - Built in line undervoltage and overvoltage protection
  - Cable voltage drop compensation
- Built in synchronous rectification for high efficiency

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5245 Hellyer Avenue, San Jose, CA 95138 USA.
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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This document is an engineering report describing a 5.3 V 3 A power supply utilizing INN2124K from the InnoSwitch-CE family of ICs.

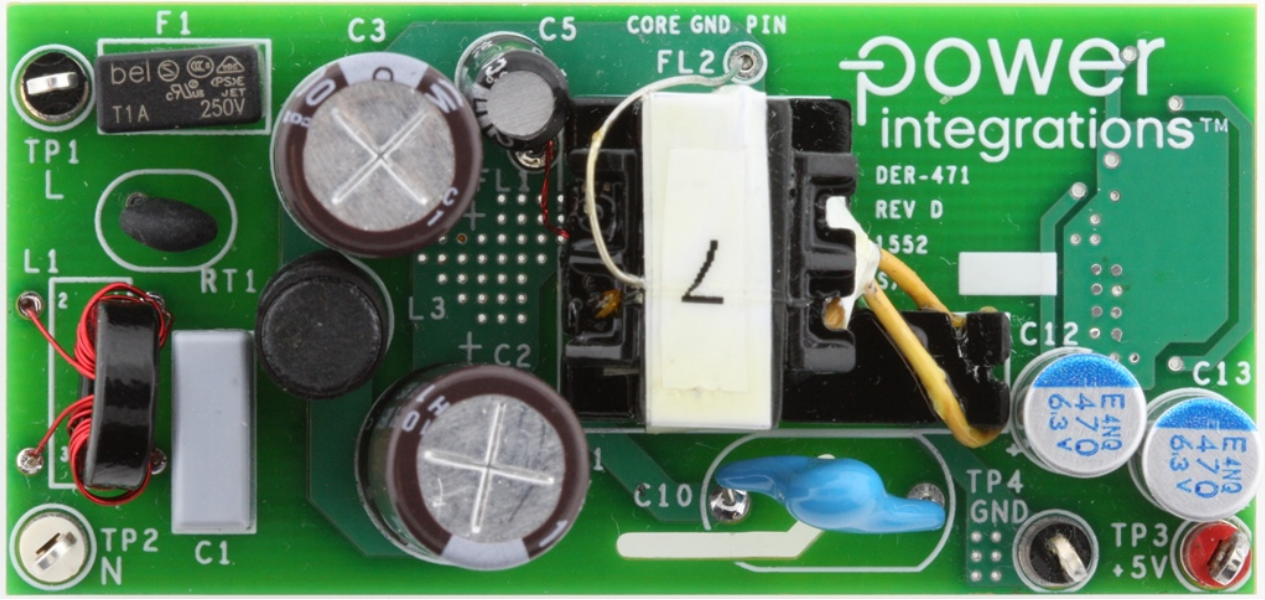

Figure 1 – Populated Circuit Board Photograph, Top.

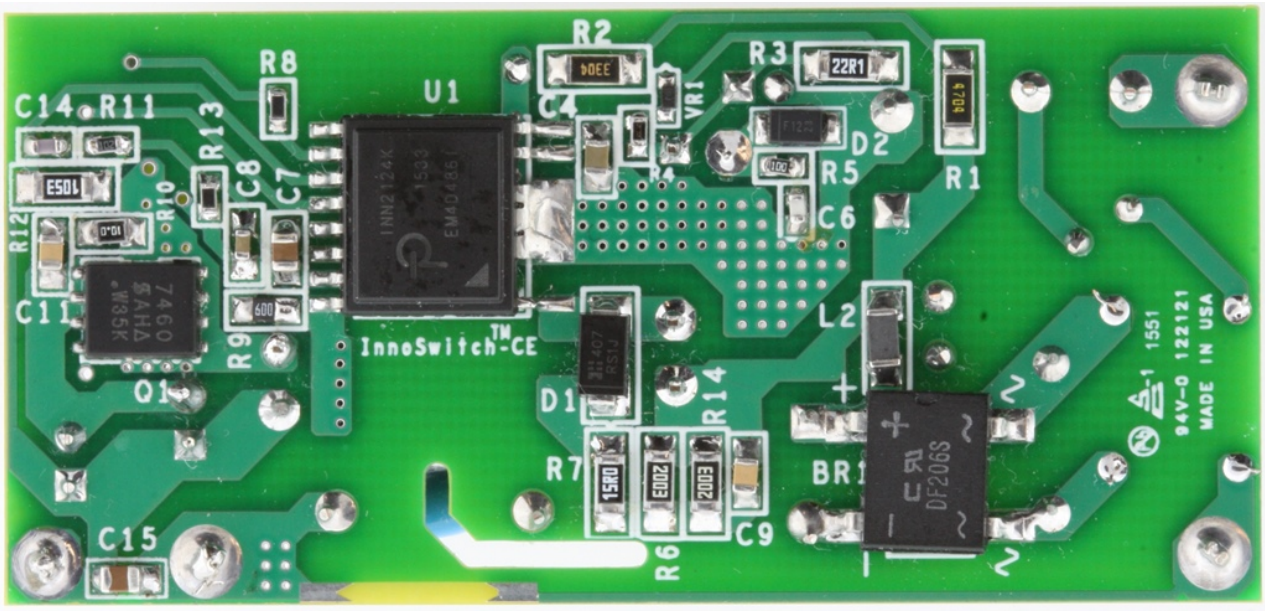

Figure 2 – Populated Circuit Board Photograph, Bottom.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	85		265	VAC	2 Wire Input.
Frequency	f_{LINE}	47	50/60	63	Hz	
Output						
Output Voltage [Full Load] (Measured at board terminals)	V_{OUT}	5.14	5.3	5.45	V	5.3 V at the Main Output Terminal Considering 0.30 V Cable Resistance Drop (End of Cable).
Transient Output Voltage	$V_{OUT(T)}$	4.2		5.5	V	0 A - 3 A - 0 A Load Step Measured at End of Cable.
Output Ripple Voltage	V_{RIPPLE}			150	mV	Output Ripple Voltage Measured at the End of the Output Cable.
Output Cable Compensation	V_{CBL}	250	300	350	mV	At 3 A Output Current.
Output Current CC point	I_{OUT}	3			A	
Auto-Restart Voltage	V_{AR}		3.45		V	At the End of the Cable.
Turn on Rise Time	t_R			10	ms	
Total Output Power						
Rated Output Power	P_{OUT}	15			W	
Efficiency						
Average 25%, 50%, 75%, and 100%	η_{AVE}	82.5			%	Measured at the End of the Cable with 230 VAC, 50 Hz Input.
10%	$\eta_{10\%}$	79			%	Measured at the End of the Cable.
No-Load Input Power				30	mW	V_{IN} at 230 VAC, 50 Hz Input.
Environmental						
Conducted EMI		CISPR22B / EN55022B Load Floating or Grounded via Artificial Hand.				With 6 dB Margin Using Resistive Load and Artificial Hand Connected.
Line Surge Common Mode (L1/L2-PE)				6	kV	100 kHz Ring Wave, 12 Ω Common Mode
ESD		±16.5			kV	Air Discharge Voltage and with No Degradation in Performance After Test.
		±8.8			kV	Contact Discharge Voltage with Degradation in Performance After Test.
Ambient Temperature	T_{AMB}	0		40	°C	Free Convection, Sea Level in Sealed Enclosure.

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3 Schematic

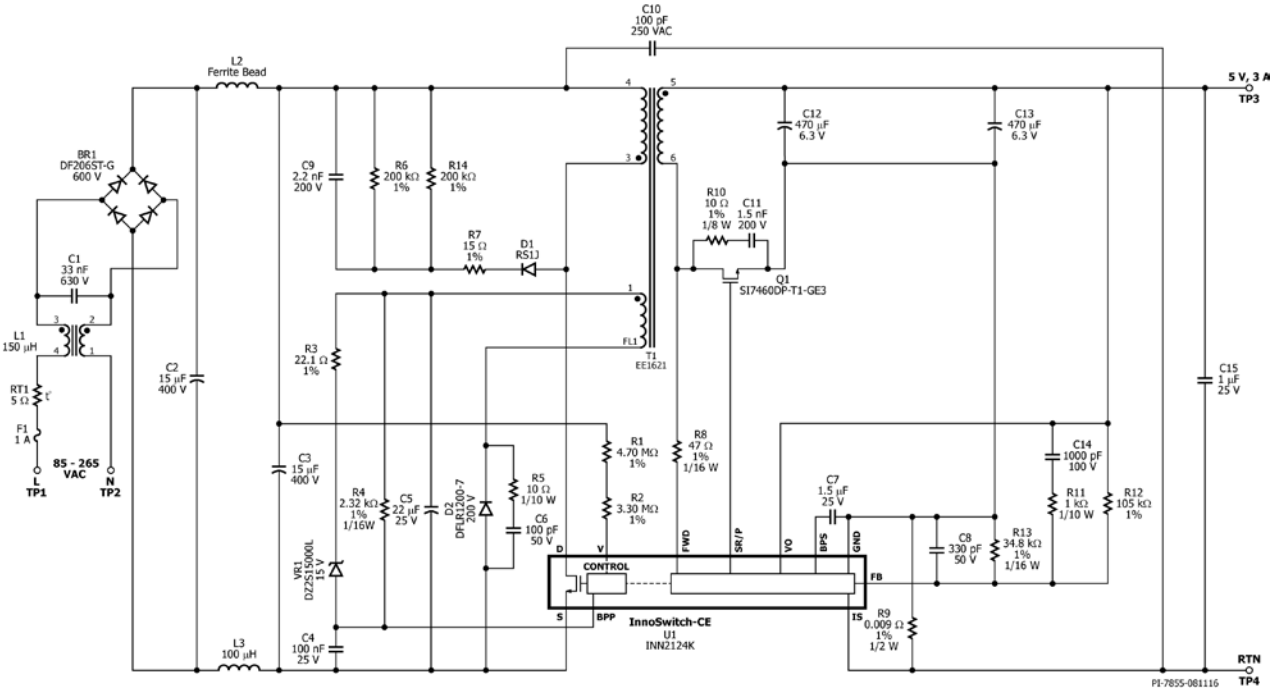

Figure 3 – Schematic.

4 Circuit Description

4.1 *Input EMI Filter and Rectifier*

Fuse F1 provides protection against catastrophic failure of components on the primary side.

An inrush limiting thermistor (RT1) ensures that the inrush current is below the surge current rating of the rectifier bridge BR1.

Physically small bridge rectifier BR1 was selected due to the limited space in compact charger designs.

Inductor L1 and capacitor C10 filter high frequency common mode noise. Leakage reactance of the common mode choke L1 and X-capacitor C1 provide differential filtering to reduce conducted EMI which is in addition to the differential filtering provided by the π (pi) filter comprising of capacitors C2 and C3 and inductors L2 and L3.

4.2 *InnoSwitch-CE IC Primary*

One side of the transformer primary is connected to the rectified DC bus, the other is connected to the drain terminal of the integrated power MOSFET inside the InnoSwitch-CE IC (U1).

A low cost RCD clamp formed by D1, R6, R7, R14 and C9 limits the peak drain voltage due to the effects of transformer and output trace inductance.

The IC is self-starting, using an internal high voltage current source to charge the BPP pin capacitor (C4) when AC is first applied. During normal operation the primary side block is powered from an auxiliary winding on the transformer. The output of this is configured as a flyback winding, rectified and filtered (D2 and C5) and fed in the BPP pin via a current limiting resistor R4. A snubber comprising of resistor R5 and capacitor C6 help to damp any high frequency ring across bias winding rectifier diode D2 and reduces radiated EMI.

Output regulation is achieved using On/Off control, the number of enabled switching cycles are adjusted based on the output load. At high load most switching cycles are enabled, and at light load or no-load most cycles are disabled or skipped. Once a cycle is enabled, the power MOSFET remain on until the primary current ramps to the device current limit for the specific operating state. There are four operating states (current limits) arrange such that the frequency content of the primary current switching pattern remains out of the audible range until at light load where the transformer flux density and therefore audible noise generation is at a very low level.

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Resistors R1 and R2 are used to sense the line voltage for the Line UV/OV detection feature built inside InnoSwitch-CE. If the line voltage was to drop below approximately 74V or rise above 320V, switching will be disabled automatically.

Resistor R3 and zener diode VR1 offer a primary sensed over voltage protection. In a flyback converter the voltages of windings configured as flyback windings track each other. If the output voltage of the power supply was to increase due to any failure of the controller to regulate due to board defect or component failure, the output of the bias winding increases as well and if the winding voltage increases to cause VR1 to conduct, a current in excess of the primary bypass pin shutdown threshold current I_{SD} flows into the BPP pin of IC U1 and causes the InnoSwitch-CE controller to latch off preventing switching and further runaway.

4.3 *InnoSwitch-CE IC Secondary*

The secondary side of the InnoSwitch-CE provides output voltage, output current sensing and drive to a MOSFET providing synchronous rectification.

The secondary of the transformer is rectified by Q1 and filtered by capacitors C12 and C13. High frequency ringing during switching transients that would otherwise create high voltage across Q1 and radiated EMI is reduced via snubber components R10 and C11.

To reduce dissipation synchronous rectification (SR) is provided by Q1. The gate of Q1 is turned on based on the winding voltage sensed via R8 and the FWD pin of the IC. In continuous conduction mode operation the power MOSFET is turned off just prior to the secondary side commanding a new switching cycle from the primary. In discontinuous mode the MOSFET is turned off when the voltage drop across the MOSFET falls below a threshold. Secondary side control of the primary side MOSFET ensure that it is never on simultaneously with the synchronous rectification MOSFET. The MOSFET drive signal is output on the SR/P pin.

The secondary side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. During CV operation the output voltage powers the device, fed into the VO pin.

During CC operation, when the output voltage falls the device will power itself from the secondary winding directly. During the on-time of the primary side MOSFET the forward voltage that appears across the secondary winding is used to charge the decoupling capacitor C7 via R8 and an internal regulator. The unit enters auto-restart when the sensed output voltage is lower than the auto-restart voltage threshold which has a typical value of 3.45V.

Output current is sensed internally between the IS and GND pins with a threshold of 35 mV to minimize losses. Resistor R9 is selected such that the drop across R9 is just

slightly higher than the CC threshold required. Once the internal current sense threshold is exceeded, the device adjusts the number of enabled switching cycles to maintain a fixed output current.

Below the CC threshold the device operates in constant voltage mode. The output voltage is sensed via resistor divider R12 and R13 operation with a reference voltage of 1.265 V on the FB pin when at the regulation output voltage. RC network comprising of R11 and C14 provides phase lead and ensures stable operation. Capacitor C8 offers filtering of the feedback signal from any high frequency noise.

Capacitor C15 at the output of the power supply provides decoupling and reduces high frequency radiated EMI.

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5 PCB Layout

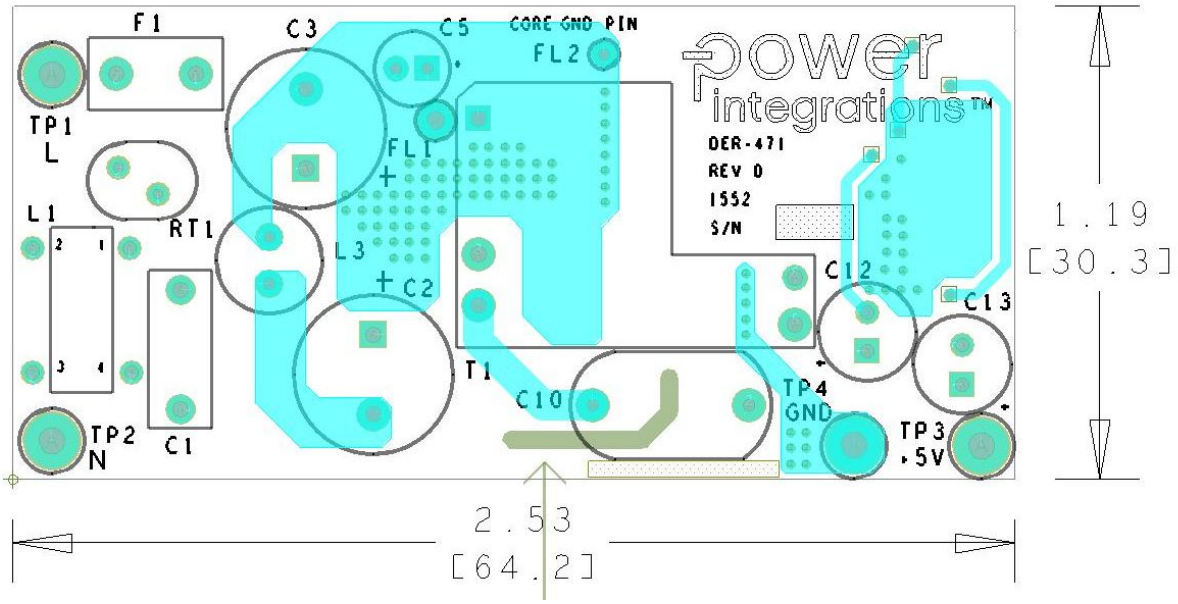

Figure 4 – Printed Circuit Layout, Top.

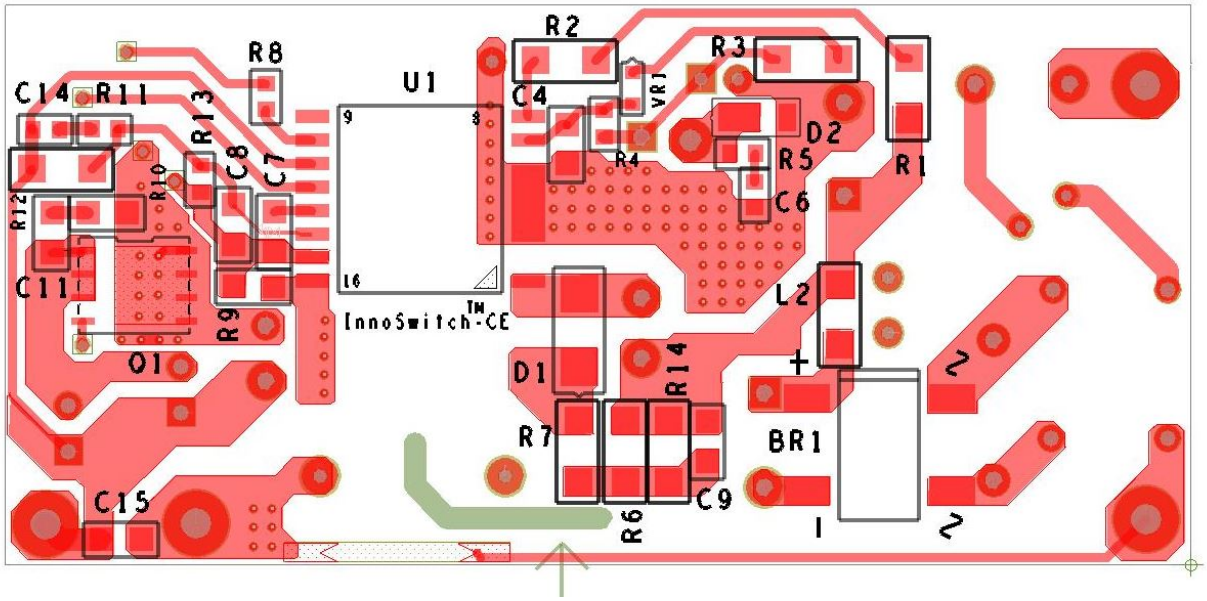

Figure 5 – Printed Circuit Layout, Bottom.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	600 V, 2 A, Bridge Rectifier, SMD, DFS	DF206ST-G	Comchip
2	1	C1	33 nF, 630 VAC, Polyester Film, X2	BFC233920333	Vishay
3	2	C2 C3	15 µF, 400 V, Electrolytic, (10 x 16)	UVC2G150MPD	Nichicon
4	1	C4	100 nF, 25 V, Ceramic, X7R, 0805	08053C104KAT2A	AVX
5	1	C5	22 µF, 25 V, Electrolytic, 20 %, Gen. Purpose, (5 x 7 mm)	EEA-GA1E220	Panasonic
6	1	C6	100 pF 50 V, Ceramic, NPO, 0603	CC0603JRNPO9BN101	Yageo
7	1	C7	1.5 µF, 25 V, Ceramic, X7R, 0805	C2012X7R1E155M125AC	TDK
8	1	C8	330 pF 50 V, Ceramic, X7R, 0603	CC0603KRX7R9BB331	Yageo
9	1	C9	2.2 nF, 200 V, Ceramic, X7R, 0805	08052C222KAT2A	AVX
10	1	C10	100 pF, 250 VAC, Film, X1Y1	DE1B3KX101KB4BN01F	TDK
11	1	C11	1.5 nF, 200 V,10%, Ceramic, X7R, 0805	08052C152KAT2A	AVX
12	2	C12 C13	470 µF, 6.3 V, 20%, Conductive Polymer aluminum, (6.3 x 8)	APSE6R3ELL471MF08S	United Chemi-con
13	1	C14	1000 pF, 100 V, Ceramic, NPO, 0603	C1608C0G2A102J	TDK
14	1	C15	1 µF, 25 V, Ceramic, X5R, 0805	C2012X5R1E105K	TDK
15	1	D1	600 V, 1 A, Fast Recovery, 250 ns, SMA	RS1J-13-F	Diodes, Inc.
16	1	D2	200 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1200-7	Diodes, Inc.
17	1	F1	1 A, 250 V, Slow, Long Time Lag, RST 1	RST 1	Belfuse
18	1	FL1	Flying Lead, Hole size 50 mils	N/A	N/A
19	1	FL2	Flying Lead , Hole size 30 mils	N/A	N/A
20	1	L1	Custom, Inductor, 150 µH,constructed on Core 35T0375-10H from PI# 30-00275-00	DER 471	Power Integrations
21	1	L2	Ferrite Bead, 220 Ω, 0.3A, 1206 SMD	742792122	Wurth
22	1	L3	100 µH, 0.490 A, 20%	RL-5480-2-100	Renco
23	1	Q1	60 V, 11 A, N-Channel, PowerPAK SO-8	SI7460DP-T1-GE3	Vishay
24	1	R1	RES, 4.70 MΩ, 1%, 1/4 W, Thick Film, 1206	KTR18EZPF4704	Rohm
25	1	R2	RES, 3.30 MΩ, 1%, 1/4 W, Thick Film, 1206	KTR18EZPF3304	Rohm
26	1	R3	RES, 22.1 Ω, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF22R1V	Panasonic
27	1	R4	RES, 2.32 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF2321V	Panasonic
28	1	R5	RES, 10 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ100V	Panasonic
29	2	R6 R14	RES, 200 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2003V	Panasonic
30	1	R7	RES, 15 Ω, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF15R0V	Panasonic
31	1	R8	RES, 47.0 Ω, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF47R0V	Panasonic
32	1	R9	RES, 0.009 Ω, 0.5 W, 1%, 0805	CRF0805-FX-R009ELF	Bourns
33	1	R10	RES, 10 Ω, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF10R0V	Panasonic
34	1	R11	RES, 1 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ102V	Panasonic
35	1	R12	RES, 105 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1053V	Panasonic
36	1	R13	RES, 34.8 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF3482V	Panasonic
37	1	RT1	NTC Thermistor, 5 Ω, 1 A	MF72-005D5	Cantherm
38	1	T1	Bobbin, EE1621, Vertical, 8 pins, 4pri, 4sec	EE-1621	Shen Zhen Xin Yu Jia Tech
39	2	TP1 TP4	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone
40	1	TP2	Test Point, WHT, THRU-HOLE MOUNT	5012	Keystone
41	1	TP3	Test Point, RED, THRU-HOLE MOUNT	5010	Keystone
42	1	U1	InnoSwitch-CE, 650 V, ReSOP-16B	INN2124K	Power Integrations
43	1	VR1	15 V, 5%, 150 mW, SSMINI-2	DZ2S15000L	Panasonic-SSG

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7 Transformer (T1) Specification

7.1 *Electrical Diagram*

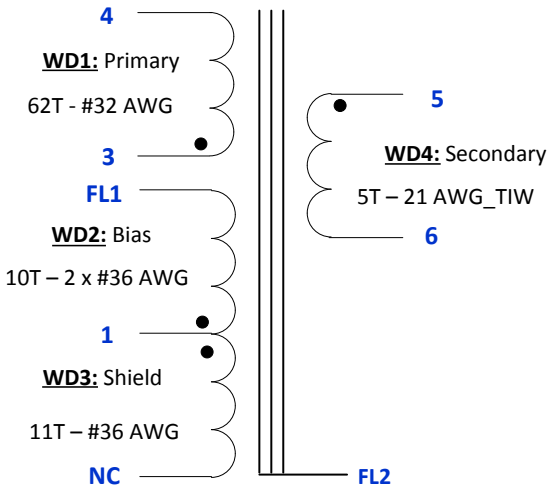

Figure 6 – Transformer Electrical Diagram.

7.2 *Electrical Specifications*

Parameter	Condition	Spec.
Primary Inductance	Pins 3 – 4, all other windings open, measured at 100 kHz, 0.4 V_{RMS}.	711 µH ±7%
Resonant Frequency	Pins 3 – 4, all other windings open, measured at 100 kHz, 0.4 V_{RMS}.	1200 kHz (Min.)
Primary Leakage Inductance	Pin 3 – 4, with Pins 5/6 shorted, measured at 100 kHz, 0.4 V_{RMS}.	27 µH (Max.)

7.3 *Material List*

Item	Description
[1]	Core: EE1621; PC-95 or equivalent; gapped for ALG of 185nH/t². Core Used: Hongkang Magnetic Electronic Co. Ltd Part# HP95-E16/12.3/7.2
[2]	Bobbin: EE-1621 – Vertical - 8 pins (4/4), PI#: 25-01044-00 Manufacturer: Shen Zhen Xin Yu Jia Technology Ltd.
[3]	Magnet Wire: #32 AWG, Solderable Double Coated..
[4]	Magnet Wire: #36 AWG, Solderable Double Coated.
[5]	Magnet Wire: #21 AWG, Triple Insulated Wire.
[6]	Tape: 3M 1298 Polyester Film, 2 mil thick, 5.5 mm Wide.
[7]	Bus wire: #26 AWG, Belden Electronics Div; or Equivalent.
[8]	Varnish: Dolph BC-359.

7.4 *Transformer Build Diagram*

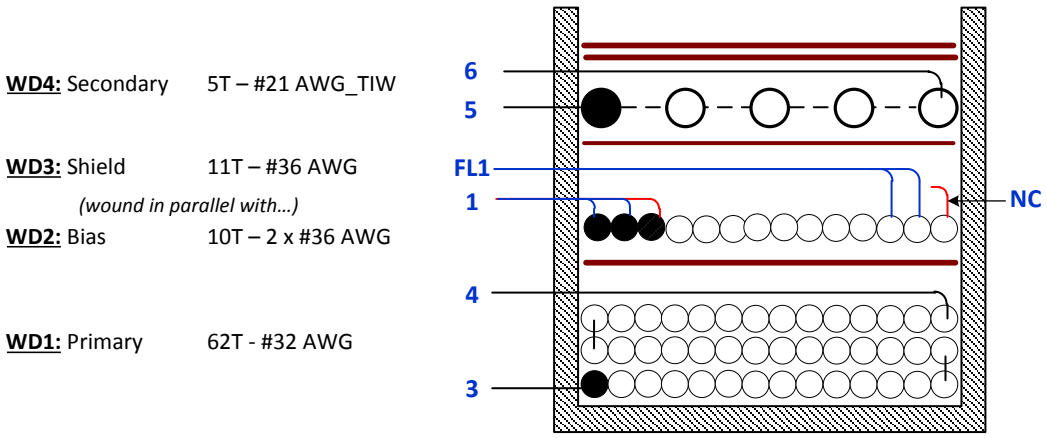

Figure 7 – Transformer Build Diagram.

7.5 *Winding Instructions*

Bobbin Preparation	For the purpose of these instructions, bobbin is oriented on winder such that pin side is on the left side. Winding direction is clockwise direction.
WD1 Primary	Start at pin 3. Wind 62 turns of item [3] in approximately 3 layers. Finish at pin 4.
Insulation	Use 1 layer of item [6] for insulation.
WD2 & WD3 Bias & Shield	Use 3 wires (trifillar) of item [4], start at pin 1, wind 10 turns from left to right. At the 10th turn, bring 2 wires to the left, and leave floating FL1 for bias winding. Continue winding the 3rd wire with 1 more turn, cut short to leave it with no-connection for shield winding.
Insulation	Use 1 layer of item [6] for insulation.
WD4 Secondary	Start at pin 5. Wind 5 turns of item [5] in 1 layer. Finish at pin 6.
Insulation	Use 2 layers of item [6] to secure the windings.
Final Assembly	Gap core halves to get 711 µH inductance. Wrap core halves and bus wire item [7] with tape item [6] (see illustration below). Varnish the transformer with item [8].

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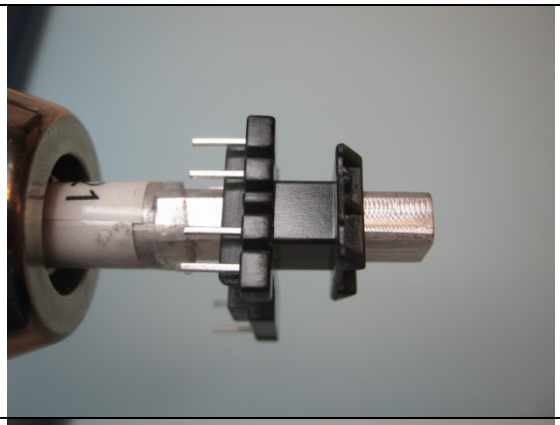
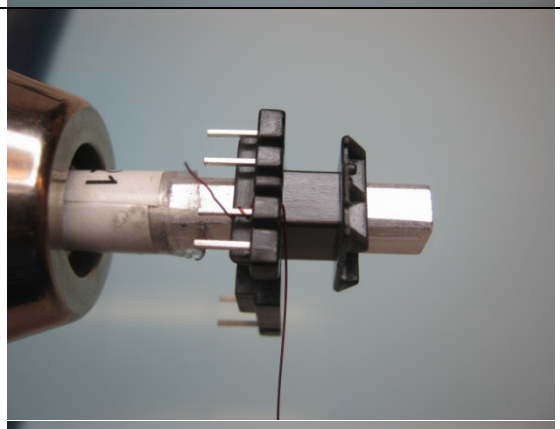
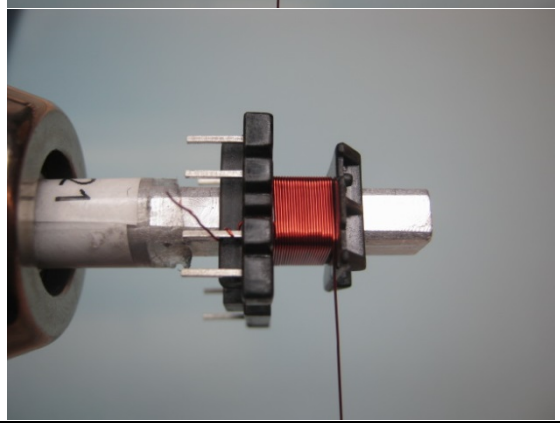
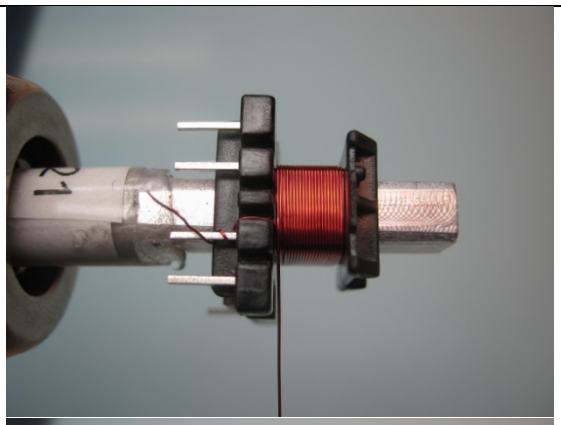
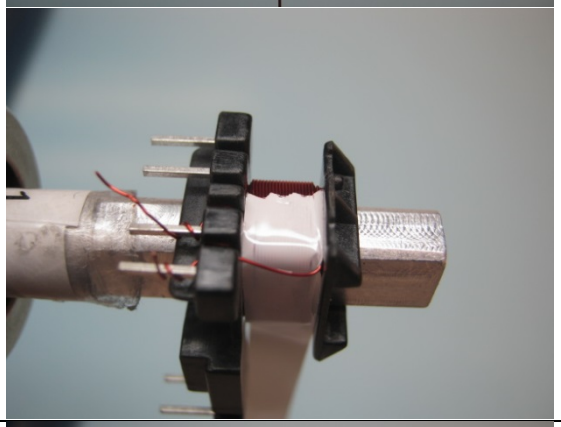
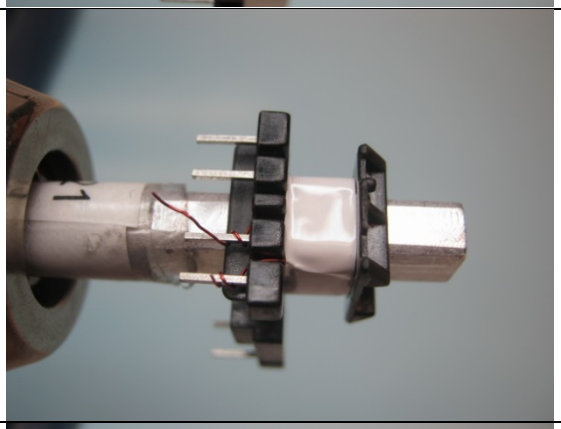
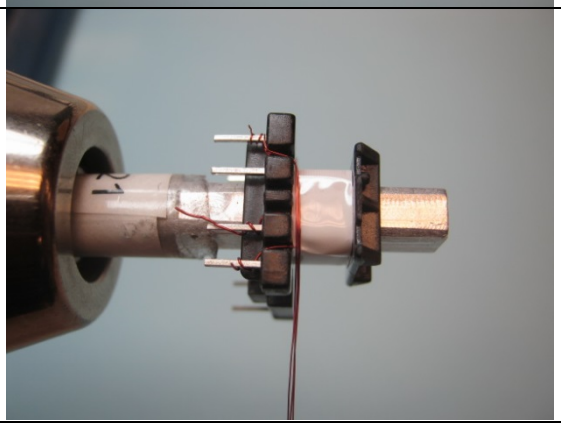
7.6 *Winding Illustrations*

Bobbin Preparation		For the purpose of these instructions, bobbin is oriented on winder such that pin side is on the left side. Winding direction is clockwise direction.
WD1 **Primary**	 	Start at pin 3. Wind 62 turns of item [3] in approximately 3 layers. Finish at pin 4.

	 	
Insulation		Use 1 layer of item [6] for insulation.
WD2 & WD3 Bias & Shield		Use 3 wires (trifillar) of item [4], start at pin 1, wind 10 turns from left to right. At the 10th turn, bring 2 wires to the left, and leave floating FL1 for bias winding. Continue winding the 3rd wire with 1 more turn, cut short to leave it with no-connection for shield winding.

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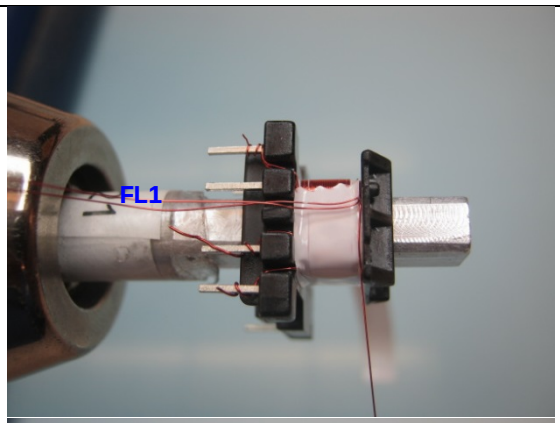
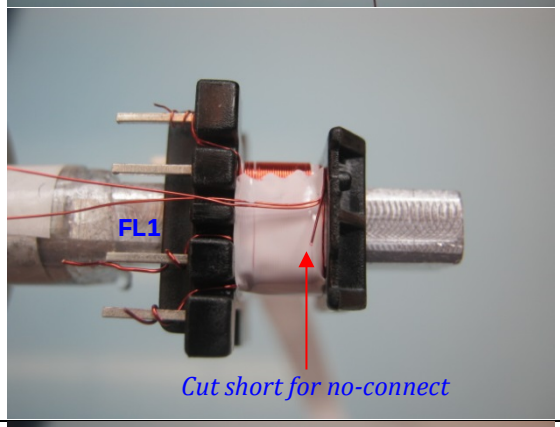
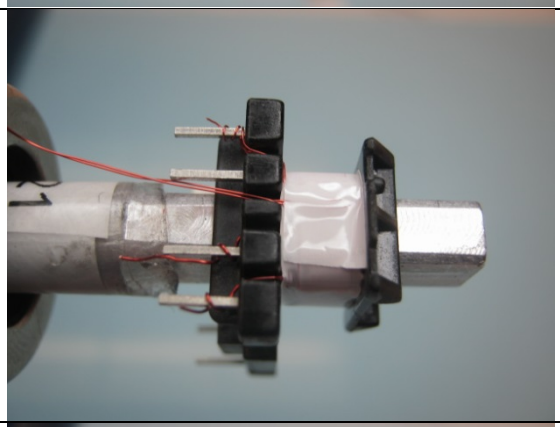
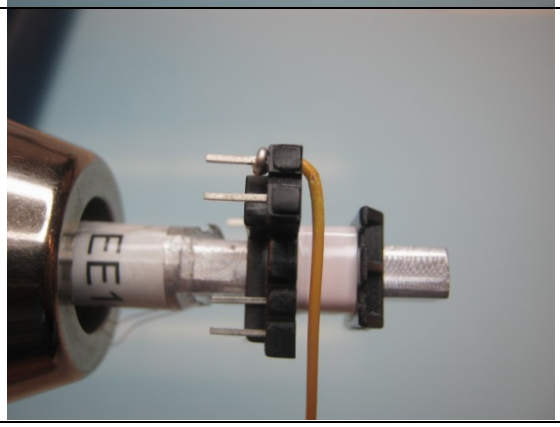
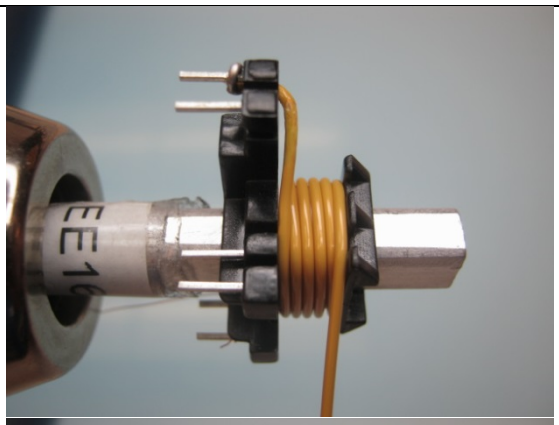
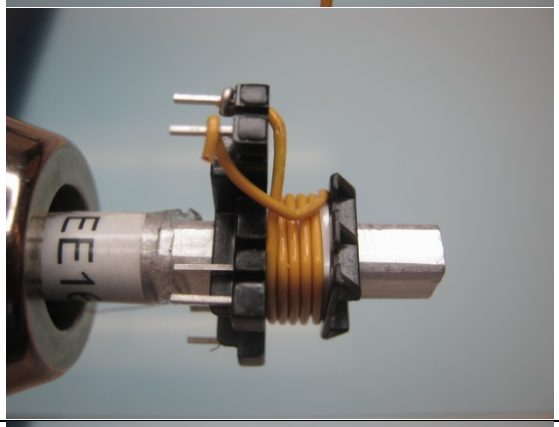
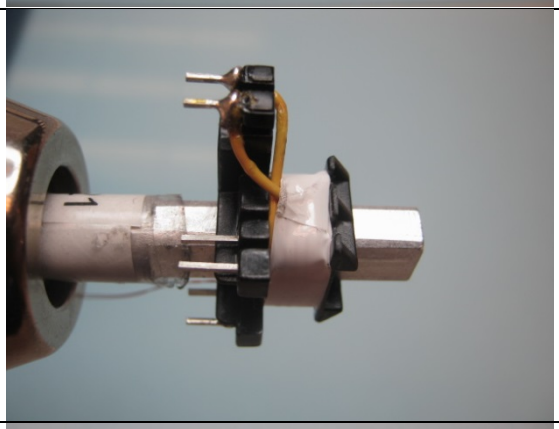
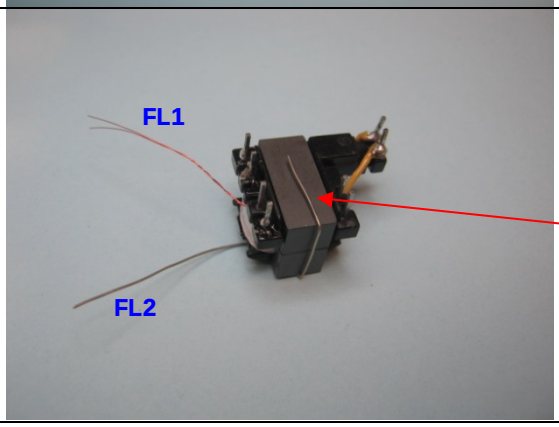
	 	
Insulation		Use 1 layer of item [6] for insulation.
WD4 Secondary		Start at pin 5. Wind 5 turns of item [5] in 1 layer. Finish at pin 6.

	 	
Insulation		Use 2 layers of item [6] to secure the windings.
Final Assembly		Gap core halves to get 711 µH inductance. Wrap core halves and bus wire item [7] with tape item [6] (see illustration). Varnish the transformer with item [8].

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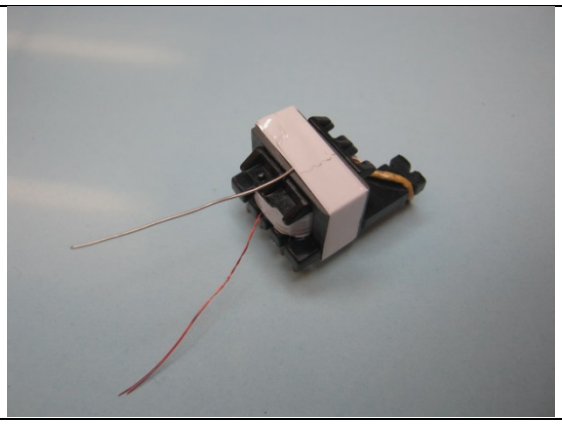
		

8 150 µH Common Mode Choke (L1) Specification

8.1 *Electrical Diagram*

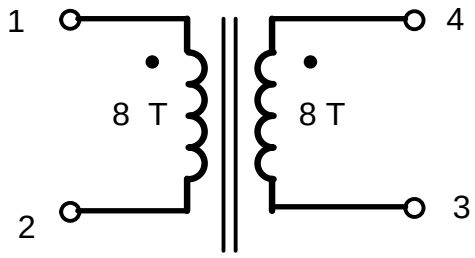


Figure 8 – Inductor Electrical Diagram.

8.2 *Electrical Specifications*

Parameter	Condition	Spec.
Inductance	Pins 1-2, all other windings open.	150 µH +15% / -25%
Primary Leakage Inductance	Pins 1-2, with 3-4 shorted.	1.5 µH

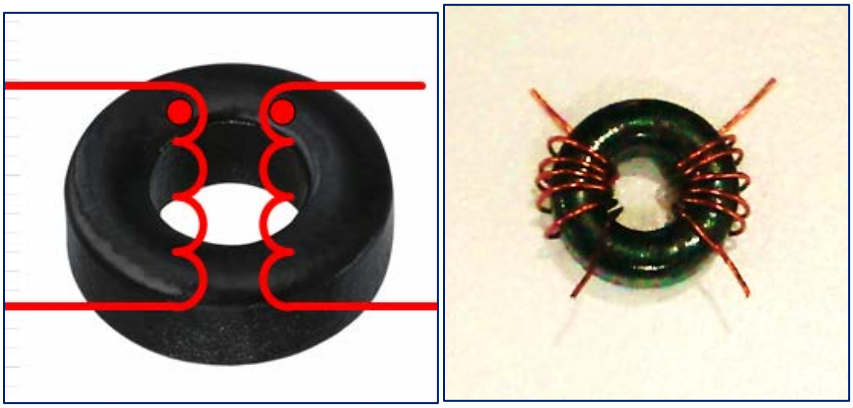
8.3 *Material List*

Item	Description
1	Toroid: Steward; Mfg#: 35T0375-10H; 9.53 mm O.D. x 4.75 mm I.D. x 3.18 mmTH. PI#: 32-00275-00; Or: JLW (HK) Electronics, MF#: T*9.00*5.00*3.00, PI#: 32-00330-00.
2	Magnet Wire: #30 AWG Single Coated.

8.4 *Winding Instructions*

- Wind 8 turns individually separated from each other as depicted below.
- Measure the inductance (should be 150 µH +15%/- 25%).

8.5 *Illustrations*



Note: Do not interleave both the windings.

Figure 9 – CMC Build Illustration.

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9 Transformer Design Spreadsheet

ACDC_InnoSwitch-CE_031116; Rev.1.0; Copyright Power Integrations 2016	INPUT	INFO	OUTPUT	UNIT	InnoSwitch-CE Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					
VACMIN	85		85	V	Minimum AC Input Voltage
VACMAX	265		265	V	Maximum AC Input Voltage
fL	50		50	Hz	AC Mains Frequency
VO	5.00		5.00	V	Output Voltage (continuous power at the end of the cable)
IO	3.04		3.04	A	Power Supply Output Current (corresponding to peak power)
Power			16.11	W	Continuous Output Power, including cable drop compensation
n	0.82		0.82		Efficiency Estimate at output terminals. Use 0.8 if no better data available
Z	0.50		0.50		Z Factor. Ratio of secondary side losses to the total losses in the power supply. Use 0.5 if no better data available
tC			3.00	mSeconds	Bridge Rectifier Conduction Time Estimate
CIN	30.00		30.00	uFarad	Input Capacitance
Enclosure	Adapter		Adapter		Power supply enclosure
ENTER InnoSwitch-CE VARIABLES					
InnoSwitch-CE	INN21X4		INN21X4		User defined InnoSwitch
Cable drop compensation	6%		6%		Select Cable Drop Compensation option
Complete Part Number			INN2124		Final part number including package
Chose Configuration	STD		Standard Current Limit		Enter "RED" for reduced current limit (sealed adapters), "STD" for standard current limit or "INC" for increased current limit (peak or higher power applications)
ILIMITMIN			0.799	A	Minimum Current Limit
ILIMITTYP			0.850	A	Typical Current Limit
ILIMITMAX			0.901	A	Maximum Current Limit
fSmin			93000	Hz	Minimum Device Switching Frequency
I^2fmin			62.86	A^2kHz	Worst case I2F parameter across the temperature range
VOR	63		63	V	Reflected Output Voltage (VOR <= 100 V Recommended)
VDS			5.00	V	InnoSwitch on-state Drain to Source Voltage
KP			0.628		Ripple to Peak Current Ratio at Vmin, assuming ILIMITMIN, and I2FMIN (KP < 6)
KP_TRANSIENT			0.344		Worst case transient Ripple to Peak Current Ratio. Ensure KP_TRANSIENT > 0.25
ENTER InnoSwitch-CE PROTECTION VARIABLES					
Line Undervoltage					
BROWN IN	74.0		73.6	VRMS	Minimum RMS AC Voltage at which the power supply will BROWN-IN (turn-on). The actual value of this voltage may differ slightly from the desired value due to the V-pin resistor's tolerance
BROWN OUT			60.4	VRMS	Typical RMS AC Voltage at which the power supply will BROWN-OUT (turn-off) under conditions of line-undervoltage
RLS			8.09	MOhms	Theoretical V-pin resistor for the desired UV/OV setup
RLS1/RLS2			4.02	MOhms	Standard value of a single 1% resistor, assuming 2 series resistors are used
VBROWNIN VARIATION			-0.61	%	Variation between the actual and desired brown-in voltage
Line Overvoltage					

BROWN IN			303.8	VRMS	Typical RMS AC voltage at which the power supply will BROWN-IN (turn-on) after a line overvoltage BROWN-OUT (turn-off) event
BROWN OUT			319.8	VRMS	Typical RMS AC voltage at which the power supply will BROWN-OUT (turn-off) under conditions of line-overvoltage
Load Overcurrent					
IOMAX			3.87	A	Load current beyond which the device will enter into overload protection. By default value consists of the sum of all output currents multiplied by 1.2
RIS			0.009	Ohms	Use a 0.009 Ohm, 1-5% resistor having a minimum power rating of 0.1353408W on the IS pin for load overcurrent protection
ENTER BIAS WINDING VARIABLES					
VB			10.00	V	Bias Winding Voltage
VDB			0.70	V	Bias Winding Diode Forward Voltage Drop
NB			9.88	V	Bias Winding Number of Turns
PIVB			95.58	V	Bias winding peak reverse voltage at VACmax and assuming VB*1.2
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	Custom		Custom		Enter Transformer Core
Core	EE1621		EE1621		Enter core part number, if necessary
Bobbin	25-01044-00		25-01044-00		Enter bobbin part number, if necessary
AE	0.32		0.32	cm^2	Core Effective Cross Sectional Area
LE	3.93		3.93	cm	Core Effective Path Length
AL	2800		2800	nH/T^2	Ungapped Core Effective Inductance
BW	5.40		5.40	mm	Bobbin Physical Winding Width
M			0.00	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	3		3		Number of Primary Layers
NS	5		5		Number of Secondary Turns
DC INPUT VOLTAGE PARAMETERS					
VMIN			73	V	Minimum DC Input Voltage
VMAX			375	V	Maximum DC Input Voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.48		Duty Ratio at full load, minimum primary inductance and minimum input voltage
IAVG			0.26	A	Average Primary Current
IP			0.80	A	Peak Primary Current assuming ILIMITMIN
IR			0.50	A	Primary Ripple Current assuming ILIMITMIN, and LPMIN
IRMS			0.39	A	Primary RMS Current, assuming ILIMITMIN, and LPMIN
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			710	uHenry	Typical Primary Inductance. +/- 7% to ensure a minimum primary inductance of 660 uH
LP_TOLERANCE	7		7	%	Primary inductance tolerance
NP			62		Primary Winding Number of Turns
ALG			185	nH/T^2	Gapped Core Effective Inductance
BM		Warning	3615	Gauss	!!! Warning. Maximum flux density too high, may cause transformer saturation. REDUCE BP<3000. Increase NS , use larger Core or increase VOR
BAC			1135	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			2736		Relative Permeability of Ungapped Core
LG			0.20	mm	Gap Length (Lg > 0.1 mm)
BWE			16.2	mm	Effective Bobbin Width
OD	0.26		0.26	mm	Maximum Primary Wire Diameter including insulation
INS			0.049	mm	Estimated Total Insulation Thickness (= 2 * film thickness)

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DIA			0.211	mm	Bare conductor diameter
AWG			32	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			64	Cmils	Bare conductor effective area in circular mils
CMA		Warning	163	Cmils/Amp	!!! INCREASE CMA > 200 (increase L(primary layers),decrease NS, use larger Core)
TRANSFORMER SECONDARY DESIGN PARAMETERS					
Lumped parameters					
ISP			9.91	A	Peak Secondary Current, assuming ILIMITMIN
ISRMS			5.06	A	Secondary RMS Current
IRIPPLE			4.04	A	Output Capacitor RMS Ripple Current
CMS			1012	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			20	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
VOLTAGE STRESS PARAMETERS					
VDRAIN			527	V	Maximum Drain Voltage Estimate
PIVS			48	V	Output Rectifier Maximum Peak Inverse Voltage for 1st output, assuming the primary has a Voltage spike 40% above VMAX and VO*1.05
TRANSFORMER SECONDARY DESIGN PARAMETERS					
1st output					
VO1			5.30	V	Main Output Voltage directly after output rectifier
IO1			3.22	A	Output DC Current
PO1			17.08	W	Output Power
VD1			0.06	V	Output Synchronous Rectification FET Forward Voltage Drop
NS1			5.00	Turns	Output Winding Number of Turns
ISRMS1			5.36	A	Output Winding RMS Current
IRIPPLE1			4.29	A	Output Capacitor RMS Ripple Current
PIVS1			48	V	Output Rectifier Maximum Peak Inverse Voltage, assuming the primary has a Voltage spike 40% above VMAX and VO*1.05
CMS1			1072	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS1			19	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS1			0.91	mm	Minimum Bare Conductor Diameter
ODS1			1.08	mm	Maximum Outside Diameter for Triple Insulated Wire
Recommended MOSFET			QM6006		Recommended SR FET for this output
RDSON_HOT			0.03	Ohm	RDSon at 100C
VRATED			60	V	Rated voltage of selected SR FET

Note: The spreadsheet shows two warnings and they can be safely ignored for the following reasons:

1. The first warning is for peak flux density since the computed maximum flux density is 3615 Gauss. The core material used for this design has a saturation flux density that exceeds 3900 Gauss when the transformer core temperature is 100 ºC and hence this warning can be ignored.

2. The second warning is for current density. A lower current density in the wire can lead to higher transformer temperature though the actual temperature of the transformer is dependent on the total loss in the transformer and the transformer surface area. Thermal data is presented in this report that shows that the transformer temperature is well below the limits and hence this warning can also be ignored.

10 Performance Data

Note: All measurements performed at the end of cable. Cable drop is 300 mV for 3 A load current.

Average Efficiency Requirements						
Test	Average	Average	Average	Average	10% Load	10% Load
Model	<6 V Voltage	<6 V Voltage	<6 V Voltage	<6 V Voltage	<6 V Voltage	<6 V Voltage
Standard	Energy Star 2	New EISA2007	CoC v5 Tier 1	CoC v5 Tier 2	CoC v5 Tier 1	CoC v5 Tier 2
Efficiency	77.2%	81.4%	79.0%	81.8%	69.5%	72.5%

V_{IN} = 115 V					
Load (%)	**V_{OUT} (V)**	**Load (A)**	**P_{IN} (W)**	**Efficiency (%)**	**Average Efficiency (%)**
100	4.94	3.00	18.38	80.59	
75	5.01	2.25	13.63	82.70	
50	5.06	1.50	9.05	83.85	
25	5.07	0.75	4.50	84.60	82.94
10	5.08	0.30	1.87	81.24	

V_{IN} = 230 V					
Load (%)	**V_{OUT} (V)**	**Load (A)**	**P_{IN} (W)**	**Efficiency (%)**	**Average Efficiency (%)**
100	4.98	3.00	18.27	81.70	
75	5.04	2.25	13.56	83.53	
50	5.07	1.50	9.00	84.47	
25	5.07	0.75	4.51	84.32	83.51
10	5.08	0.30	1.91	79.60	

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10.1 *Active Mode Efficiency – End of Cable*

Note: All measurements are made at the end of simulated cable using 100 mΩ resistor unless otherwise specified. 30 minutes soak time at start and 5 minutes wait time between each data point were provided.

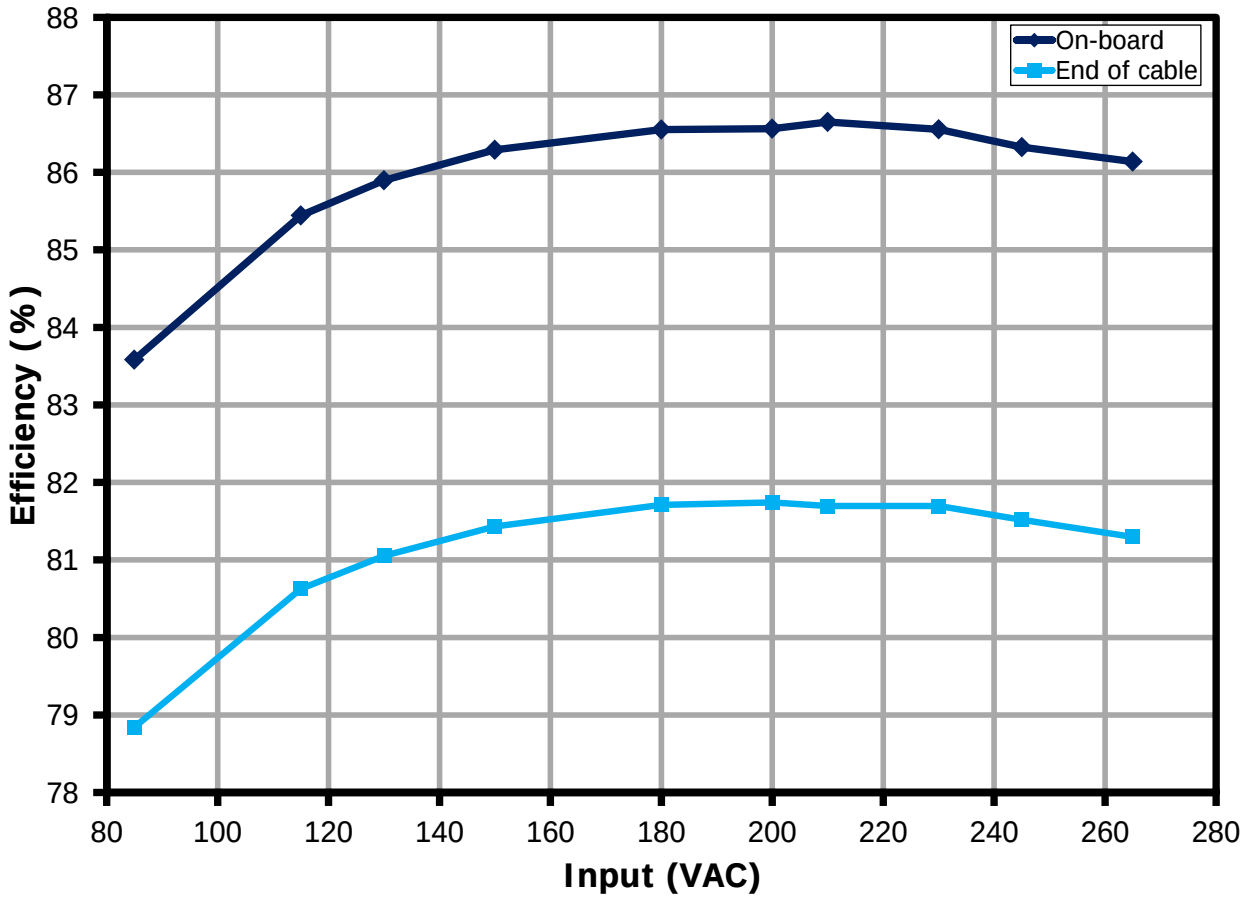

Figure 10 – Efficiency vs Line Voltage, Room Temperature.

10.2 *Active Mode Efficiency – On Board*

Note: All measurements are taken on-board, at the board terminals. 30 minutes soak time at start and 5 minutes wait time between each data point were provided.

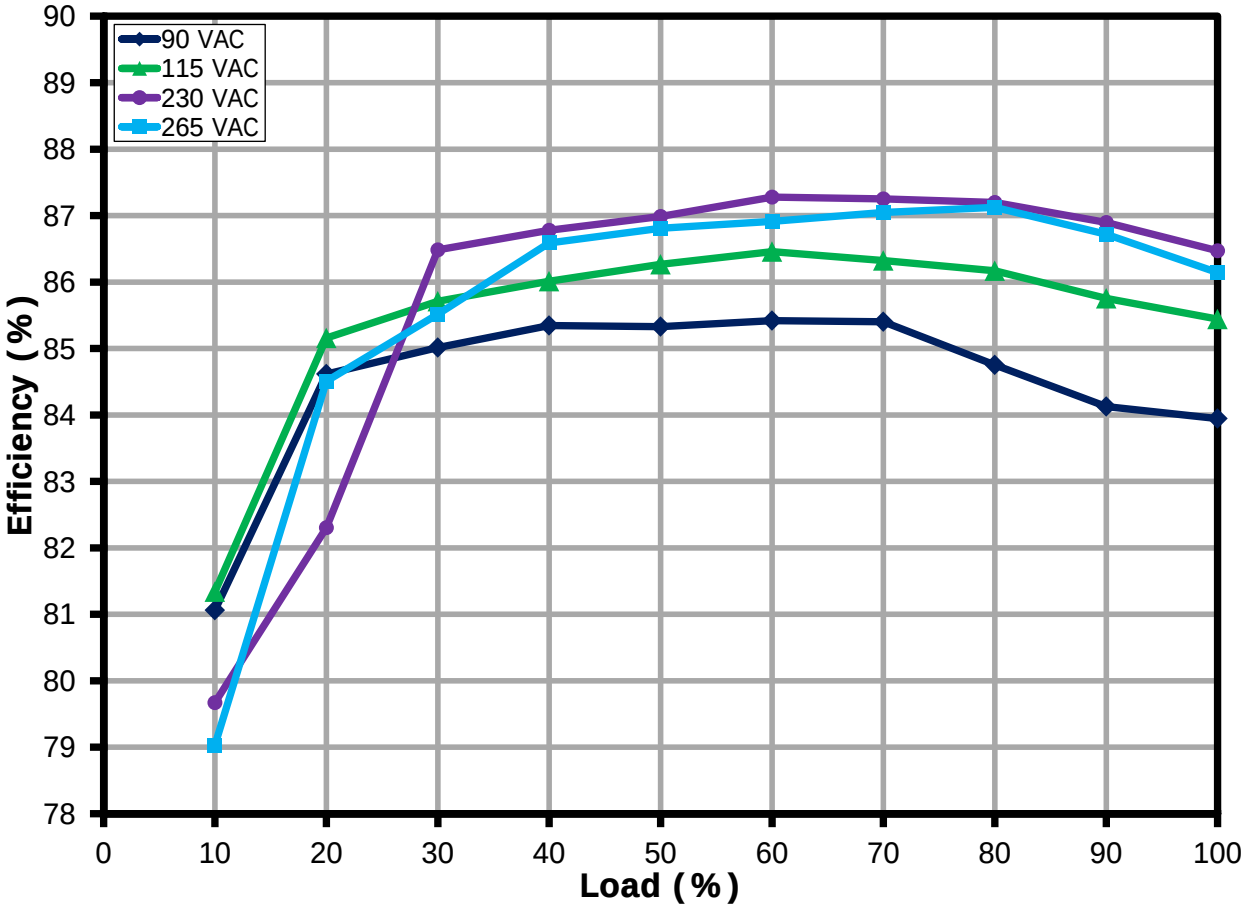

Figure 11 – Efficiency (On Board) vs Load, Room Temperature.

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10.3 *Active Mode Efficiency – End of Cable*

Note: All measurements are taken at the end of the simulated cable using 100 mΩ resistor. 30 minutes soak time at start and 5 minutes wait time between each data point were provided.

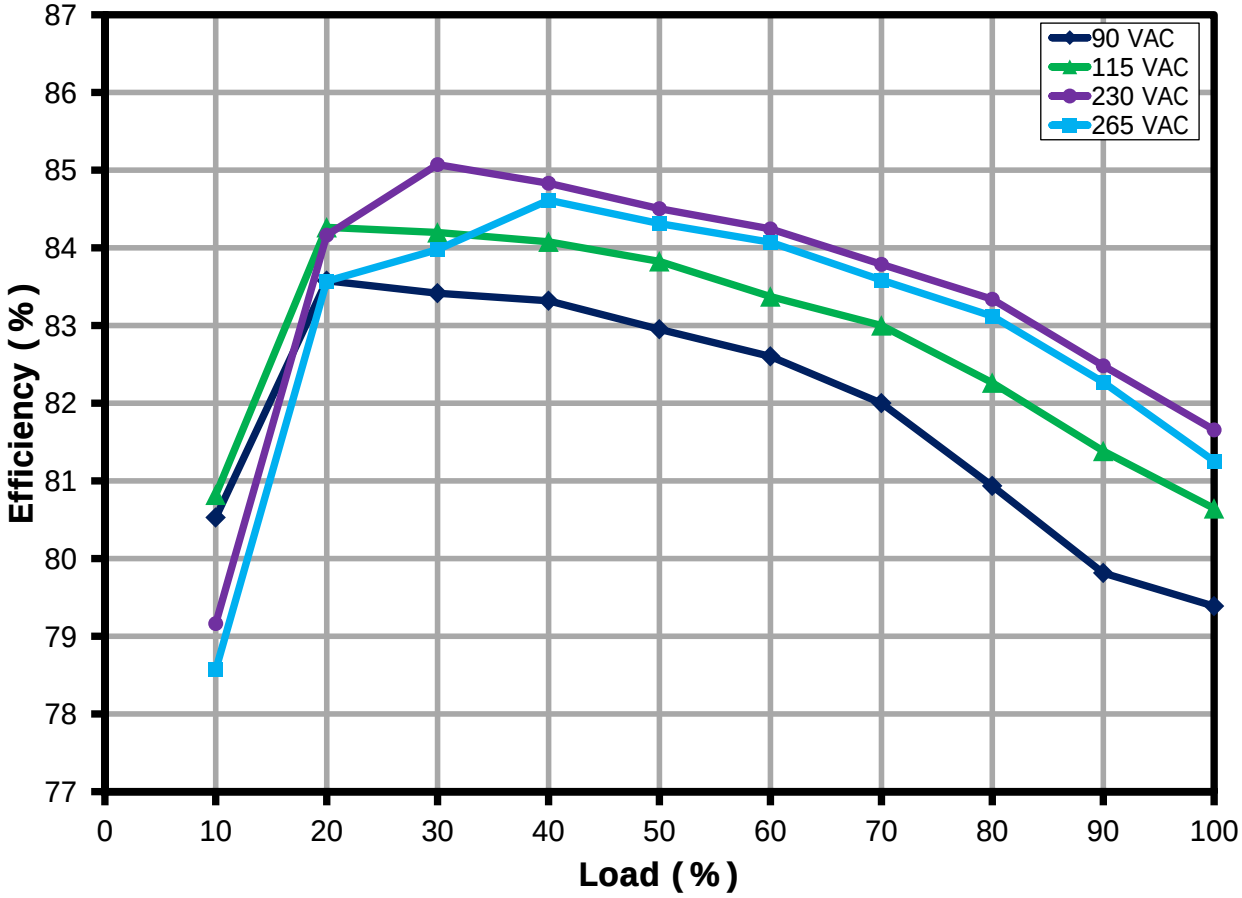

Figure 12 – Efficiency (End of cable) vs Load, Room Temperature.

10.4 *No-Load Input Power*

15 minutes soak time and 5 minutes integration time were used.

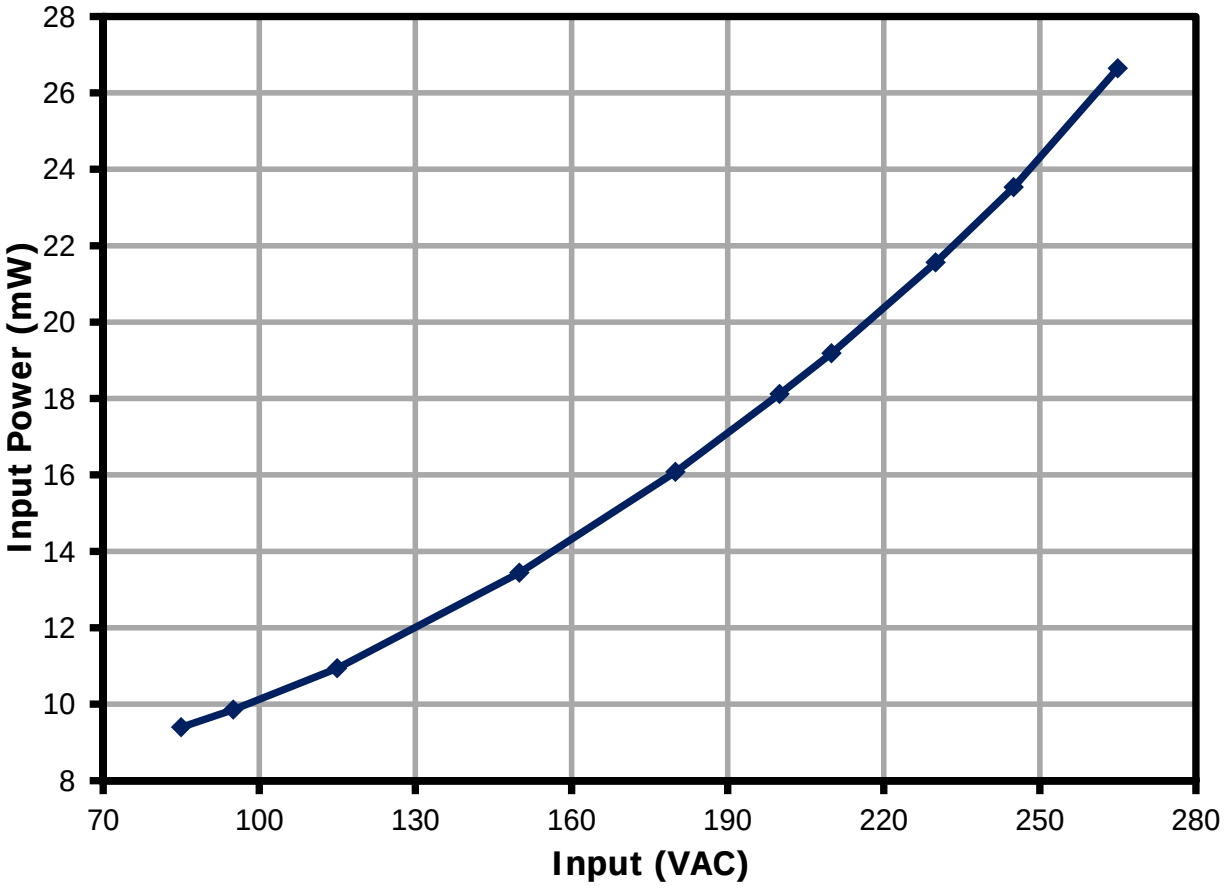

Figure 13 – No-Load Input Power vs. Input Line Voltage, Room Temperature.

V_{IN} (V)	No-Load Power (mW)
85	9.398
95	9.858
115	10.942
150	13.439
180	16.080
200	18.116
210	19.182
230	21.558
245	23.532
265	26.641

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10.5 *CV/CC Characteristics – On Board*

All measurements are taken on-board, at the start of the simulated cable using 100 mΩ resistor. A 47 uF electrolytic capacitor was used across the E-load input.

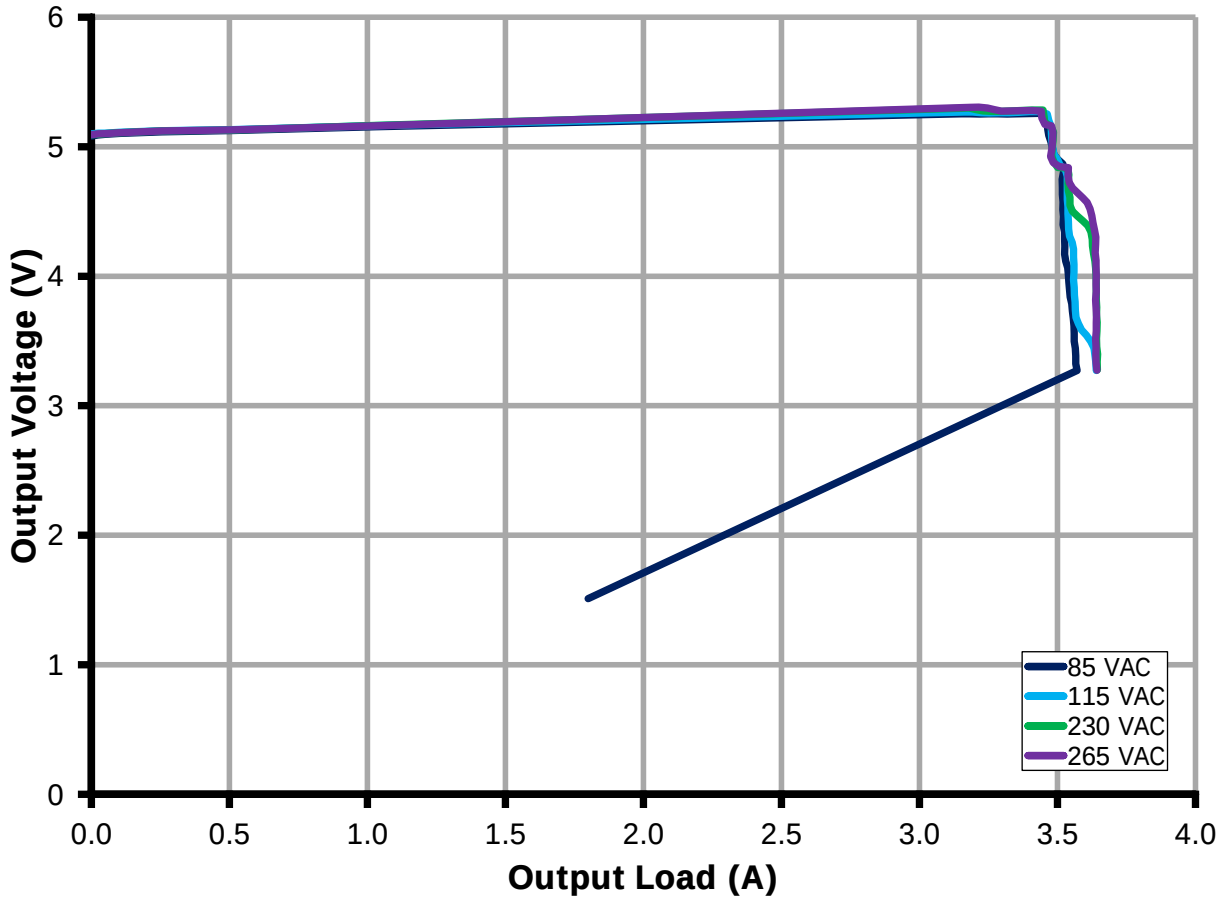

Figure 14 – CV/CC Characteristics Measured on Board.

10.6 *CV/CC Characteristics – End of Cable*

All measurements are taken at the end of the simulated cable using 100 mΩ resistor. A 47 µF electrolytic capacitor was used across the E-load input.

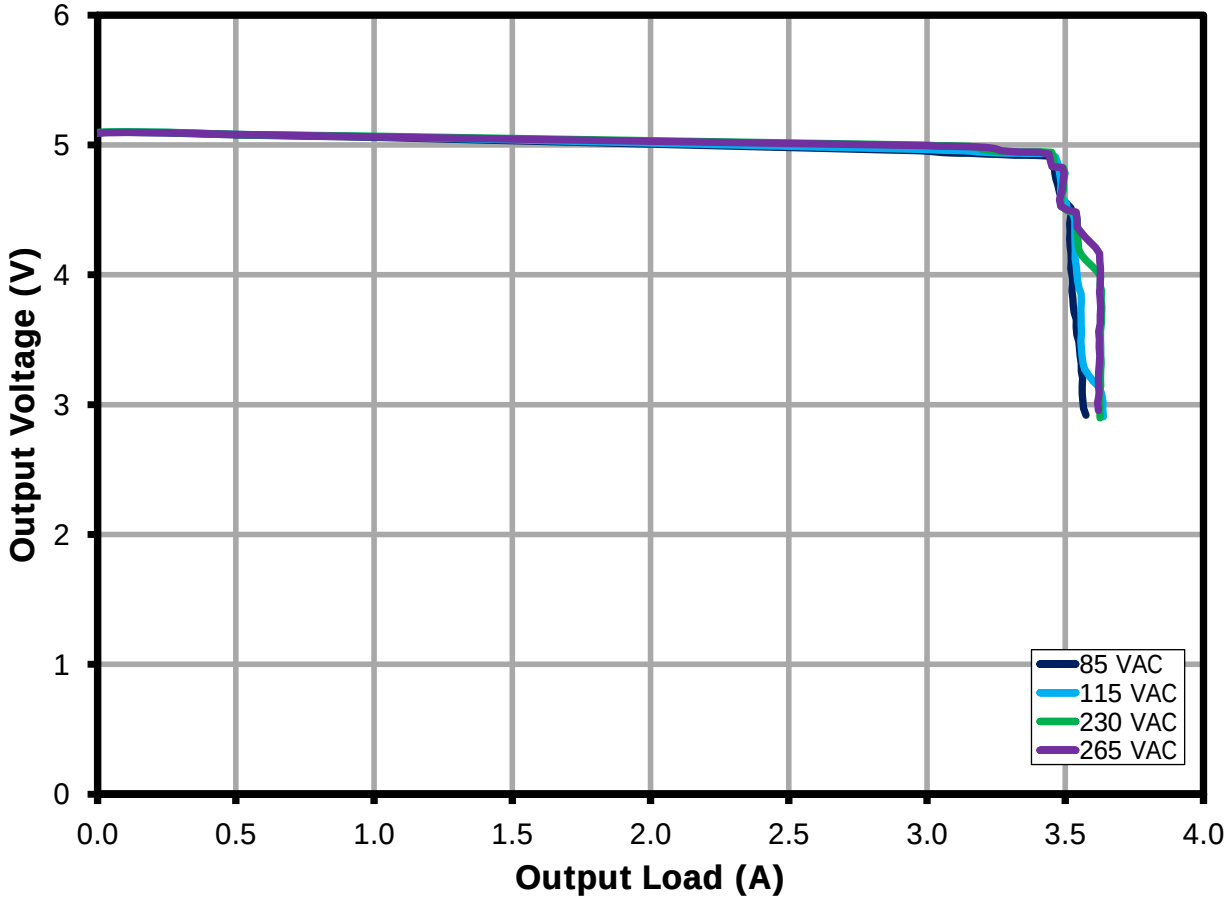

Figure 15 – CV/CC Characteristics Measured at the End of Cable.

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11 Thermal Performance

11.1 *85 VAC, Room Temperature*

Figure 16 – Bottom Side. 85 VAC, Full Load.
Sp1 – Clamp Diode – 80.7 °C.
Sp2 – InnoSwitch-CE – 81.6 °C.
Sp3 – SRFET – 78 °C.

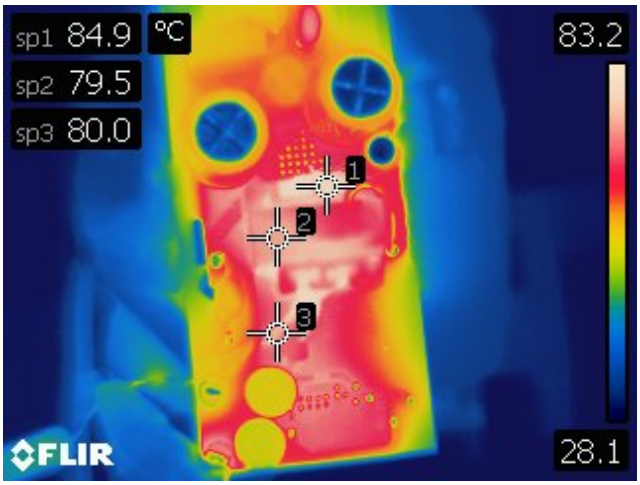

Figure 17 – Top Side. 85 VAC, Full Load.
Sp1 – Transformer Secondary Winding – 84.9 °C.
Sp2 – Transformer Core – 79.5 °C.
Sp3 – Transformer Wire Secondary Winding – 80 °C.

11.2 *265 VAC, Room Temperature*

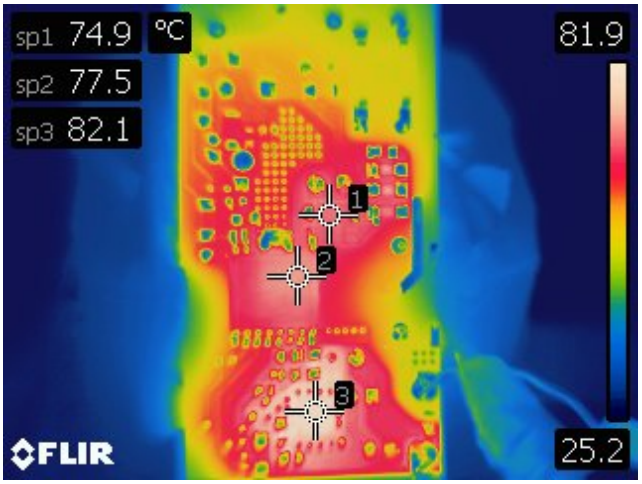

Figure 18 – Bottom Side. 265 VAC, Full Load.
Sp1 – Clamp Diode – 74.9 °C.
Sp2 – InnoSwitch-CE – 77.5 °C.
Sp3 – SRFET – 82.1 °C.

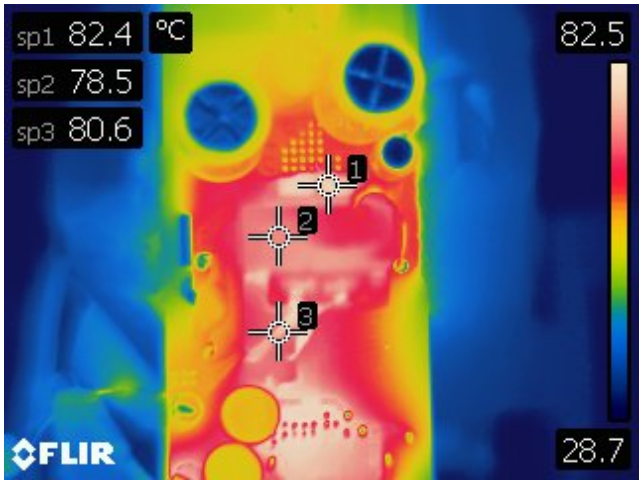

Figure 19 – Top Side. 265 VAC, Full Load.
Sp1 – Transformer Secondary Winding – 82.4 °C.
Sp2 – Transformer Core – 78.5 °C.
Sp3 – Transformer Wire Secondary Winding – 80.6 °C.

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12 Waveforms

12.1 *Output Voltage Start-up Waveform*

Figure 20 – V_{IN} = 85 VAC, No-Load.
C2 Green: V_{OUT}, 1 V / div., 2 ms / div.
C4 Red: I_{OUT}, 1 A / div., 2 ms / div.
$V_{OUT(MAX)}$ = 5.12 V.

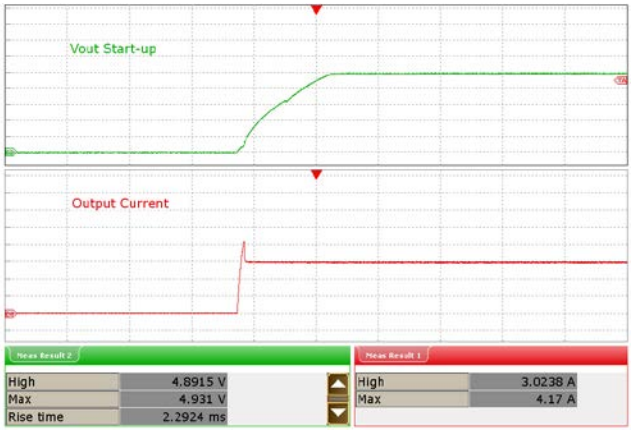

Figure 21 – V_{IN} = 85 VAC, Full Load.
C2 Green: V_{OUT}, 1 V / div., 2 ms / div.
C4 Red: I_{OUT}, 1 A / div., 2 ms / div.
$V_{OUT(MAX)}$ = 4.93 V.

Figure 22 – V_{IN} = 115 VAC, No-Load.
C2 Green: V_{OUT}, 1 V / div., 2 ms / div.
C4 Red: I_{OUT}, 1 A / div., 2 ms / div.
$V_{OUT(MAX)}$ = 5.12 V.

Figure 23 – V_{IN} = 115 VAC, Full Load.
C2 Green: V_{OUT}, 1 V / div., 2 ms / div.
C4 Red: I_{OUT}, 1 A / div., 2 ms / div.
$V_{OUT(MAX)}$ = 4.93 V.

Figure 24 – V_{IN} = 230 VAC, No Load.
C2 Green: V_{OUT}, 1 V / div., 2 ms / div.
C4 Red: I_{OUT}, 1 A / div., 2 ms / div.
$V_{OUT(MAX)}$ = 5.12 V

Figure 25 – V_{IN} = 230 VAC, Full Load.
C2 Green: V_{OUT}, 1 V / div., 2 ms / div.
C4 Red: I_{OUT}, 1 A / div., 2 ms / div.
$V_{OUT(MAX)}$ = 5.01 V

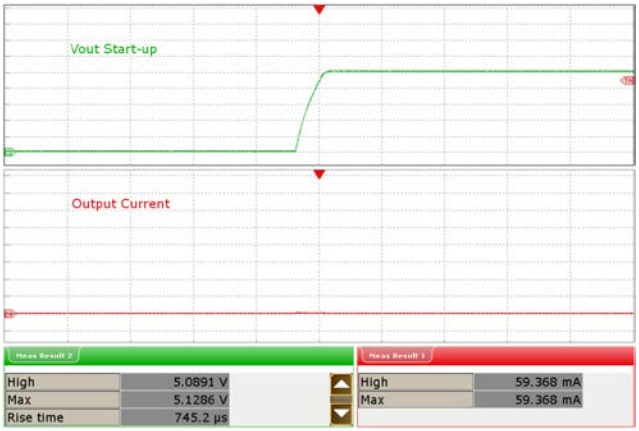

Figure 26 – V_{IN} = 265 VAC, No-Load.
C2 Green: V_{OUT}, 1 V / div., 2 ms / div.
C4 Red: I_{OUT}, 1 A / div., 2 ms / div.
$V_{OUT(MAX)}$ = 5.12 V.

Figure 27 – V_{IN} = 265 VAC, Full Load.
C2 Green: V_{OUT}, 1 V / div., 2 ms / div.
C4 Red: I_{OUT}, 1 A / div., 2 ms / div.
$V_{OUT(MAX)}$ = 5.01 V.

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12.2 *Drain-Source Voltage Waveform*

12.2.1 Normal Operation, Full Load

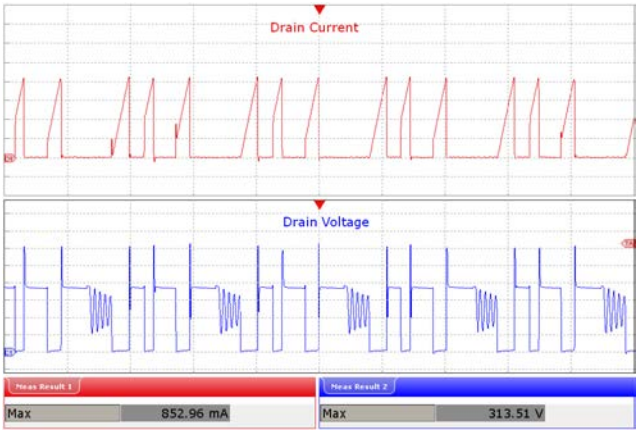

Figure 28 – V_{IN} = 85 VAC.
C4 Red: I_{DS}, 200 mA / div., 20 µs / div.
C1 Blue: V_{DS}, 50 V / div., 20 µs / div.
$V_{DS(MAX)}$ = 313 V.

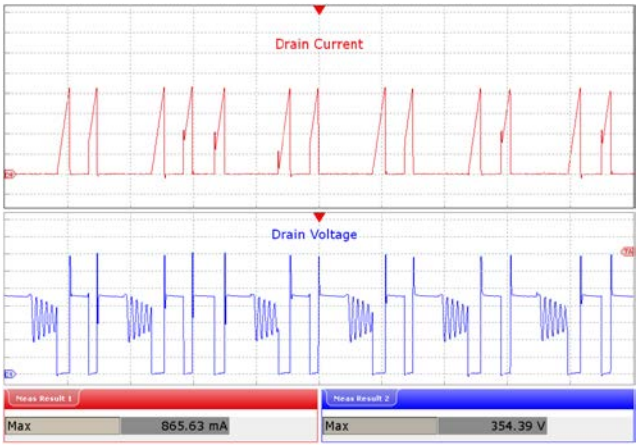

Figure 29 – V_{IN} = 115 VAC.
C4 Red: I_{DS}, 200 mA / div., 20 µs / div.
C1 Blue: V_{DS}, 50 V / div., 20 µs / div.
$V_{DS(MAX)}$ = 354.39 V.

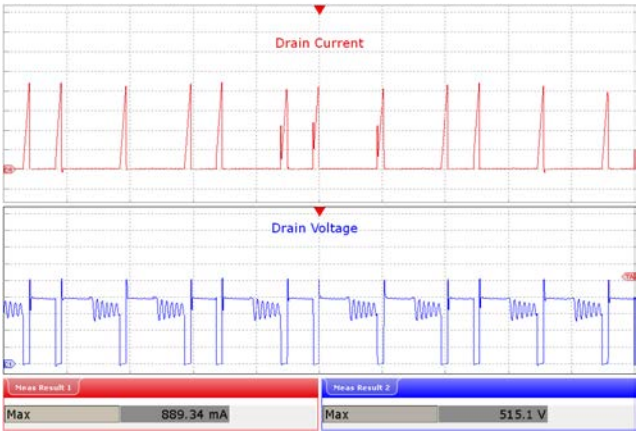

Figure 30 – V_{IN} = 230 VAC.
C4 Red: I_{DS}, 200 mA / div., 20 µs / div.
C1 Blue: V_{DS}, 100V / div., 20 µs / div.
$V_{DS(MAX)}$ = 515 V.

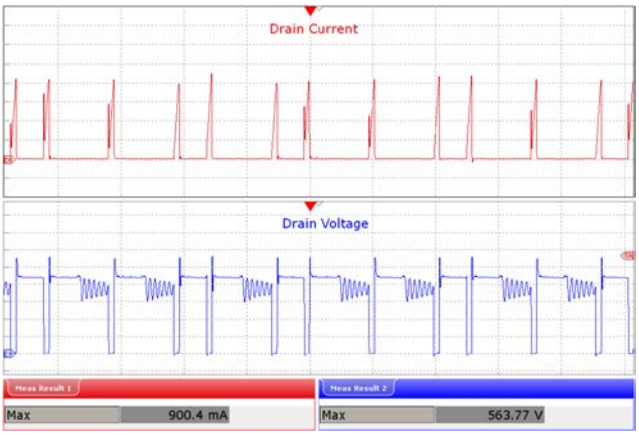

Figure 31 – V_{IN} = 265 VAC.
C4 Red: I_{DS}, 200 mA / div., 20 µs / div.
C1 Blue: V_{DS}, 100 V / div., 20 µs / div.
$V_{DS(MAX)}$ = 564 V.

12.2.2 Start-up Operation, Full Load

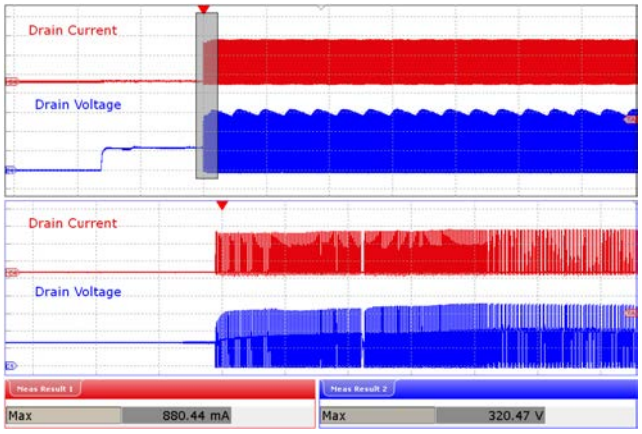

Figure 32 – V_{IN} = 85 VAC.
C4 Top Red: I_{DS}, 400 mA / div., 20 ms / div.
C1 Top Blue: V_{DS}, 100V / div., 20 ms / div.
$V_{DS(MAX)}$ = 320 V.

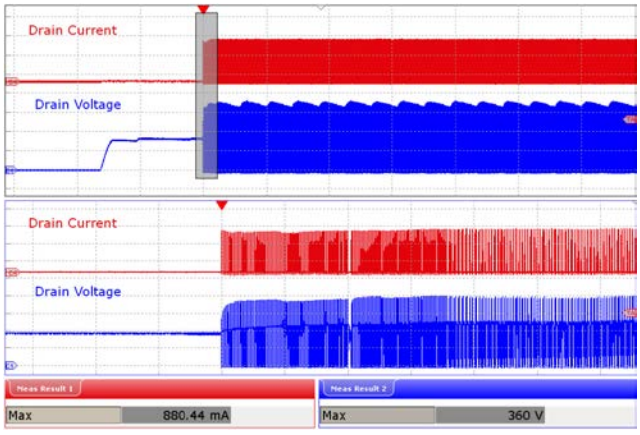

Figure 33 – V_{IN} = 115 VAC.
C4 Top Red: I_{DS}, 400 mA / div., 20 ms / div.
C1 Top Blue: V_{DS}, 100 V / div., 20 ms / div.
$V_{DS(MAX)}$ = 360 V.

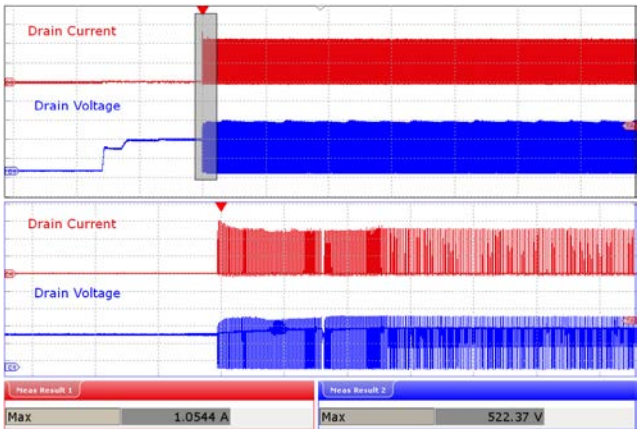

Figure 34 – V_{IN} = 230 VAC.
C4 Top Red: I_{DS}, 400 mA / div., 20 ms / div.
C1 Top Blue: V_{DS}, 200 V / div., 20 ms / div.
$V_{DS(MAX)}$ = 522 V.

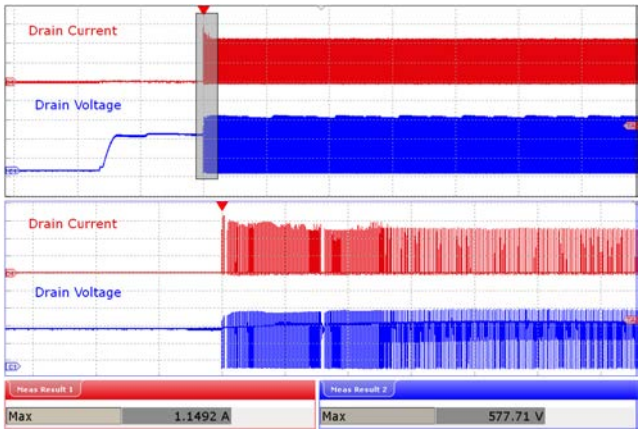

Figure 35 – V_{IN} = 265 VAC.
C4 Top Red: I_{DS}, 400 mA / div., 20 ms / div.
C1 Top Blue: V_{DS}, 200 V / div., 20 ms / div.
$V_{DS(MAX)}$ = 578 V.

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12.3 *0% -100% Load Transient Response*

All measurements are taken at the end of the 100 mΩ cable. Load transition from 3 A for 1 ms to 0 A for 1 ms; at a slew rate of 100 mA / µs

Figure 36 – V_{IN} = 85 VAC, V_{OUT} Waveform.
C2 Green: V_{OUT}, 1 V / div., 2 ms / div.
C4 Red: I_{OUT}, 500 mA / div., 2 ms / div.
$V_{OUT(MAX)}$ = 5.44 V.
$V_{OUT(MIN)}$ = 4.56 V.

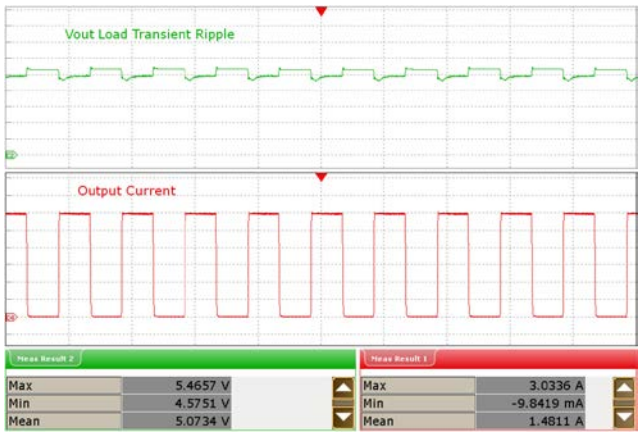

Figure 37 – V_{IN} = 115 VAC, V_{OUT} Waveform.
C2 Green: V_{OUT}, 1 V / div., 2 ms / div.
C4 Red: I_{OUT}, 500 mA / div., 2 ms / div.
$V_{OUT(MAX)}$ = 5.47 V.
$V_{OUT(MIN)}$ = 4.57 V.

Figure 38 – V_{IN} = 230 VAC, V_{OUT} Waveform.
C2 Green: V_{OUT}, 1 V / div., 2 ms / div.
C4 Red: I_{OUT}, 500 mA / div., 2 ms / div.
$V_{OUT(MAX)}$ = 5.49 V.
$V_{OUT(MIN)}$ = 4.61 V.

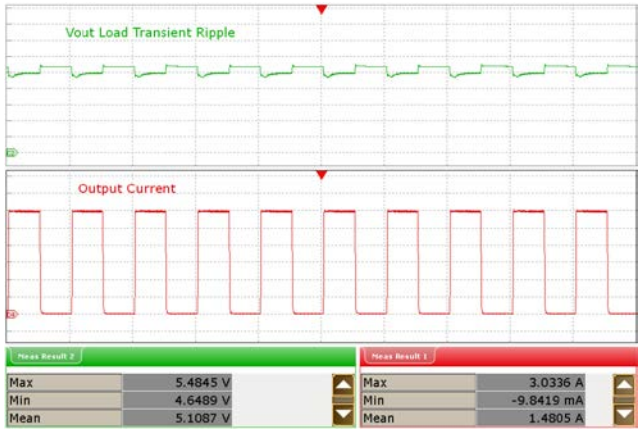

Figure 39 – V_{IN} = 265 VAC, V_{OUT} Waveform.
C2 Green: V_{OUT}, 1 V / div., 2 ms / div.
C4 Red: I_{OUT}, 500 mA / div., 2 ms / div.
$V_{OUT(MAX)}$ = 5.48 V.
$V_{OUT(MIN)}$ = 4.65 V.

12.4 *SRFET Drain-Source Voltage Waveform*

12.4.1.1 Normal Operation, Full Load

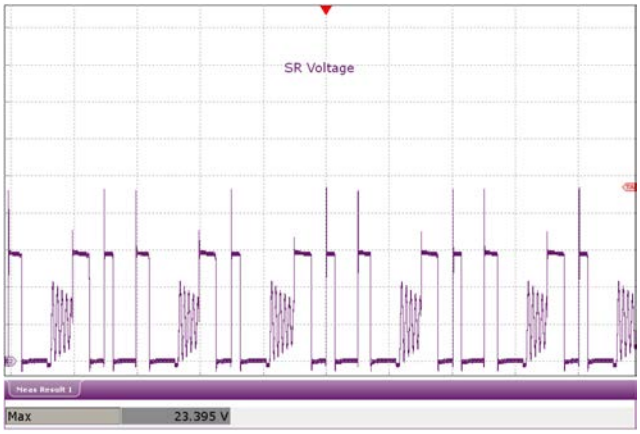

Figure 40 – V_{IN} = 85 VAC.
C2 Violet: V_{SRFET}, 5 V / div., 20 μs / div.
$V_{DS(MAX)}$ = 23.4 V.

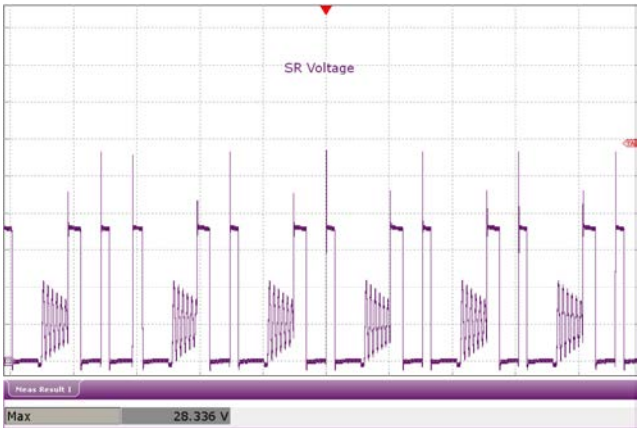

Figure 41 – V_{IN} = 115 VAC.
C2 Violet: V_{SRFET}, 5 V / div., 20 μs / div.
$V_{DS(MAX)}$ = 28 V.

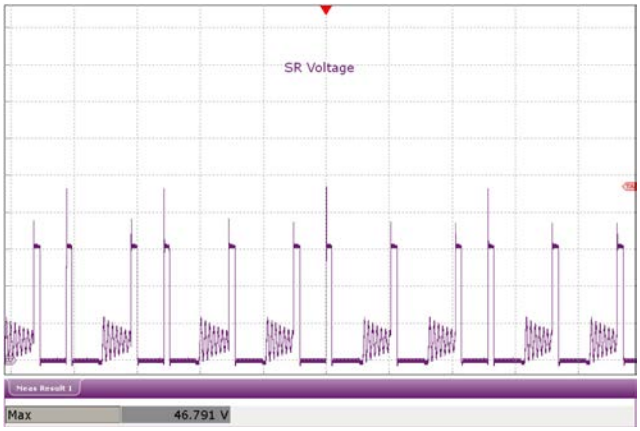

Figure 42 – V_{IN} = 230 VAC.
C2 Violet: V_{SRFET}, 5 V / div., 20 μs / div.
$V_{DS(MAX)}$ = 47 V.

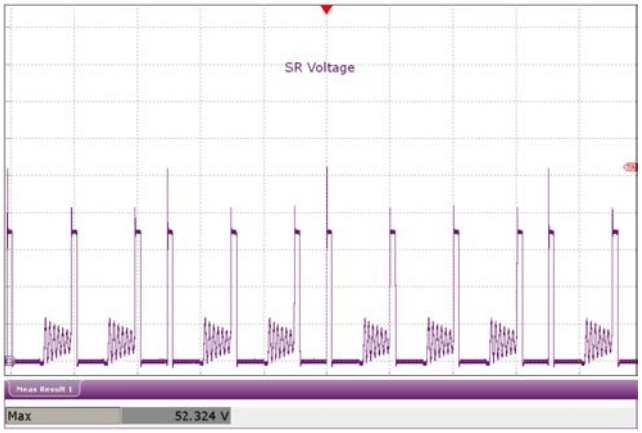

Figure 43 – V_{IN} = 265 VAC.
C2 Violet: V_{SRFET}, 5 V / div., 20 μs / div.
$V_{DS(MAX)}$ = 52 V.

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12.5 *Output Ripple Measurements*

12.5.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 47 μF/50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

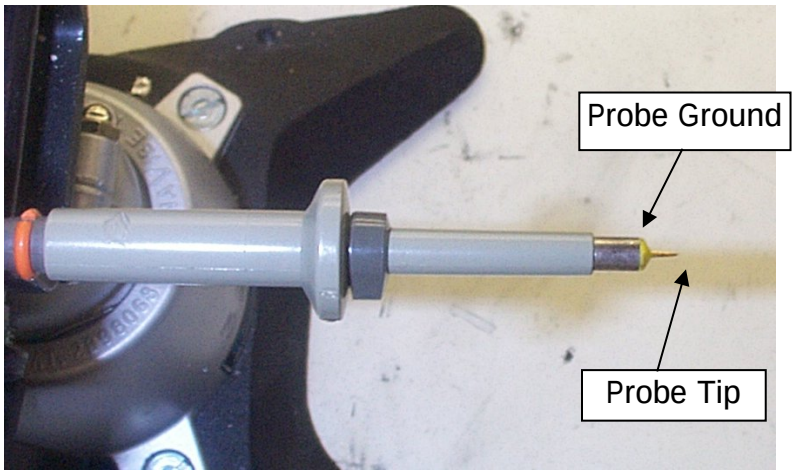

Figure 44 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed.)

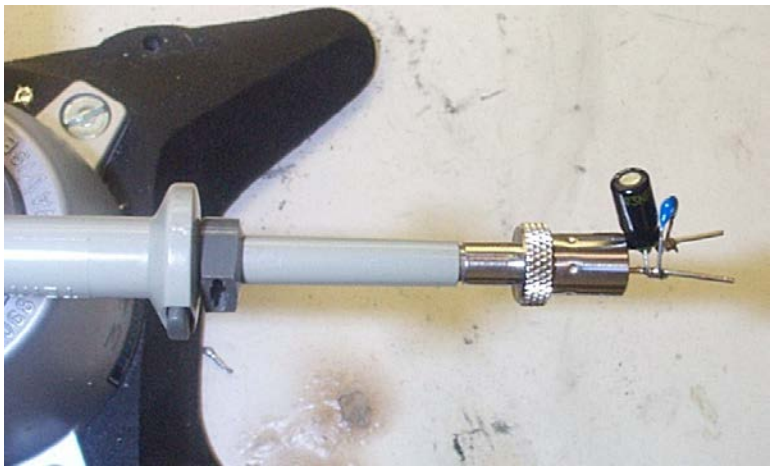

Figure 45 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added.)

12.5.2 Ripple Voltage Waveforms

All measurements are taken at the E-load end using a barrel probe with decoupling capacitors 47 μF electrolytic capacitor and 100 nF ceramic capacitor.

Figure 46 – V_{IN} = 85 V, I_{OUT} = 3 A.
C2 Violet: V_{OUT}, 20 mV / div., 5 ms / div.
Oscilloscope Settings: 20 MHz BW, Peak-Detect Acquisition, AC coupling.
V_{PK-PK} = 81.42 mV.

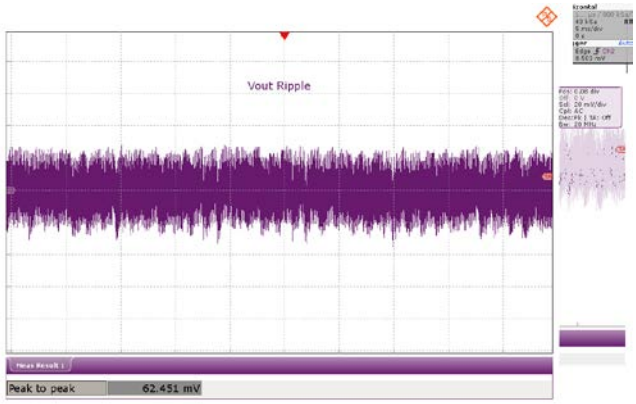

Figure 47 – V_{IN} = 115 V, I_{OUT} = 3 A.
C2 Violet: V_{OUT}, 20 mV / div., 5 ms / div.
Oscilloscope Settings: 20 MHz BW, Peak-Detect Acquisition, AC Coupling.
V_{PK-PK} = 62.45 mV.

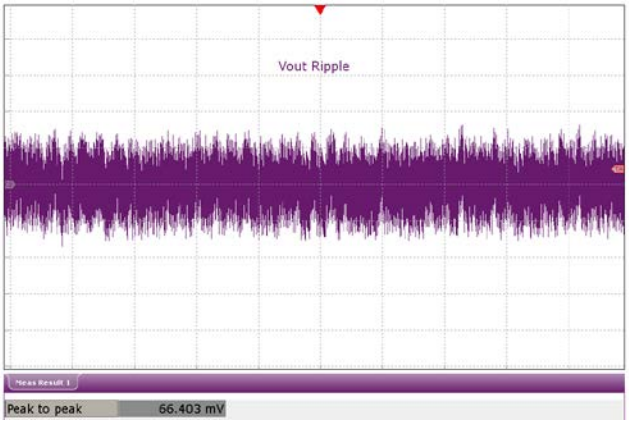

Figure 48 – V_{IN} = 230 V, I_{OUT} = 3 A.
C2 Violet: V_{OUT}, 20 mV / div., 5 ms / div.
Oscilloscope Settings: 20 MHz BW, Peak-Detect Acquisition, AC Coupling.
V_{PK-PK} = 66.4 mV.

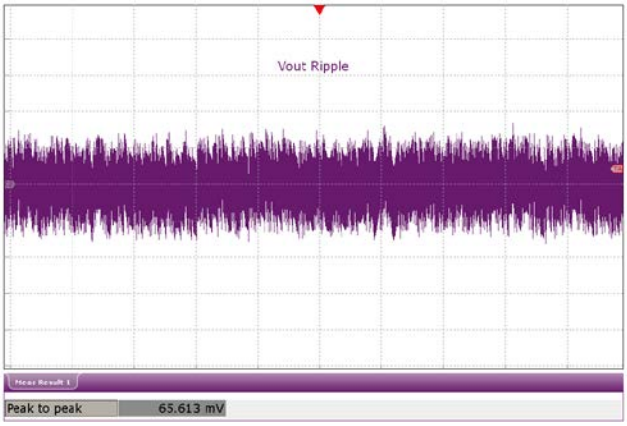

Figure 49 – V_{IN} = 265 V, I_{OUT} = 3 A.
C2 Violet: V_{OUT}, 20 mV / div., 5 ms / div.
Oscilloscope Settings: 20 MHz BW, Peak-Detect Acquisition, AC Coupling.
V_{PK-PK} = 65.6 mV.

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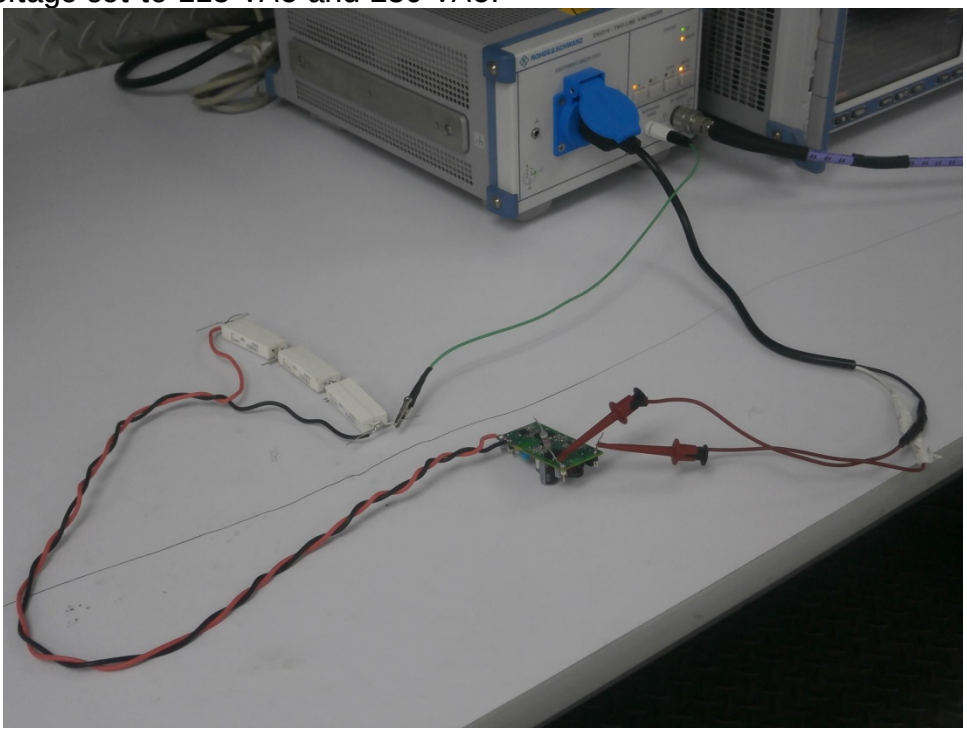
13 **EMI Performance**

13.1 *EMI Test Set-up*

13.2 *Equipment and Load Used and Test Condition*

1) Rohde & Schwarz ENV216 two line V-network.
2) Rohde & Schwarz ESRP EMI test receiver.
3) HIOKI 3322 Power HiTester.
4) Chroma measurement test fixture.
5) Resistor load (1.5 Ω) to cater approx. ≈15 W full load power.
6) Input voltage set to 115 VAC and 230 VAC.



13.2.1.1 230 VAC Input

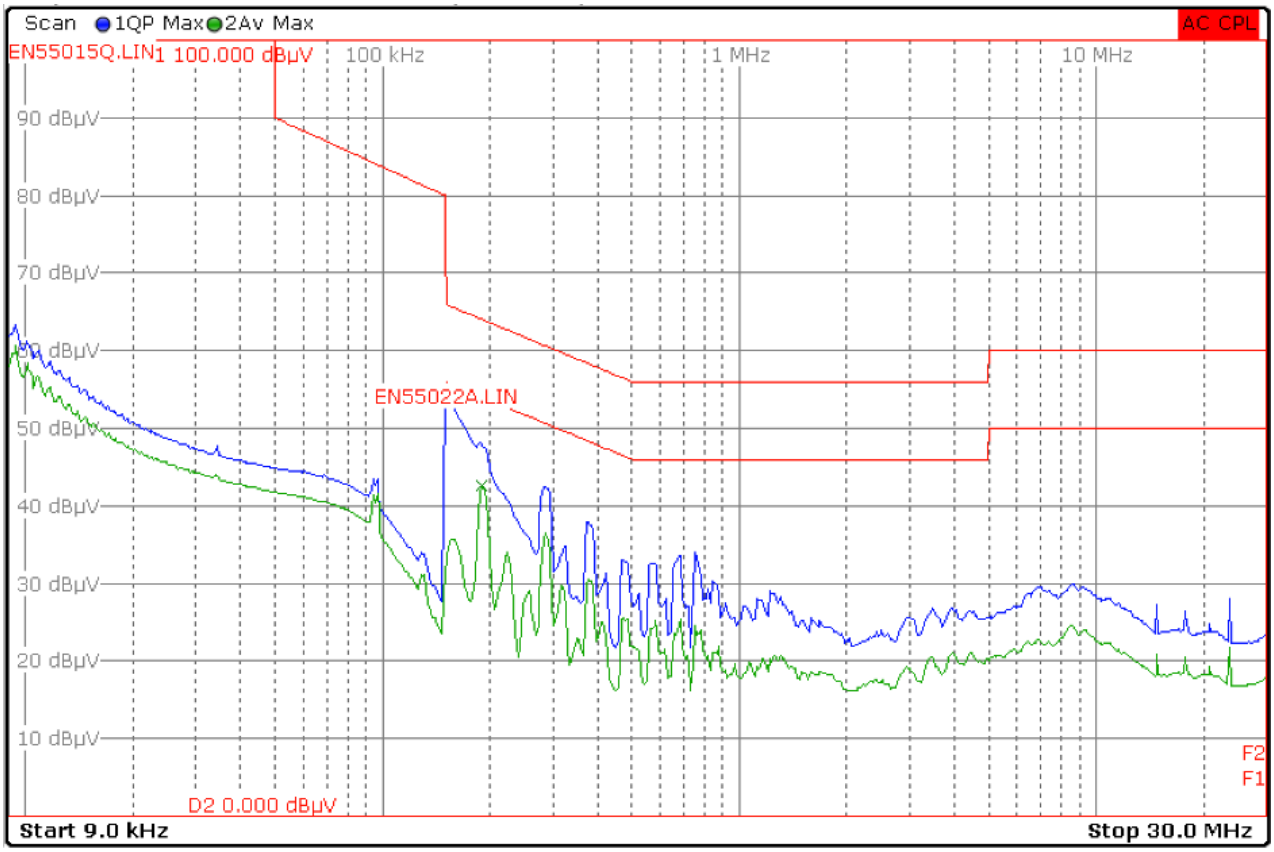


Figure 50 – Output Not Connected to the Artificial Hand or Ground of the LISN.

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13.2.1.2 230 VAC Input

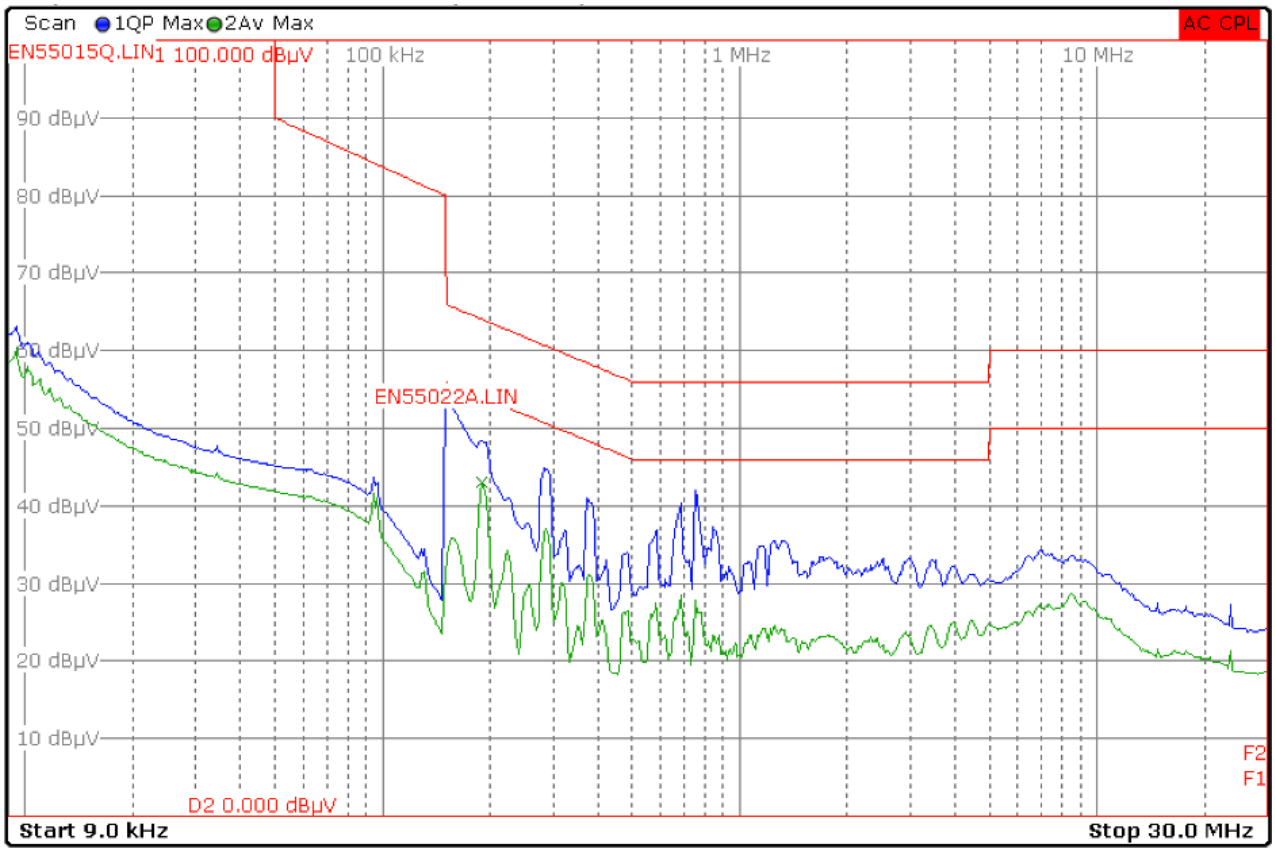

Figure 51 – Output Connected to the Artificial Hand of the LISN.

13.2.1.3 230 VAC Input

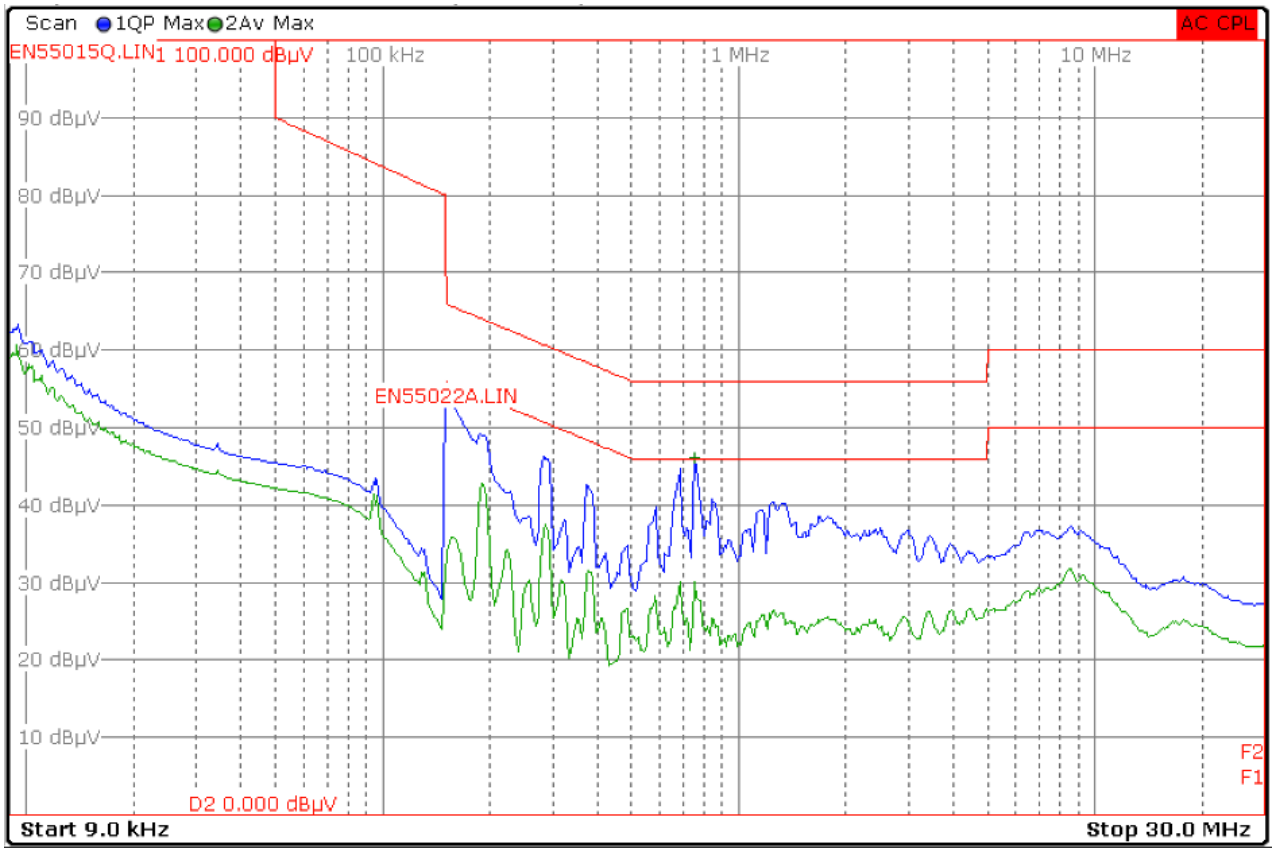

Figure 52 – Output Connected to the Ground of the LISN.

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13.2.1.4 115 VAC Input

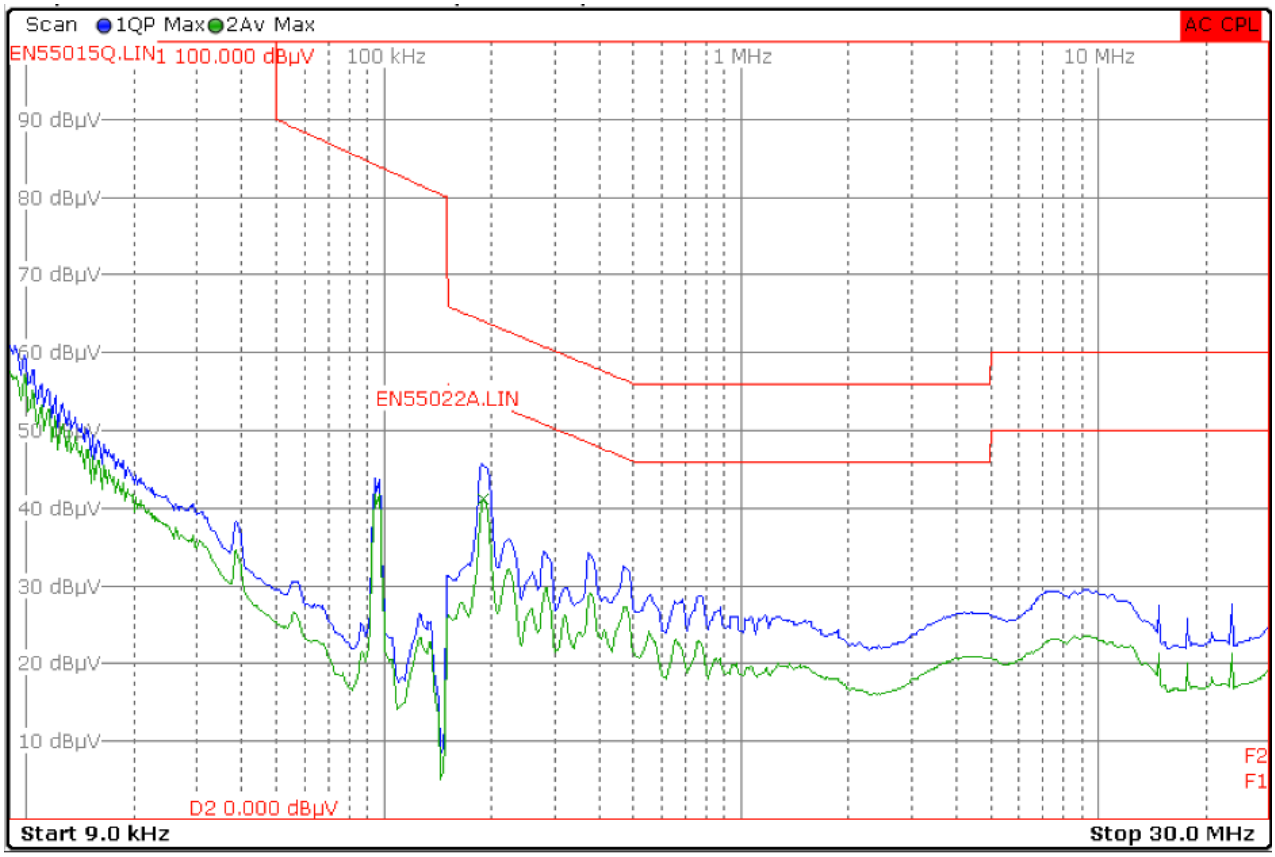

Figure 53 – Output Not Connected to the Artificial Hand or Ground of the LISN.

13.2.1.5 115 VAC Input

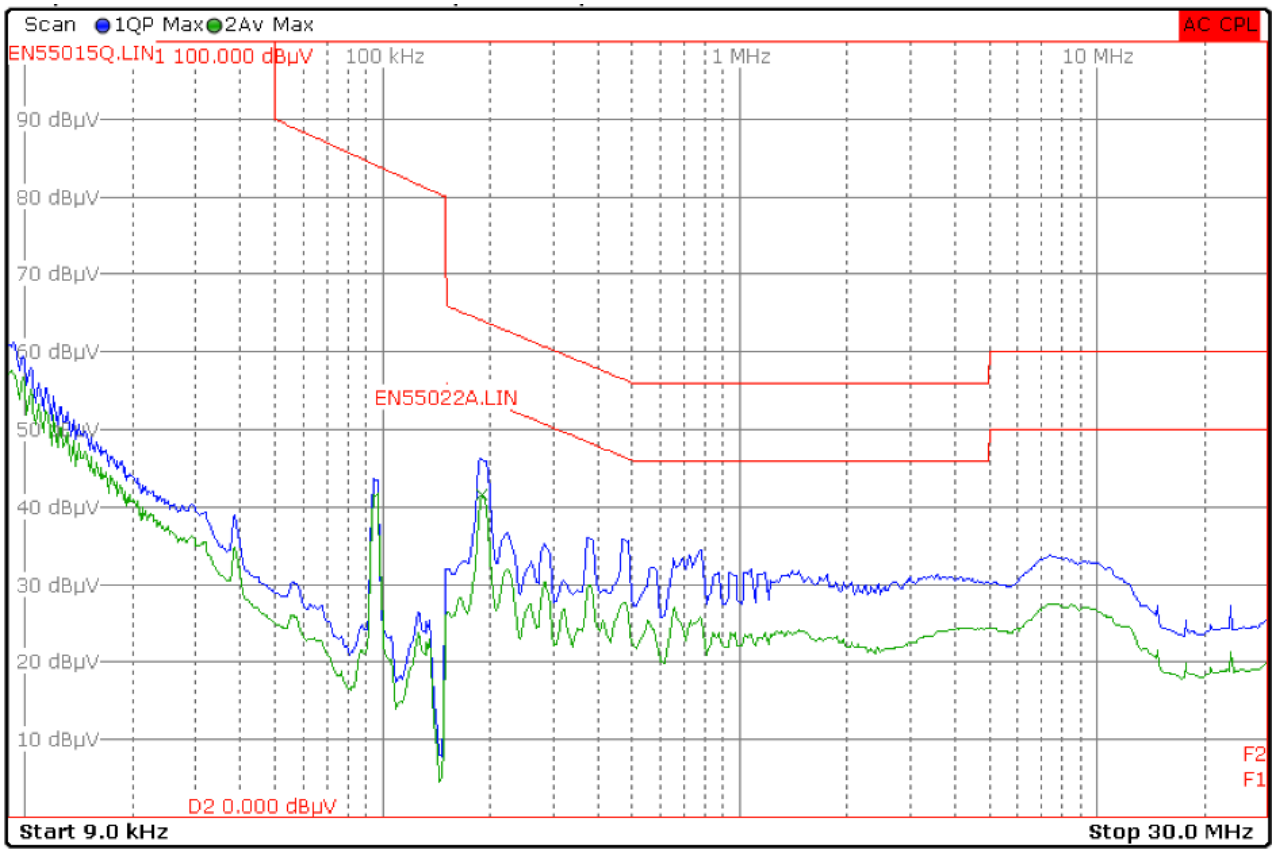

Figure 54 – Output Connected to the Artificial Hand of the LISN.

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13.2.1.6 115 VAC Input

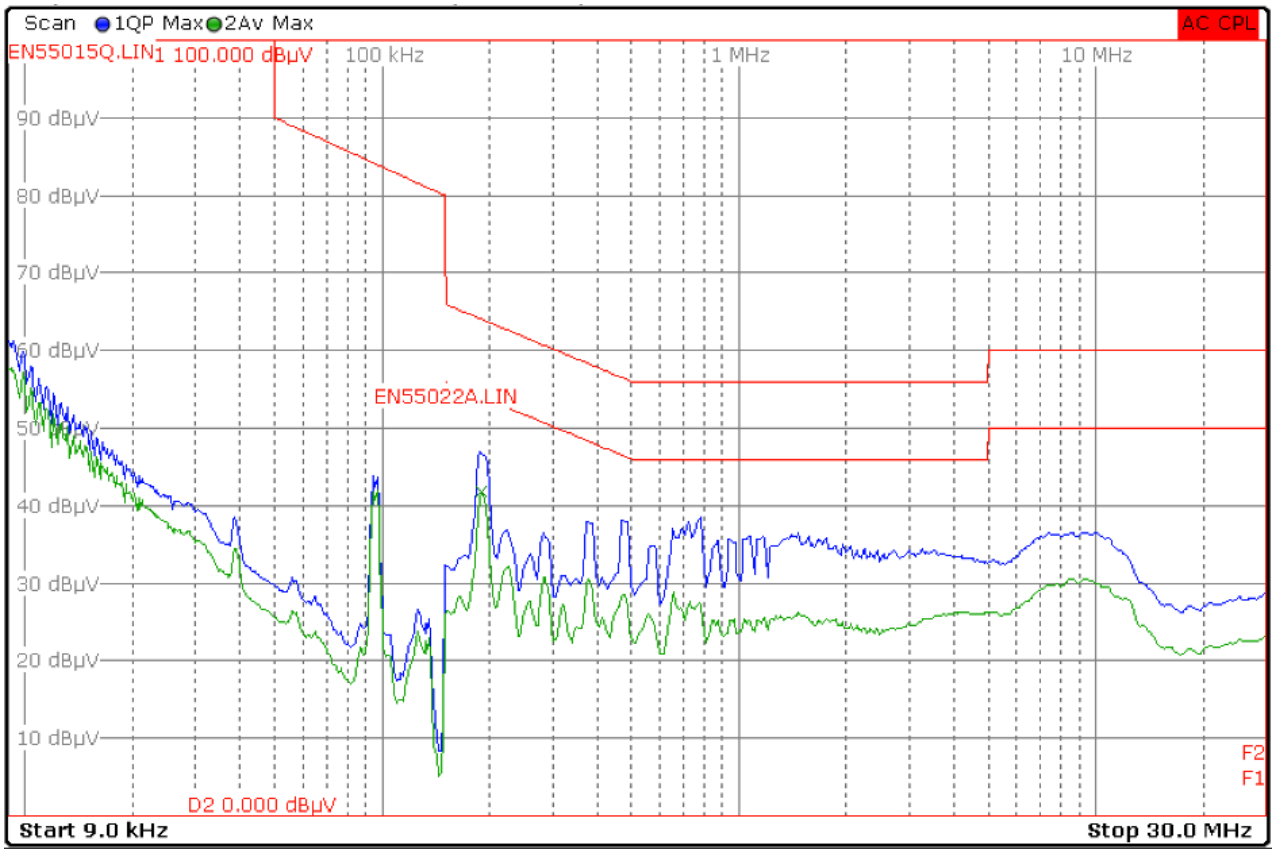


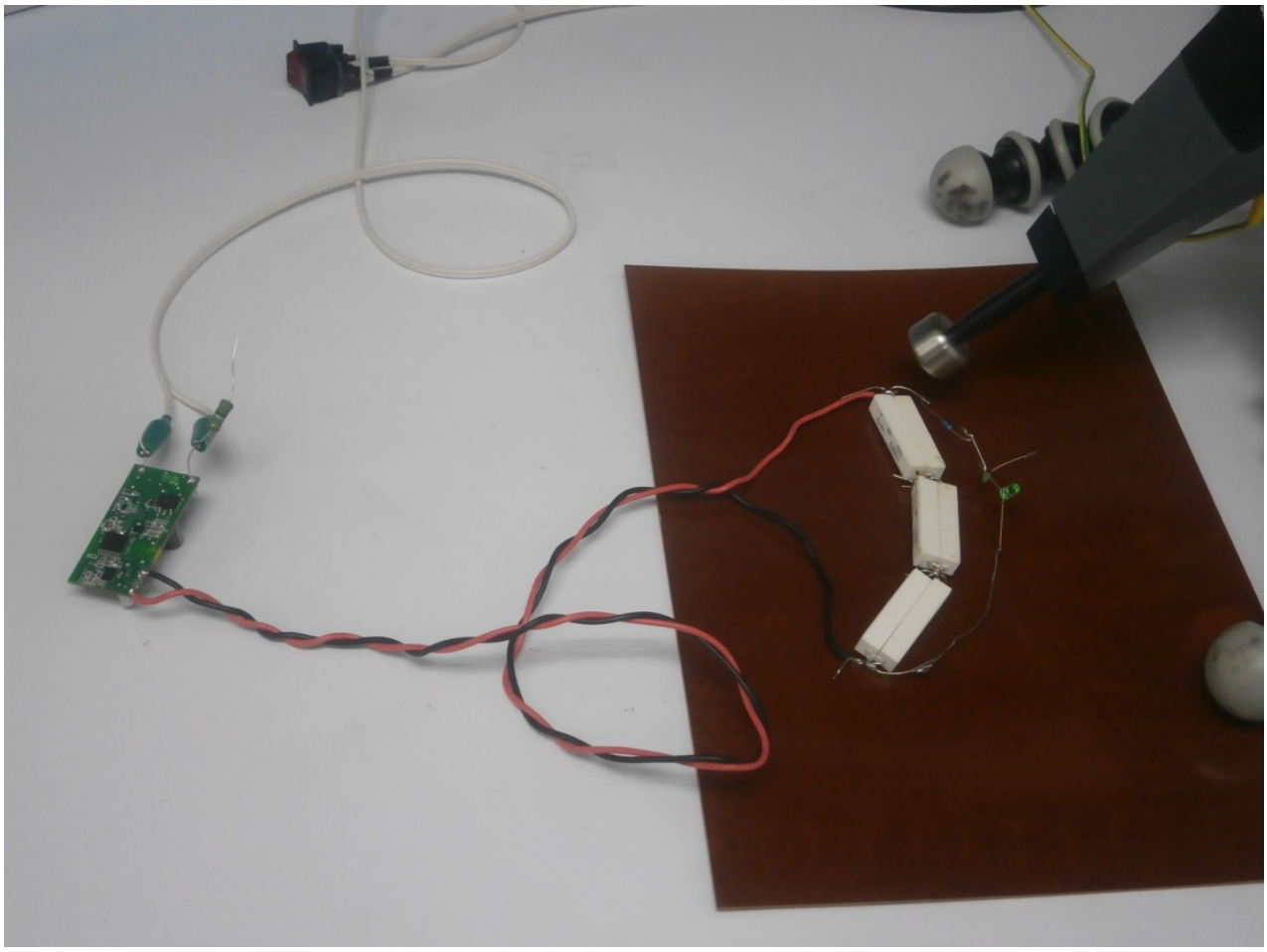
Figure 55 – Output Connected to the Ground of the LISN.

14 **ESD**

14.1 *ESD Test (Set-up)*

14.1.1 Equipment Used and Test Condition

1. Used EMTEST ESD equipment for the testing.
2. Line input is set at 230 VAC.
3. Total output power is 15 W using a resistive load of 1.5 Ω.
4. Contact discharge test is set at ±8 kV for both the positive and negative rail of the 5 V output.
5. Air discharge test is set at ±16.5 kV for both the positive and negative rail of the 5 V output.



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Level (V)	Input Voltage (VAC)	Discharge	Number of Discharge	Test Result (Pass/Fail)
8800	230	Contact	10	Pass
16500	230	Air	10	Pass

Level (V)	Input Voltage (VAC)	Discharge	Number of Discharge	Test Result (Pass/Fail)
-8800	230	Contact	10	Pass
-16500	230	Air	10	Pass

14.2 *Ring Wave Common Mode Surge Test*

Voltage	Angle	IEC Coupling	Impedance	# of Strikes	P/F
+6 kV	0	L→P.E.	12 Ω	10	P
+6 kV	0	N→P.E.	12 Ω	10	P
+6 kV	0	L, N→P.E.	12 Ω	10	P
-6 kV	0	L→P.E.	12 Ω	10	P
-6 kV	0	N→P.E.	12 Ω	10	P
-6 kV	0	L, N→P.E.	12 Ω	10	P
+6 kV	90	L→P.E.	12 Ω	10	P
+6 kV	90	N→P.E.	12 Ω	10	P
+6 kV	90	L, N→P.E.	12 Ω	10	P
-6 kV	90	L→P.E.	12 Ω	10	P
-6 kV	90	N→P.E.	12 Ω	10	P
-6 kV	90	L,N→P.E.	12 Ω	10	P
+6 kV	180	L→P.E.	12 Ω	10	P
+6 kV	180	N→P.E.	12 Ω	10	P
+6 kV	180	L, N→P.E.	12 Ω	10	P
-6 kV	180	L→P.E.	12 Ω	10	P
-6 kV	180	N→P.E.	12 Ω	10	P
-6 kV	180	L, N→P.E.	12 Ω	10	P
+6 kV	270	L→P.E.	12 Ω	10	P
+6 kV	270	N→P.E.	12 Ω	10	P
+6 kV	270	L, N→P.E.	12 Ω	10	P
-6 kV	270	L→P.E.	12 Ω	10	P
-6 kV	270	N→P.E.	12 Ω	10	P
-6 kV	270	L, N→P.E.	12 Ω	10	P

15 Revision History

Date	Author	Revision	Description & Changes	Reviewed
22-Mar-16	DK	1.0	Initial Release	Apps & Mktg
9-Mar-16	AP	1.1	Updated PIXIs and minor edits	
29-Mar-16	RJ	1.2	Updated summary	
15-Aug-16	KM	1.2	Updated Schematic.	

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