Design Example Report

Title	***65 W Dual USB-C Shared Capacity Ports with Current Sharing Using InnoSwitch™3-Pro PowiGaN™ INN3370C-H302***
Specification	100 VAC – 132 VAC Input; 65 W Power Limited Single Port: 5 V / 3 A, 9 V / 3 A, ,12 V / 3 A, 15 V / 3 A, 20 V / 3.25 A Dual Port, Port 1: 5 V / 3 A, 9 V / 3 A, 12 V / 3 A, 15 V / 3 A, 20 V / 2.25 A Dual Port, Port 2: 5 V / 3 A, 9 V / 2.22 A, 12 V / 1.66 A, 15 V / 1.33 A 20 V / 1 A[1]
Application	Wall Outlet, Power Strip and Surge Protectors
Author	Applications Engineering Department
Document Number	DER-916
Date	November 3, 2021
Revision	1.0

Summary and Features

- InnoSwitch3-Pro - digitally controllable CV/CC QR flyback switcher IC with integrated high-voltage MOSFET, synchronous rectification and FluxLink™ feedback
  - I²C Interface enables low pin count USB PD controller (8 pin)
  - Sophisticated telemetry and comprehensive protection features
- Dual Type-C USB PD 3.0 shared capacity ports using IP2726 USB PD controller
- 65 W available on both Type-C ports

[1] Port designation depends on loading order. See the table on page 6 for details.

Power Integrations
5245 Hellyer Avenue, San Jose, CA 95138 USA.
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.power.com

- 5/9/12/15/20 V supported on both ports, no dc/dc converters
- >92% end to end efficiency at full load
- Meets DOE6 and CoC v5 2016 efficiency requirement (>1% efficiency margin)
- Maximum component temperature <110 ºC at 50 ºC ambient temperature operation
- Output overvoltage and overcurrent protection
- Integrated thermal protection
- Compact size 2.36” x 1.57” x 0.8”

PATENT INFORMATION

Table of Contents

Important Note:

Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This document is an engineering report describing a 65 W Dual USB PD 3.0 power supply using InnoSwitch3-Pro INN3370-H302 IC and Injoinic IP2726 USB PD controller. The USB PD source capabilities of the power supply are listed below.

Single Port Mode:

- 5 V / 3 A (Fixed Supply PDO)
- 9 V / 3 A (Fixed Supply PDO)
- 12 V / 3 A (Fixed Supply PDO)
- 15 V / 3 A (Fixed Supply PDO)
- 20 V / 3.25 A (Fixed Supply PDO)

Dual Port Mode (Power Limited to 65 W):

Port 1:

- 5 V / 3 A (Fixed Supply PDO)
- 9 V / 3 A (Fixed Supply PDO)
- 12 V / 3 A (Fixed Supply PDO)
- 15 V / 3 A (Fixed Supply PDO)
- 20 V / 2.25 A (Fixed Supply PDO)

Port 2:

- 5 V / 3 A (Fixed Supply PDO)
- 9 V / 2.22 A (Fixed Supply PDO)
- 12 V / 1.66 A (Fixed Supply PDO)
- 15 V / 1.33 A (Fixed Supply PDO)
- 20 V / 1 A (Fixed Supply PDO)

Operation of the power supply is described in the table below.

Operating Mode	USB Port 1 Max power	USB Port 2 Max Power	Description
Single Port Operation	65 W	Unused	Output of both flyback converters combine to supply Port 1 Both power supplies provide 32.5 W and in parallel
Single Port Operation	Unused	65 W	Output of both flyback converters combine to supply Port 2 Both power supplies provide 32.5 W and in parallel
Port 1 in use, Port 2 load inserted	45 W	20 W	Port 1 starts at 65 W maximum power then drop to 45 W Port 2 maximum will be 20 W Ports operate independently
Port 2 in use, Port 1 load inserted	20 W	45 W	Port 2 starts at 65 W maximum power then drop to 45 W Port 1 maximum will be 20 W Ports operate independently

This design shows the high power density and efficiency that is possible due to the high level of integration of the InnoSwitch3-Pro controller providing exceptional performance.

The report contains the power supply specification, schematic diagrams, PCB layouts, bill of materials (BOM), magnetics design, and performance data.

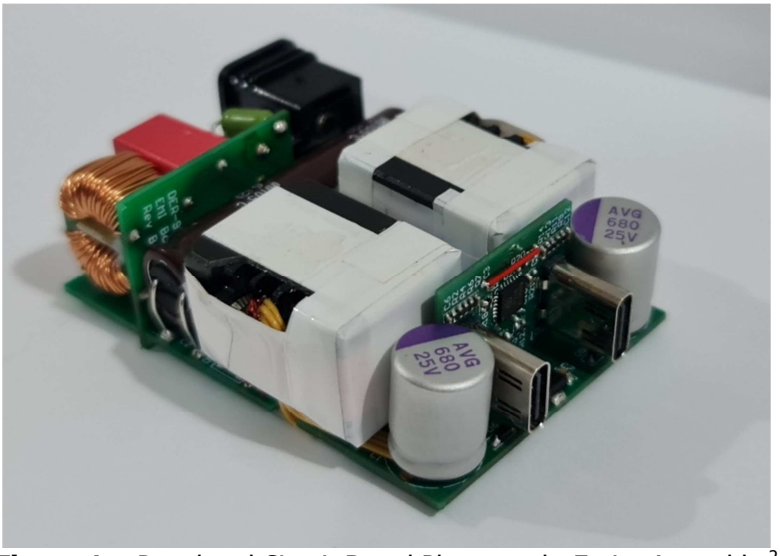


Figure 1 – Populated Circuit Board Photograph, Entire Assembly.[2]

[2] EMI Board used here is labelled Rev B. Rev C and Rev B EMI boards are identical. Latest EMI boards are labelled Rev C to match Main Board revision letter.

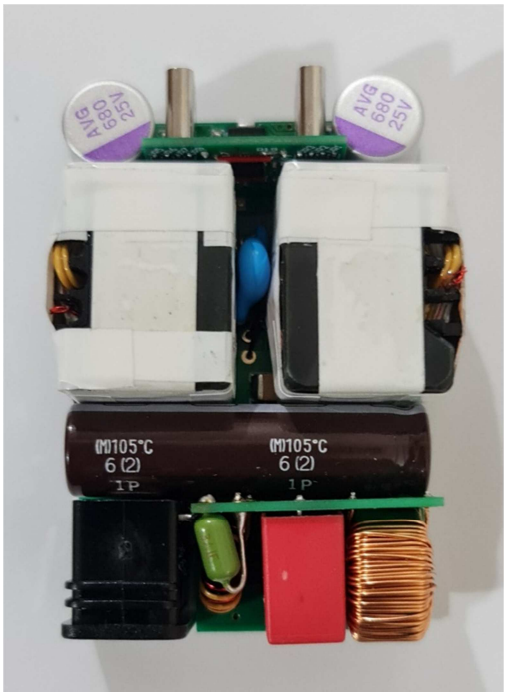


Figure 2 – Populated Circuit Board Photograph - Top.

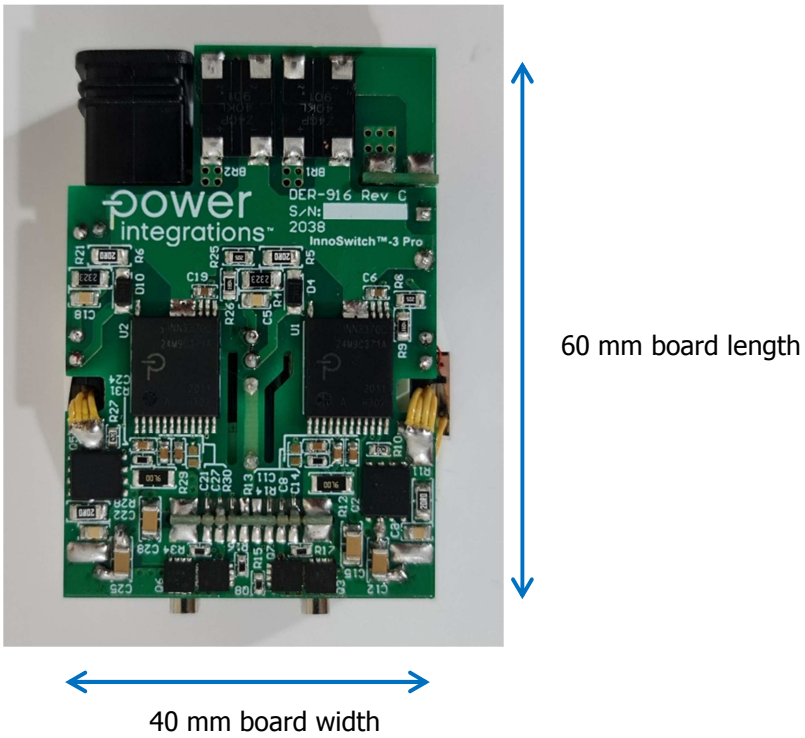


Figure 3 – Populated Circuit Board Photograph - Bottom.

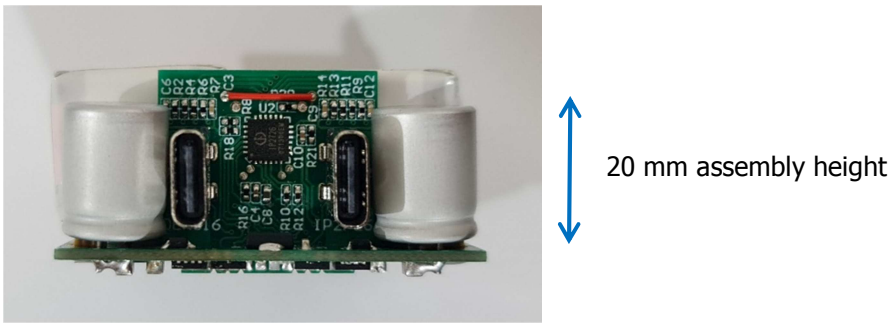


Figure 4 – Populated Circuit Board Photograph - Front.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	100		132	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	56	60	64	Hz	
No-load Input Power				200	mW	Measured at 115 VAC.
5 V / 3 A Setting						
Output Voltage	$V_{OUT(5\ V)}$		5.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE(5\ V)}$			150	mV	Measured at End of 100 mΩ Cable.
Output Current	$I_{OUT(5\ V)}$			3.0	A	±3%
Average Efficiency	$\eta_{(5\ V)}$		91		%	Measured at 115 VAC from AC Receptacle to Type-C Receptacle on the Board.
Continuous Output Power	$P_{OUT(5\ V)}$			15	W	
9 V / 3 A Setting						
Output Voltage	$V_{OUT(9\ V)}$		9.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE(9\ V)}$			150	mV	Measured at End of 100 mΩ Cable.
Output Current	$I_{OUT(9\ V)}$			3.0	A	±3%
Average Efficiency	$\eta_{(9\ V)}$		91		%	Measured at 115 VAC from AC Receptacle to Type-C Receptacle on the Board.
Continuous Output Power	$P_{OUT(9\ V)}$			27	W	
12 V / 3 A Setting						
Output Voltage	$V_{OUT(15\ V)}$		12.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE(15\ V)}$			150	mV	Measured at End of 100 mΩ Cable.
Output Current	$I_{OUT(15\ V)}$			3.0	A	±3%
Average Efficiency	$\eta_{(15\ V)}$		91		%	Measured at 115 VAC from AC Receptacle to Type-C Receptacle on the Board.
Continuous Output Power	$P_{OUT(15\ V)}$			36	W	
15 V / 3 A Setting						
Output Voltage	$V_{OUT(20\ V)}$		15.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE(20\ V)}$			150	mV	Measured at End of 100 mΩ Cable.
Output Current	$I_{OUT(20\ V)}$			2.25	A	±3%
Average Efficiency	$\eta_{(20\ V)}$		91		%	Measured at 115 VAC from AC Receptacle to Type-C Receptacle on the Board.
Continuous Output Power	$P_{OUT(20\ V)}$			45	W	
20 V / 3.25 A Setting						
Output Voltage	$V_{OUT(20\ V)}$		20.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE(20\ V)}$			150	mV	Measured at End of 100 mΩ Cable.
Output Current	$I_{OUT(20\ V)}$			3.25	A	±3%
Average Efficiency	$\eta_{(20\ V)}$		92		%	Measured at 115 VAC from AC Receptacle to Type-C Receptacle on the Board.
Continuous Output Power	$P_{OUT(20\ V)}$			65	W	
Conducted EMI		Meets CISPR22B / EN55022B				
Ambient Temperature	T_{AMB}	0		50	ºC	Open Frame, Sea Level.

Note: To use this design for a charger/adapter with a different shape and form factor, the circuit board layout and heat spreader design would need to be adjusted to meet the target specifications for EMI, ESD, and Line Surge performance.

3 Schematic

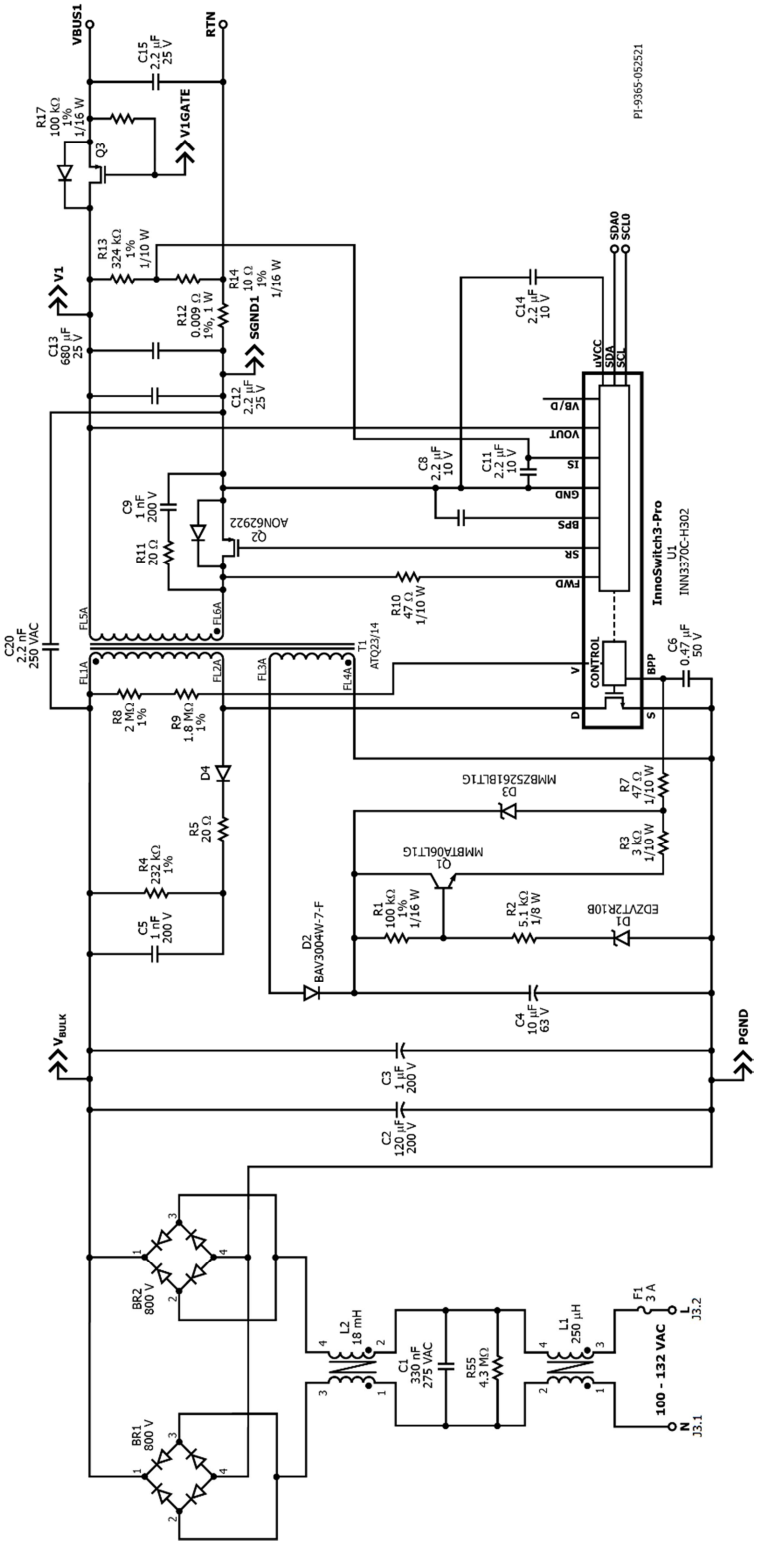


Figure 5 – DER-916 Rev C Schematic, Flyback 1 Power Section.

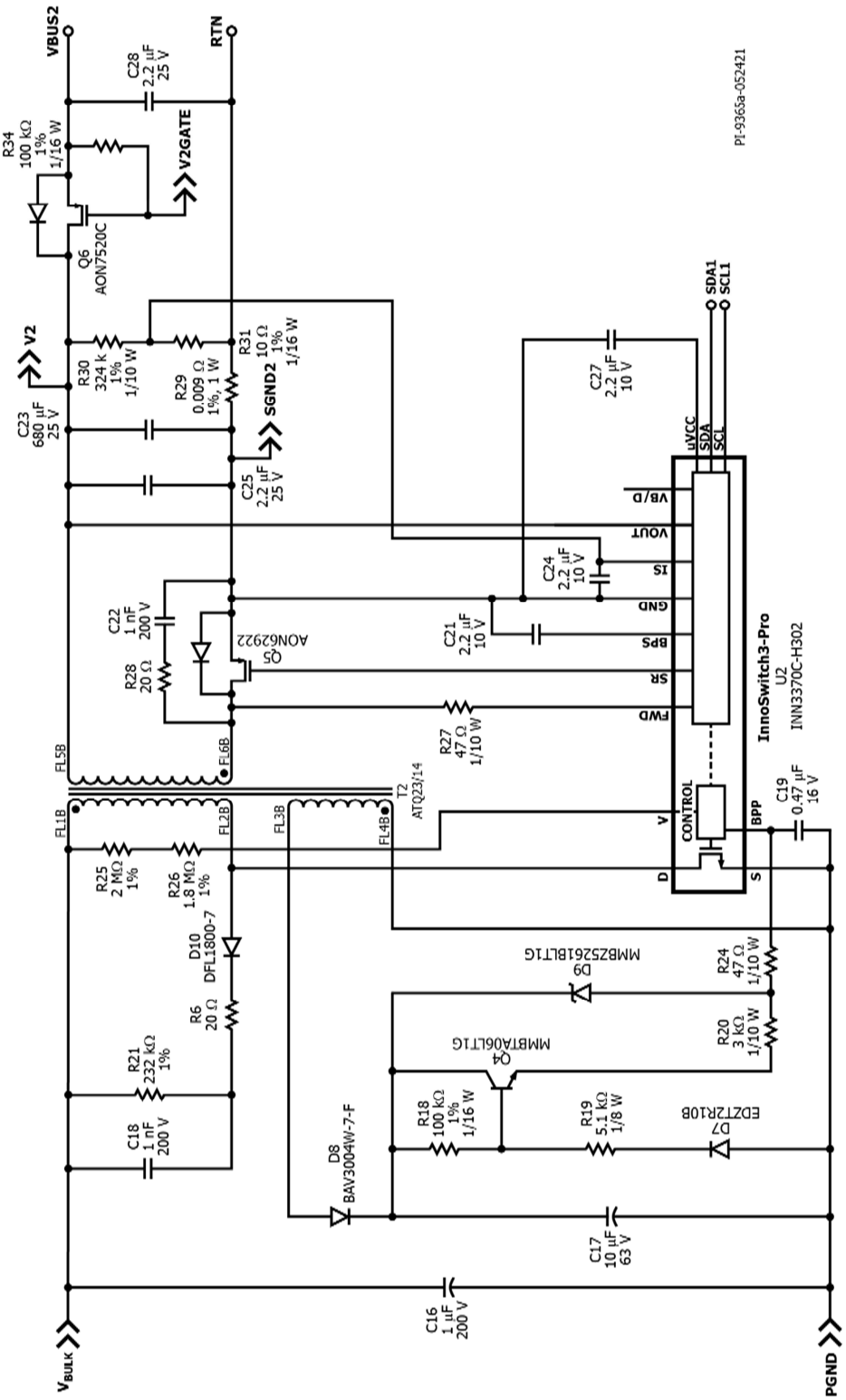


Figure 6 – DER-916 Rev C Schematic, Flyback 2 Power Section.

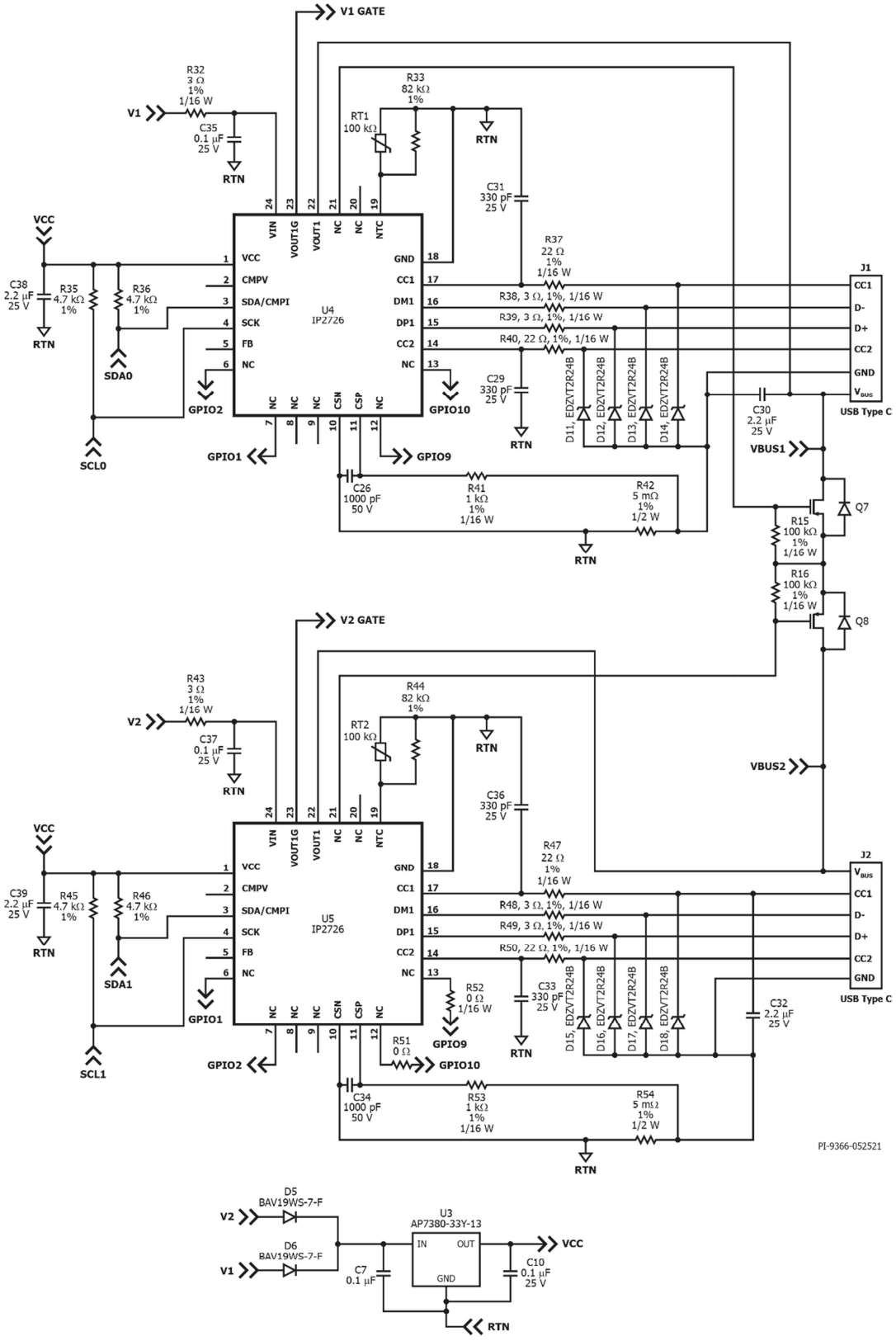


Figure 7. DER-916 Rev C Schematic, USB-PD Controller and Ports

4 Circuit Description

4.1 *Input Rectifier and EMI Filter*

The input fuse F1 isolates the circuit and provides protection from component failure. Common mode chokes L1 and L2, with capacitors C1 and C20 provide common mode and differential mode noise filtering for EMI attenuation. Bridge rectifiers BR1 and BR2 rectify the AC line voltage to have a full wave rectified DC, which is filtered by the bulk capacitor C2.

Resistor R55 discharges capacitor C1 when the power supply is disconnected from AC mains.

4.2 *InnoSwitch3-Pro IC Primary*

This design uses two identical flyback converters that operate independently from each other. The following paragraphs describe only one of the converters but is applicable to the other by cross-referencing the part designators in the schematic.

One end of the flyback transformer T1 primary winding is connected to the rectified DC bus while the other end is connected to the drain terminal of the switch inside the InnoSwitch3-Pro IC U1. Resistors R8 and R9 provide input voltage sensing for AC input undervoltage or overvoltage protection.

A low-cost RCD clamp formed by diode D4, resistors R4 and R5, and capacitor C5 limits the peak drain-source voltage of U1 at the instant the switch inside U1 turns off. The clamp helps to dissipate the energy stored in the leakage reactance of transformer T1.

The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor C6 when the AC is first applied. During normal operation, the primary-side block is powered by the auxiliary winding of transformer T1. The output of the auxiliary (or bias) winding is rectified using diode D2 and filtered using capacitor C4. The NPN BJT Q1, resistors R1 and R2, and Zener diode D1 form a linear regulator to maintain the voltage at the Emitter terminal of Q1 to approximately 9V regardless of the output voltage set point. Resistor R3 limits the BPP pin current of the InnoSwitch3-Pro IC U1 to a value sufficient for normal operation without incurring excessive losses.

Zener diode D3 offers primary sensed output overvoltage protection. In a flyback converter, the output of the auxiliary winding tracks the output voltage of the converter. In case of overvoltage at the output of the converter, the auxiliary winding voltage increases causing VR1 to breakdown resulting in a very low impedance. This will cause excessive current to flow into the BPP pin of InnoSwitch3-Pro IC U1. If the current flowing into the BPP pin increases above the I_{SD} threshold, the InnoSwitch3-Pro controller will latch off to prevent any further increase in output voltage. Resistor R7 limits the current injected to BPP pin when the output overvoltage protection is triggered.

4.3 *InnoSwitch3-Pro IC Secondary and USB Power Delivery Controller*

The secondary-side of the InnoSwitch3-Pro IC provides output voltage and current sensing as well as a gate driver for the synchronous rectification FET (SR FET). The voltage across the transformer secondary winding is rectified by the SR FET Q2 and filtered by capacitors C12 and C13. High frequency ringing during switching transients that would otherwise create radiated EMI is reduced via the RC snubber formed by resistor R11 and capacitor C9.

Switching of Q3 is controlled by the secondary-side controller inside IC U1. Control is based on the secondary winding voltage sensed by the FWD pin via resistor R10.

In continuous conduction mode (CCM) of operation, the SR FET is turned off just prior to the secondary-side commanding a new switching cycle to the primary. In discontinuous mode of operation, the SR FET is turned off when the magnitude of the voltage drop across the SR FET falls below a certain threshold of approximately $V_{SR(TH)}$. Secondary-side control of the primary-side power switch avoids any possibility of cross conduction of the two switches and ensures reliable synchronous rectifier operation.

The secondary-side of the IC is powered either by the secondary winding forward voltage (thru R10 and the FWM pin) or by the output voltage (thru the VOUT pin). Capacitor C8 connected to the BPS pin of InnoSwitch3-Pro IC U2 provides decoupling for the internal circuitry.

Output current is sensed by monitoring the voltage drop across resistor R12. Resistors R13 and R14 add an offset to the sensed output current to provide a positive slope to the CC characteristic. The resulting current measurement is filtered with decoupling capacitor C11 and monitored across the IS and SECONDARY GROUND pins. An internal current sense threshold, programmable up to 32mV thru the I^2C interface, is used to reduce losses. Once the threshold is exceeded, the InnoSwitch3-Pro IC U1 regulates the number of switch pulses to maintain a fixed output current.

During constant current (CC) operation, when the output voltage falls significantly, the secondary-side controller inside InnoSwitch3-Pro IC U1 derives power from the secondary winding directly. During the ON-time of the primary-side power switch, the forward voltage that appears across the secondary winding is used to charge the SECONDARY BYPASS pin decoupling capacitor C8 via resistor R10 and an internal regulator. This allows output current regulation to be maintained down to the minimum UV threshold. Below this threshold, the unit enters auto-restart until the output load is reduced.

When the output current is below the CC threshold, the converter operates in constant voltage mode. The output voltage is monitored by the VOUT pin of the InnoSwitch3-Pro IC. Similar with current regulation, the output voltage is also compared to an internal

voltage reference that is set via the I^2C interface. Capacitor C12 is placed directly across the VOUT pin and the SECONDARY GROUND pin for ESD protection of the VOUT pin.

N-channel MOSFET Q3 is the bus switch used to connect or disconnect the output of the flyback converter to the USB Type-C port V_{BUS} pin. MOSFET Q3 is controlled by the USB-PD controller IC. Resistor R17 is a pulldown resistor to prevent unwanted triggering of Q3 and while also acting as a discharge path for the bus voltage when the Q3 is turned off. Capacitor C15 is used at the output for ESD protection.

In this design, a couple of IP2726 (U4, U5) ICs are used as the USB Power Delivery (USB PD) controller. The IP2726 also controls paralleling of the power supplies for 65W peak power operation. The USB-PD controllers are powered from the outputs of both flyback converters thru the LDO IC (U3). USB PD protocol is communicated over either CC1 or CC2 line depending on the orientation in which Type-C plug is connected.

The IP2726 ICs communicate with InnoSwitch3-Pro IC through the I^2C interface using the SCL and SDA lines in which it sets the CV, CC, V_{KP}, OVA and UVA parameters. These parameters correspond to the output voltage, constant output current, constant output power voltage threshold, output overvoltage threshold, and output undervoltage threshold registers of the InnoSwitch3-Pro IC, respectively. The status of the InnoSwitch3-Pro IC is read by the IP2726 IC from the telemetry registers also using the I^2C interface.

Capacitors C7 and C10 provide decoupling for the LDO. Capacitors C29 and C31, resistors R37 to R40, and TVS diodes D11 to D14 provide protection from ESD to pins D+, D-, CC1 and CC2. The IP2726 has a dedicated sense resistor R42 to measure the USB Port output current. The signal from R42 is filtered by the low pass filter formed by R41 and C26 before entering the ADC port inputs of the IP2726. RT1 is used for temperature sensing while R33 is used to trim the readings of the temperature ADC. Resistors R35 and R36 are the pull-up resistors of the I^2C lines (SDA/SCL). Resistor R32 and C35 form the low pass filter for the V_{IN} input pin of the USB-PC controller.

MOSFETs Q7 and Q8 are used as OR-in FETs for parallel operation. Resistors R15 and R16 are the pull-down resistors for the OR-in FETs.

5 PCB Layout

PCB copper thickness is 1.0 mm.

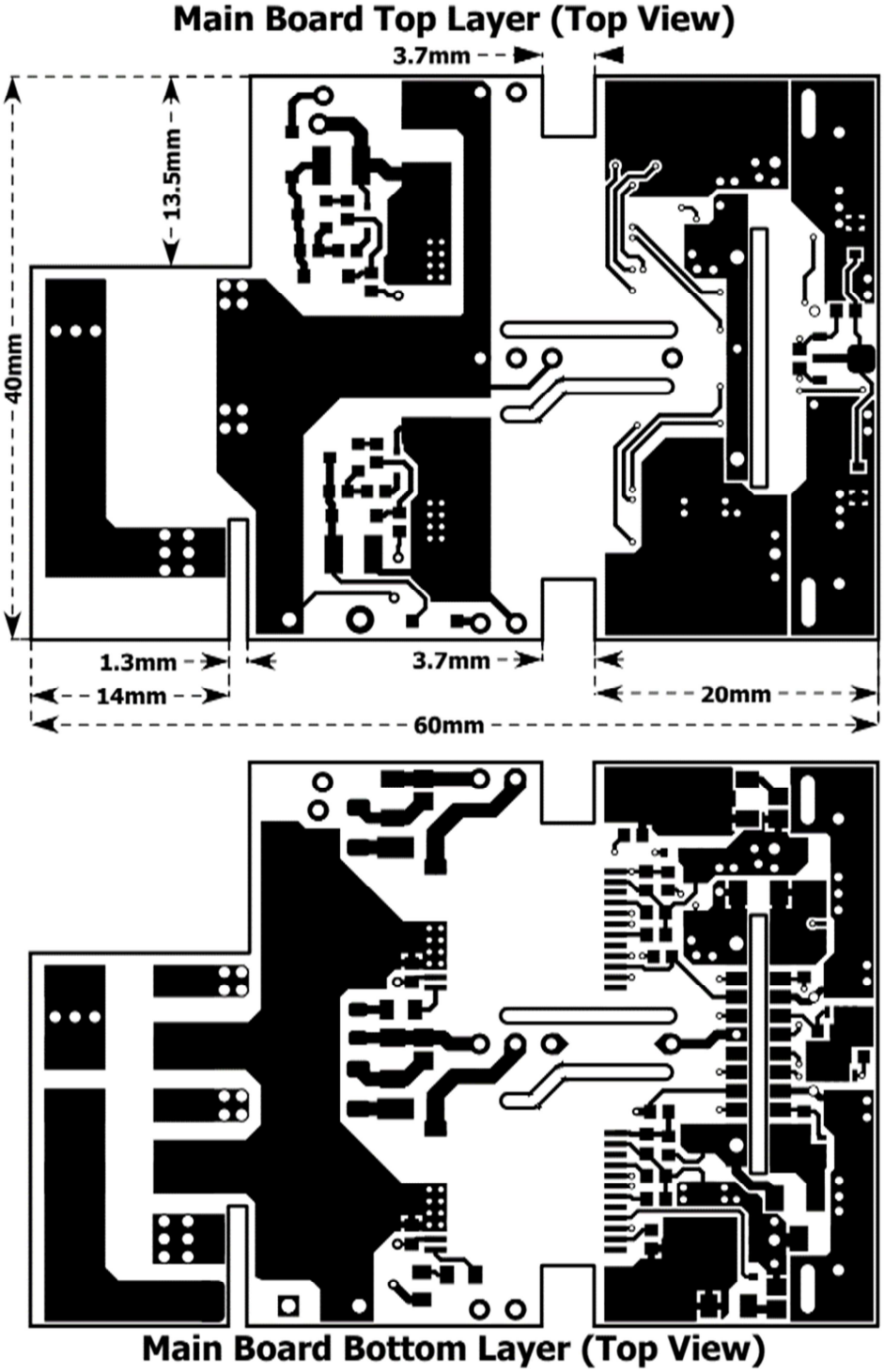


Figure 8 – DER-916 Main Board Rev C Printed Circuit Layout.

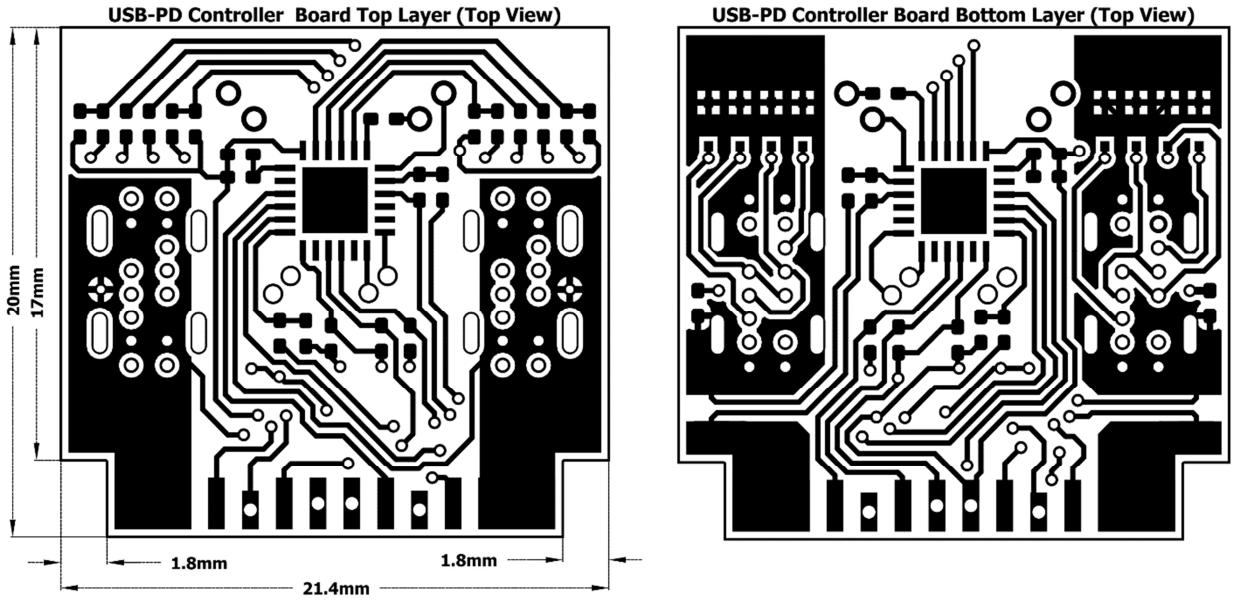


Figure 9 – DER-916 USB PD Controller Board Rev C Printed Circuit Layout.

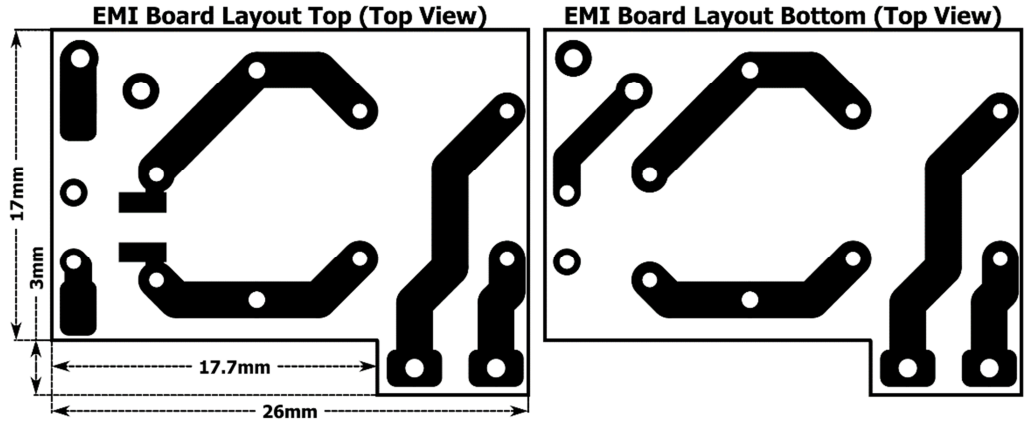


Figure 10 – DER-916 EMI Board Rev C Printed Circuit Layout.

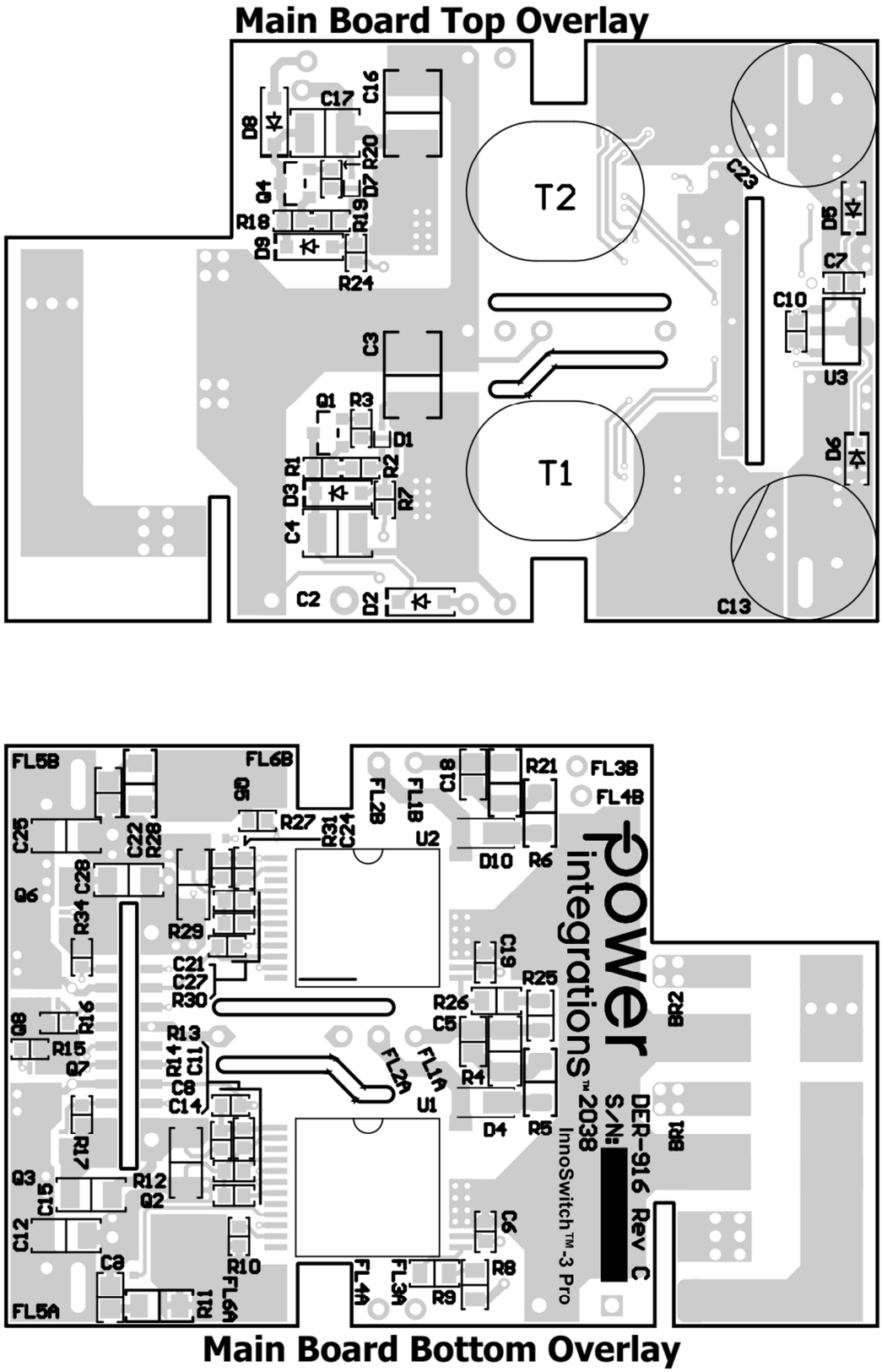


Figure 11 – Main Board Rev C PCB Overlay Layers.

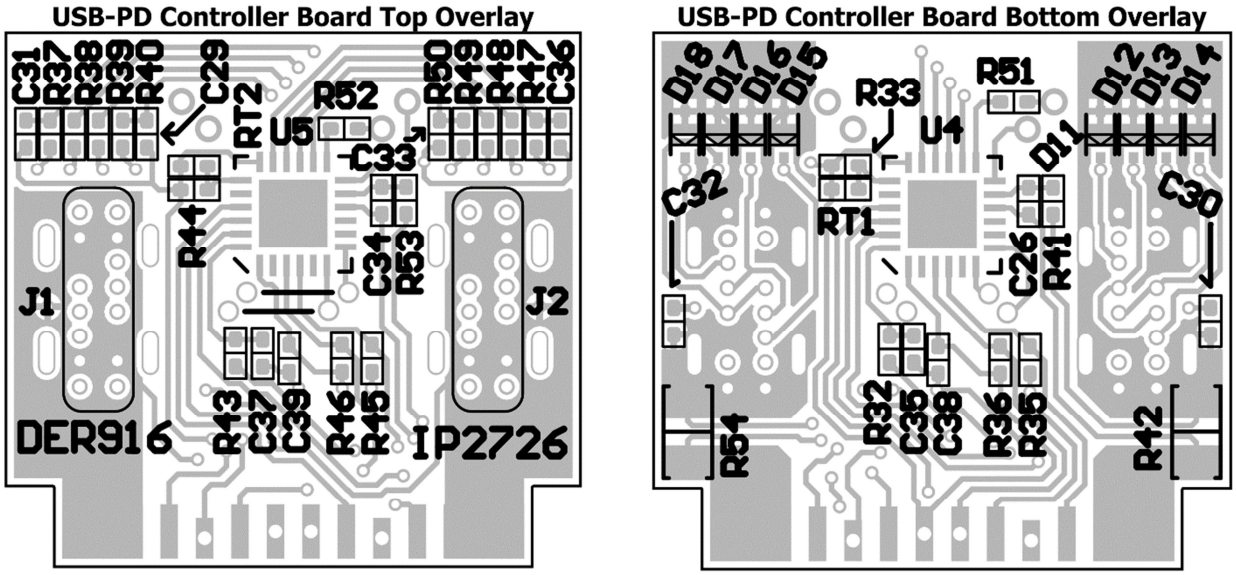


Figure 12 – DER-916 PD Controller Board Rev C PCB Overlay Layers.

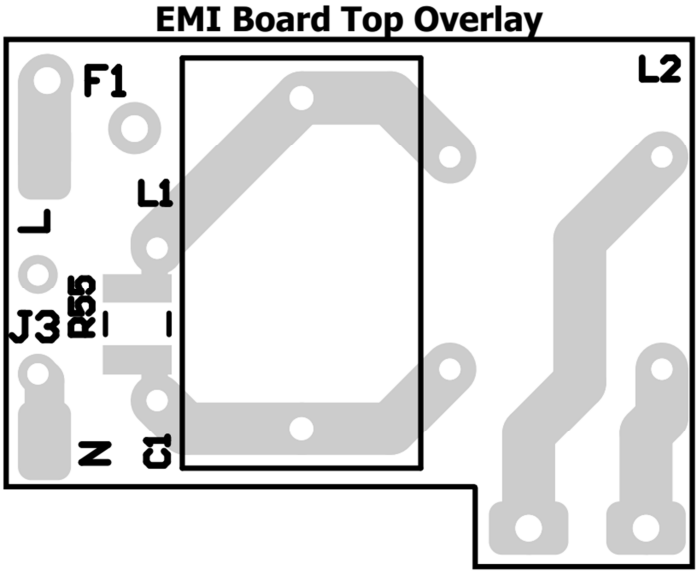


Figure 13 – DER-916 EMI Board Rev C Overlay Layer.

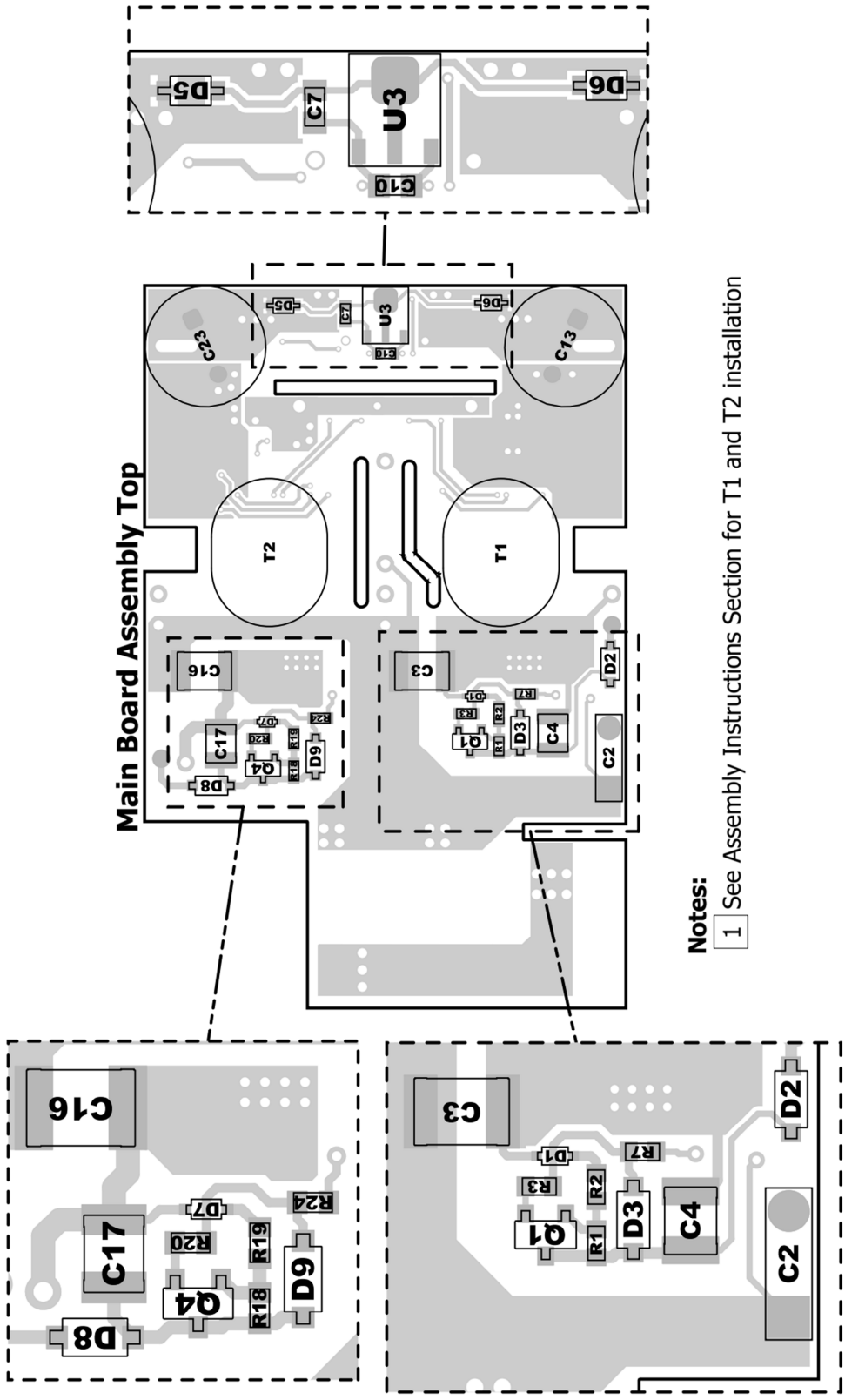


Figure 14 – DER-916 Main Board Rev C PCB Assembly Top.

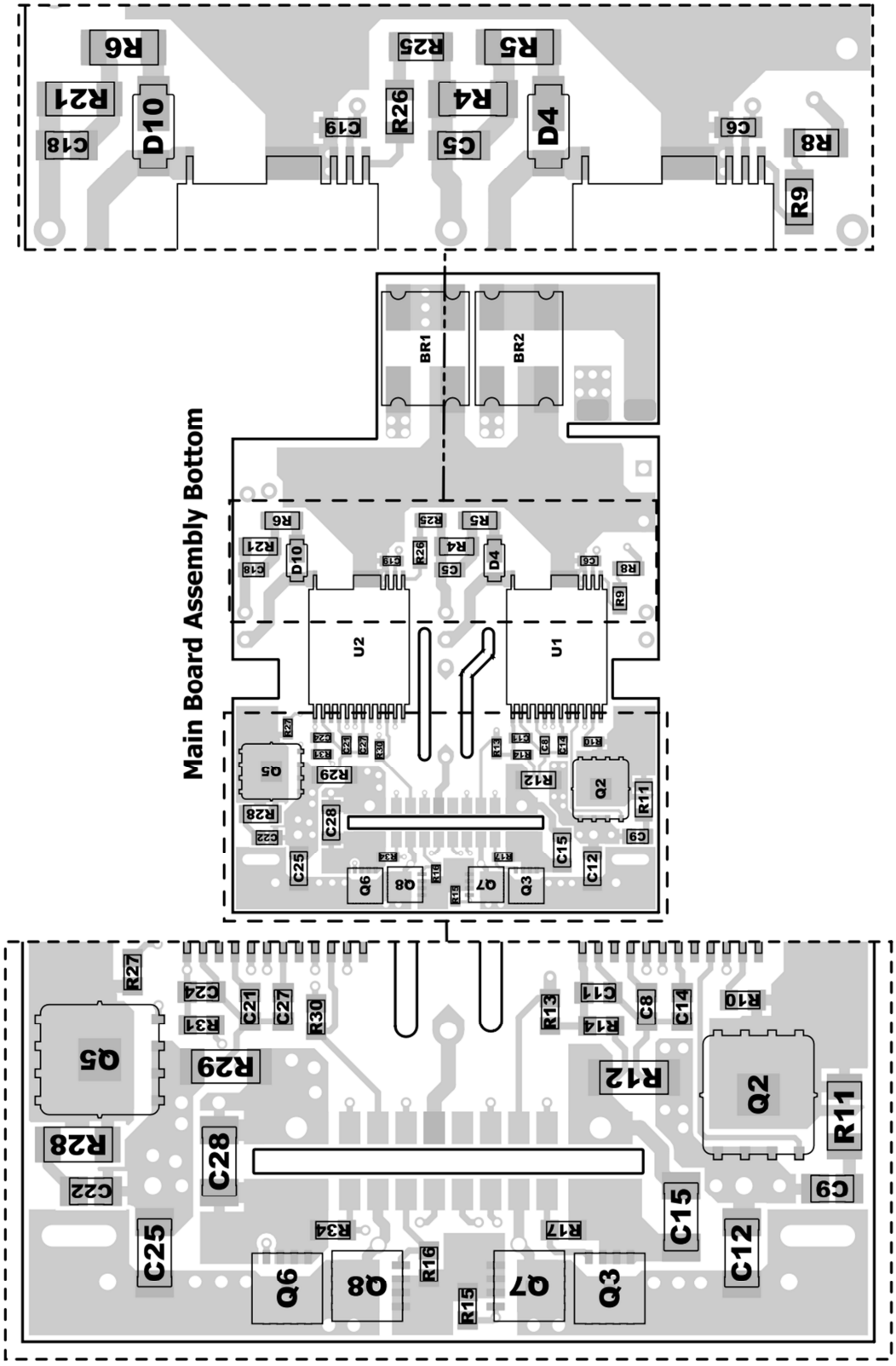


Figure 15 – DER-916 Main Board PCB Rev C Assembly Bottom.

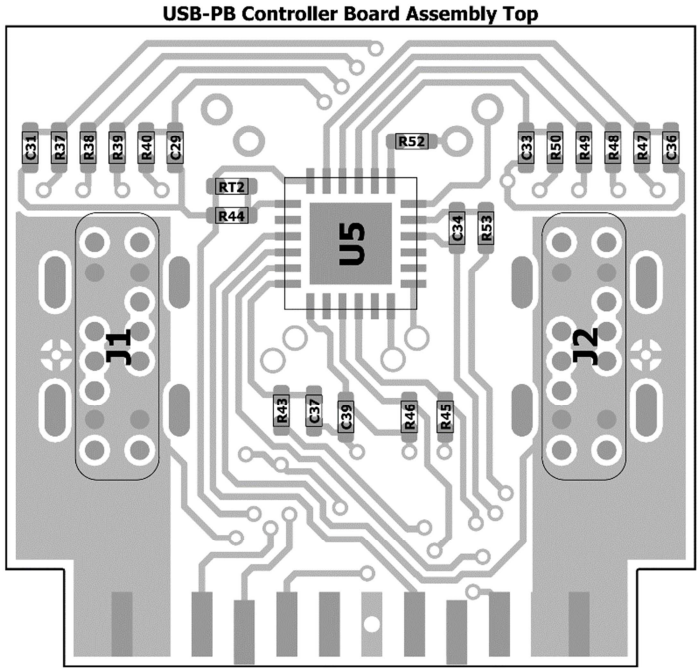


Figure 16 – DER-916 USB PD Controller Rev C Assembly Top.

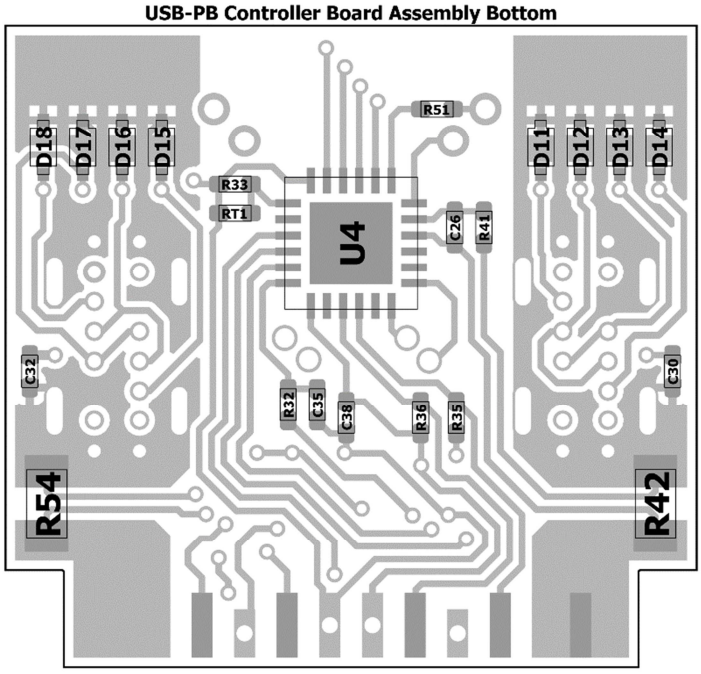


Figure 17 – DER-916 USD PD Controller Rev C Assembly Bottom.

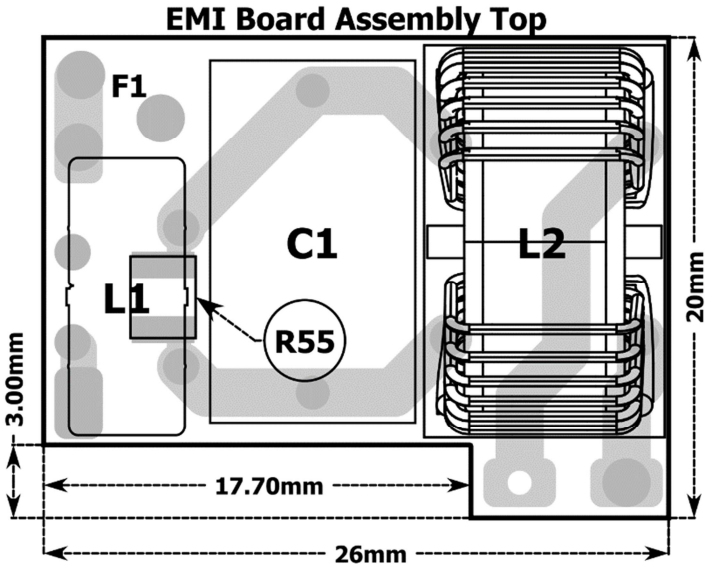


Figure 18 – DER-916 EMI Board Rev C Assembly Top.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	2	BR1 BR2	RECT BRIDGE, GP, 800 V, 4 A, Z4-D	Z4DGP408L-HF	Comchip
2	1	C1	FILM 0.33 µF 10% 275 VAC RAD	890324024003	Würth
3	1	C2	ALUM 120 µF 20% 200 V RADIAL	EKXJ201ELL121MK30S	Rubycon
4	2	C3 C16	1 µF ±5% 200 V Ceramic X7R 1812	18122C105JAT2A	AVX
5	2	C4 C17	CER 10 µF 63 V X7R 1210	CL32B106KMVNNWE	Samsung
6	4	C5 C9 C18 C22	CER 1000 PF 200 V X7R 0805	08052C102KAT2A	AVX
7	2	C6 C19	0.47 µF, 16 V, Ceramic, X7R, 0603	GRM188R71C474KA88D	Murata
8	2	C7 C10	0.1 µF ±10% 25 V Ceramic X7R 0603	06033C104KAT4A	AVX
9	6	C8 C11 C14, C21 C24 C27	2.2 µF 10 V X7R 0603	GRM188R71A225KE15D	Murata
10	4	C12 C15 C25 C28	CER 2.2 µF 25 V X7R 1206	12063C225K4Z2A	AVX
11	2	C13 C23	680 µF 25 V Aluminum - Polymer Radial, Can 16 mΩ 1500 Hrs @ 125 °C	687AVG025MGBJ	Illinois Capacitor
12	1	C20	2200 pF ±20% 250 VAC Ceramic E Radial, Disc	DE1E3RA222MN4AN01F	Murata
13	4	C29 C31 C33 C36	330 pF ±10% 25 V Ceramic X7R 0402	04023C331KAT2A	AVX
14	4	C32 C30, C38 C39	CER 2.2 µF 25 V X5R 0402	C1005X5R1E225K050BC	TDK
15	2	C35 C37	CER 0.1 µF 25 V X7R 0402	CL05B104KA5NNNC	Samsung
16	2	C34 C26	1000 pF ±10% 50 V Ceramic X7R 040	C1005X7R1H102K050BA	TDK
17	2	D1 D7	10 V, 5%, 150 mW, SSMINI-2	EDZVT2R10B	Rohm
18	2	D2 D8	Diode GEN PURP 300 V 225 mA SOD123	BAV3004W-7-F	Diodes, Inc.
19	2	D3 D9	Diode Zener 47 V 500 mW SOD123	MMSZ5261BT1G	ON Semi
20	2	D4 D10	800 V, 1 A, Fast Recovery Rectifier, POWERDI123	DFLF1800-7	Diodes, Inc.
21	2	D5 D6	Diode GEN PURP 100 V 200 mA SOD323	BAV19WS-7-F	Diodes, Inc.
22	8	D11 D12, D13 D14, D15 D16, D17 D18	Zener Diode 24 V 150 mW ±2% SMT EMD2	EDZVT2R24B	Rohm
23	1	F1	3 A 250 V ACDC Fuse Board Mount (Cartridge Style Excluded) Through Hole Axial	0263003.MXL	Littlefuse
24	2	J1 J2	Vertical USB		
25	1	J3	Power Entry Connector Receptacle, Male Pins, IEC 320-C8, Non-Polarized, Panel Mount, Snap-In; TH, Right Angle	RAPC322X	Switchcraft
26	1	L1	250 µH, Toroidal CMC, custom, DER-538, wound on 32-00275-00 core.	32-00367-00	Power Integrations
27	1	L2	Custom, CMC, 18 mH @ 10 kHz, Toroidal, 17.5 mm OD x 11.0 mm thick. 40 turns x 2, 0.40 mm wire 190 mΩ max	04291-T231	Sumida
28	2	Q1 Q4	NPN, Small Signal BJT, 80 V, 0.5 A, SOT-23	MMBTA06LT1G	On Semi
29	2	Q2 Q5	MOSFET, N-CH, 120 V, 85 A (at VGS=10 V), Trench Power AlphaSGT 120 V TM Technology, DFN5x6	AON62922	Alpha & Omega Semi
30	4	Q3 Q6 Q7 Q8	MOSFET, N-CH, 30 V, 48 A (Ta), 50 A (Tc), 6.2 W (Ta), 8.3 W (Tc), SMT, 8-DFN-EP (3.3x3.3)	AON7520C	Alpha & Omega Semi
31	2	R1 R18	RES, 100 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1003V	Panasonic
32	2	R2 R19	RES SMD 5.11 kΩ 1% 1/10 W 0603	ERJ-3EKF5111V	Panasonic
33	2	R3 R20	RES, 3 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ302V	Panasonic
34	2	R4 R21	RES SMD 232 kΩ 1% ¼ W 1206	ERJ-8ENF2323V	Panasonic
35	4	R5 R6 R11 R28	RES, 20 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ200V	Panasonic
36	4	R7 R10 R24 R27	RES, 47 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ470V	Panasonic
37	2	R8 R25	2 MΩ ±1% 0.125 W, 1/8 W Chip Resistor 0805	RMCF0805FT2M00	Stackpole

			Automotive AEC-Q200 Thick Film		
38	2	R9 R26	1.8 MΩ ±1% 0.125 W, 1/8 W Chip Resistor 0805 Automotive AEC-Q200 Thick Film	RMCF0805FT1M80	Stackpole
39	2	R12 R29	9 mΩ ±1% 1 W Chip Resistor 1206 Automotive AEC-Q200, Current Sense Thick Film	PMR18EZPFU9L00	Rohm
40	2	R13 R30	RES SMD 324 kΩ 1% 1/10 W 0603	RC0603FR-07324KL	Yageo
41	2	R14 R31	RES, 10 Ω, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF10R0V	Panasonic
42	4	R15 R16 R17 R34	RES, 100 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1003V	Panasonic
43	6	R32 R43 R38 R3, R48 R49	RES 3 Ω 1% 1/16 W 0402	RMCF0402FT3R00	Stackpole
44	2	R33 R44	CRGCQ 0402 82 kΩ 1%	CRGCQ0402F82K	TE Connectivity
45	4	R35 R3, R45 R46	CRGCQ 0402 4.7 kΩ 1%	CRGCQ0402F4K7	TE Connectivity
46	4	R37 R4, R47 R50	RES SMD 22 Ω 1% 1/16 W 0402	PFR05S-220-FNH	Delta
47	2	R41 R53	RES SMD 1 kΩ 1% 1/16 W 0402	RT0402FRE071KL	Yageo
48	2	R51 R52	RES 0 Ω JUMPER 1/16 W 0402	RMCF0402ZT0R00	Stackpole
49	2	R42 R54	RES 0.005 Ω 1% ½ W 0805	ERJ-6LWFR005V	Panasonic
50	1	R55	RES SMD 4.3 MΩ 1% ¼ W 1206	KTR18EZPF4304	Rohm
51	2	RT1 RT2	NTC, 100 kΩ, 0.5%,0402, AEC-Q200,125	NTCG104ED104DTDSX	TDK
52	2	U1 U2	InnoSwitch3-Pro	INN3370C-H302	Power Integrations
53	1	U3	IC REG LINEAR 3.3 V 150 mA SOT89	AP7380-33Y-13	Diodes, Inc.
54	2	U4 U5	USB-C Quick Charge Protocol IC	IP2726	Injoinic
55	2	T1 T2	ATQ 23.7/14.6 Bobbin	25-01171-00	
56	2	T1 T2	ATQ 23.7/14.6 Core	99-00072-00	

7 Transformer Specification (T1 and T2)

7.1 *Electrical Diagram*

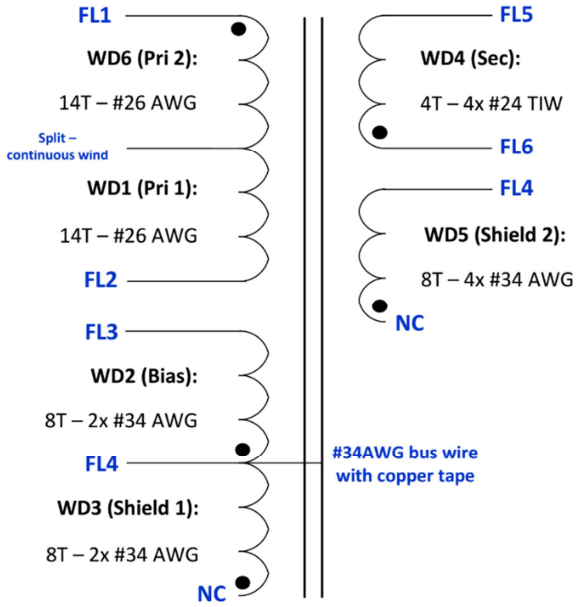


Figure 19 – Transformer Electrical Diagram.

7.2 *Electrical Specifications*

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V_{PK-PK}, 100 kHz switching frequency, between FL1 and FL2, with all other windings open.	370 µH ±5%
Resonant Frequency	Between FL1 and FL2, other windings open.	1200 kHz (Min.)
Primary Leakage Inductance	Between FL1 and FL2, with all other FLs shorted	7.4 µH (Max.)

7.3 *Material List*

Item	Description
[1]	Core: ATQ23.7/14 PI Part #: 99-00072-00.
[2]	Bobbin: ATQ23.7/14 Bobbin PI Part #: 25-01171-00.
[3]	Magnet Wire: #26 AWG, Double Coated.
[4]	Magnet Wire: #34 AWG, Double Coated.
[5]	Magnet Wire: #24 AWG, Triple Insulated Wire.
[6]	Bus Wire: #34 AWG, Double Coated.
[7]	Copper Foil: Copper Tape, 1 mil Thickness, 5 mm Width
[8]	Tape: 3M 1350-F, Polyester Film, 1 mil Thickness, 7.0 mm Width.
[9]	Tape: 3M 1350-F, Polyester Film, 1 mil Thickness, 20 mm Width.
[10]	Varnish: Dolph BC-359.

7.4 *Transformer Build Diagram*

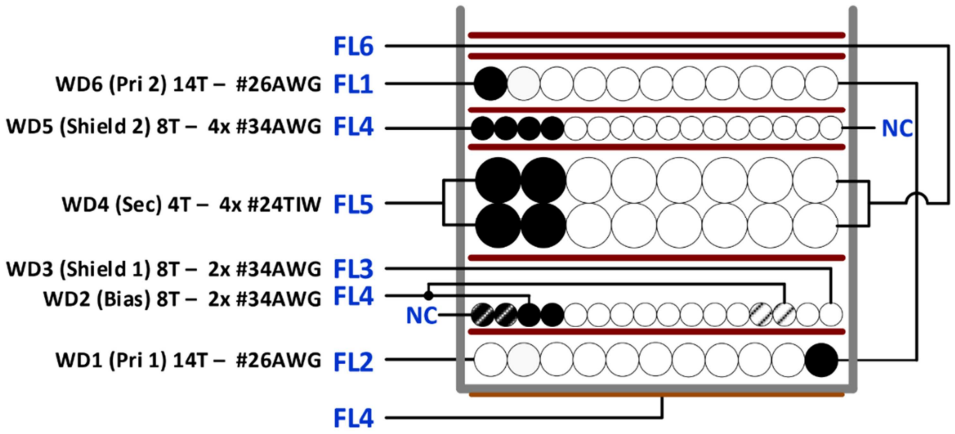


Figure 20 – Transformer Build Diagram.

7.5 *Bobbin Preparation*

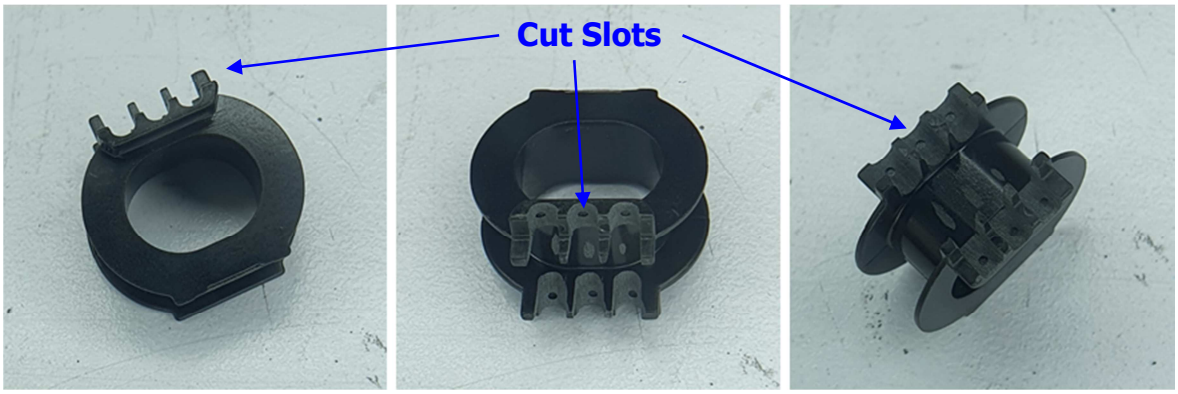


Figure 21 – Transformer 1 Bobbin Modification.

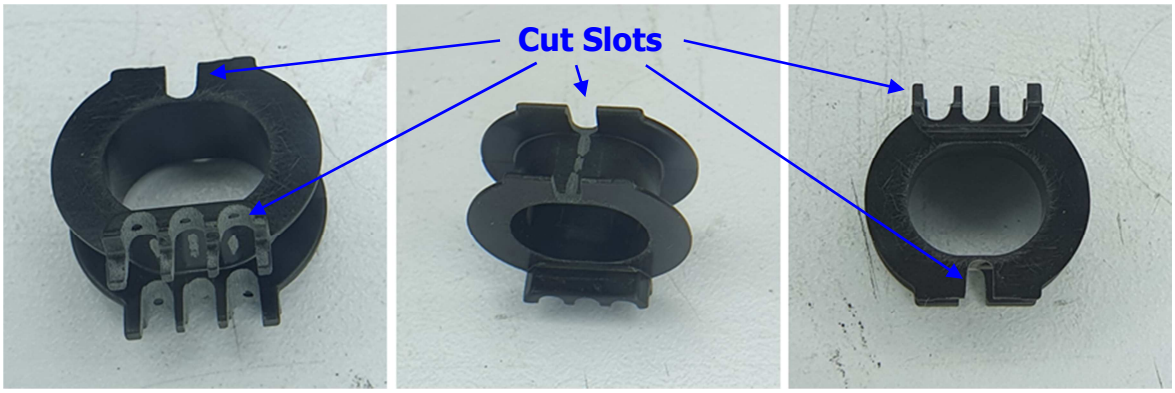


Figure 22 - Transformer 2 Bobbin Modification.

7.6 ***Transformer Construction***

7.6.1 Transformer 1 Construction

Winding Preparation	Make slots on bobbin as shown in Figure 21. Position the bobbin on the mandrel such that the pin side of the bobbin is on the left side. Rotation of mandrel is referenced as seen from the right of the set-up.
WD1 1st Primary	Start at lower left slot, wind 14 turns of wire Item [3] in 1 layer from left to right. Rotation of mandrel is counterclockwise. Exit at lower right slot and secure the remaining wire for use later.
Insulation	2 layers of tape Item [8].
WD2 Bias & WD3 Shield 1	Start at middle left slot using 2 strands Item [4] for WD2. Start at lower left slot using 2 strands of Item [4] for WD3. Mandrel direction is clockwise. Wind all 4 wires simultaneously for 8 turns. Exit at lower right slot. Place start of insulating tape Item [8] as shown and bend back all 4 wires to lower left slot. Cut the start of WD2. This is a No Connect.
Insulation	2 layers of tape Item [8]. Combine the end of WD2 to the start of WD3. Twist the wires together. This will be FL4. The end of WD3 will be FL3.
WD4 Secondary	Start at the middle left slot of the bobbin. Use 2 strands Item [5] and wind clockwise. Leave ~1.5" floating and mark as FL5. Wind 4 turns in 1 layer. At the last turn, exit at the middle right slot. Leave ~1.5" floating and mark as FL6. Repeat steps above to complete the secondary winding. All 4 wires are in parallel.
Insulation	2 layers of tape Item [8].
WD5 Shield 2	Start at lower left slot. Wind 8 turns using 4 strands of wire Item [4]. Exit at lower right slot.
Insulation	2 layers of tape Item [8]. Position remaining wire for the primary winding.
WD6 2nd Primary	Use wire hanging from WD1 and continue winding 14 turns from left to right. Mandrel direction is counterclockwise. Exit at lower left slot. This is FL1A.[3]
Insulation	2 layers of tape Item [8]. Bend back the secondary winding through the upper slots as shown.
Gap and Ground Core	Add gap to the middle leg of core Item [1] to get 370 uH primary inductance. Place copper tape to secure core as shown. Solder copper tape intersections to ensure good connection. Solder FL4 end of Shield 2 winding to copper tape. Solder 1 strand of wire Item [4] to copper tape. Twist this wire together with the FL4 end of the Bias and Shield 1 winding bundle.
Finish	Add another 2 layers of tape Item [8] to transformer bottom and sides to cover copper tape. Cover secondary-side of core with tape Item [9] Varnish using Item [10]. Trim all Fly-leads to at least 25 mm.

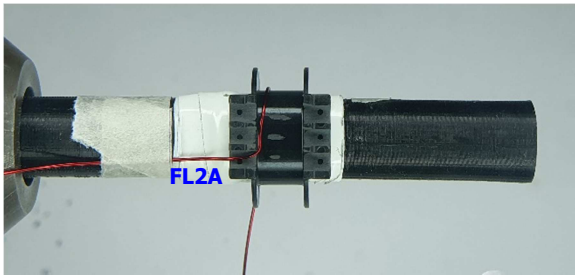
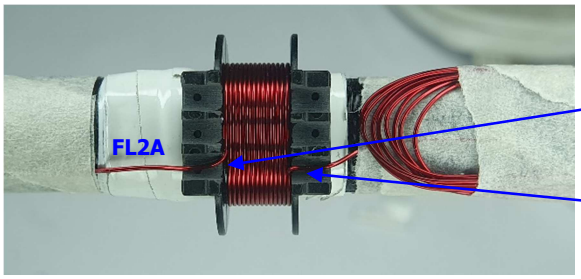
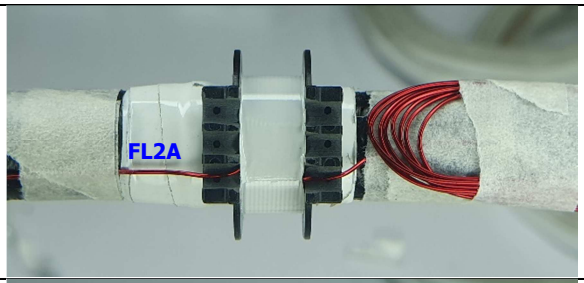
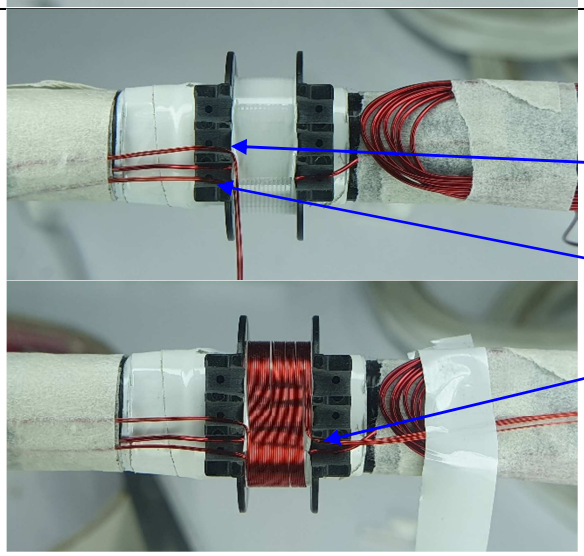
[3] FL*xy* refers to Fly-lead number *x* (*x* = 1 to 6) of transformer *y* (A for Transformer 1 or B for Transformer 2) e.g. FL1A is Fly-lead 1 of Transformer A.

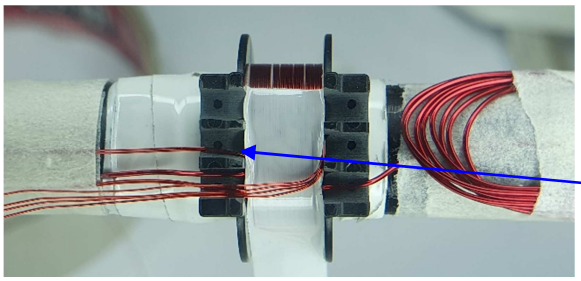
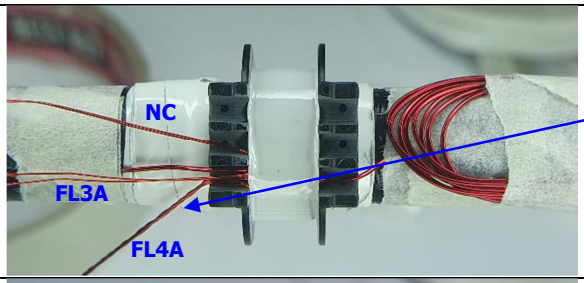
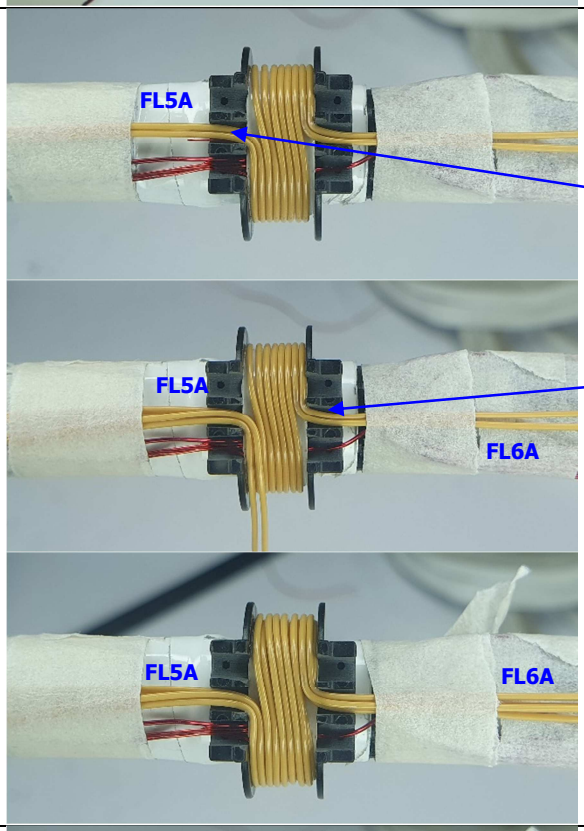
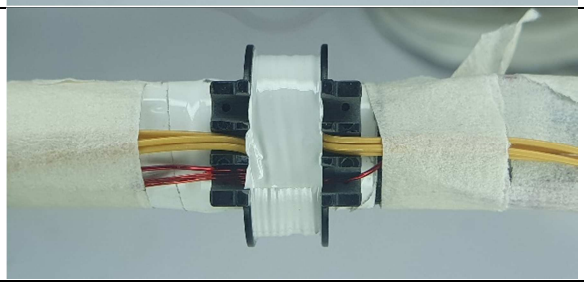
7.6.2 Transformer 2 Construction

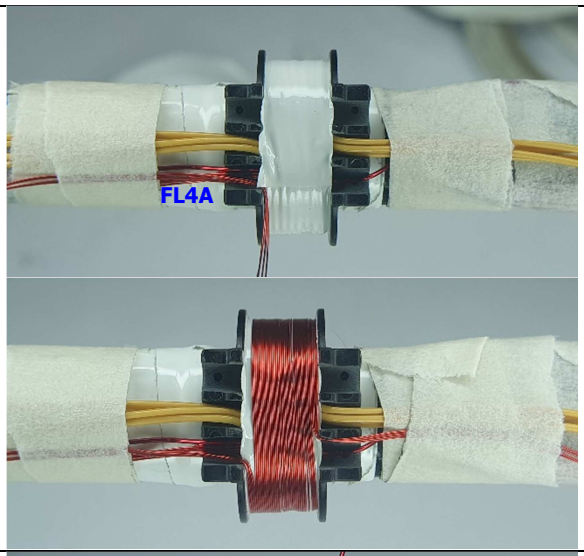
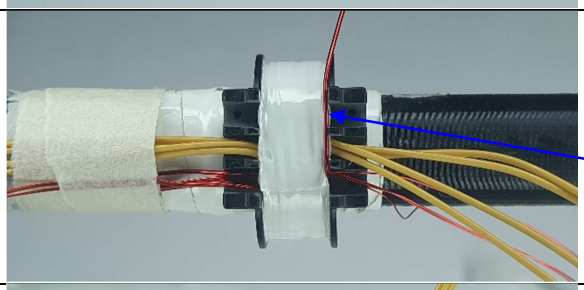
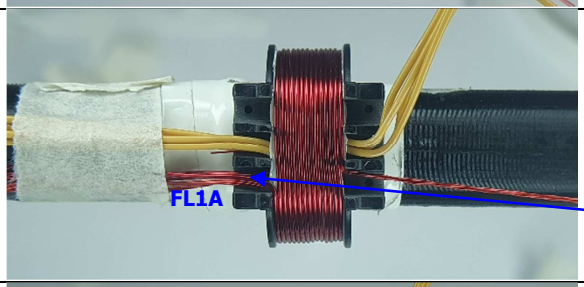
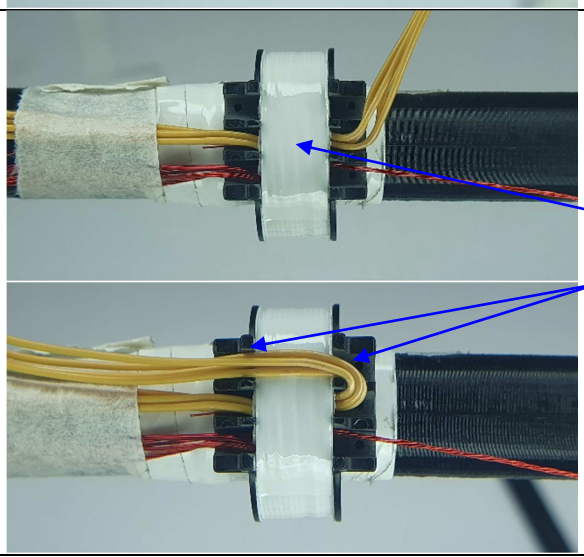
Winding Preparation	Make slots on bobbin as shown in Figure 22. Position the bobbin on the mandrel such that the pin side of the bobbin is on the left. Rotation of mandrel is referenced as seen from the right of the set-up. Start at side of bobbin with only 2 slots.
WD1 1st Primary	Start at left slot, wind 14 turns of wire Item [3] in 1 layer from left to right. Rotation of mandrel is counterclockwise. Exit at right slot and secure the remaining wire for use later.
Insulation	2 layers of tape Item [8]. Rotate mandrel to show section of bobbin with 6 slots.
WD2 Bias & WD3 Shield 1	Start at upper left slot using 2 strands Item [4] for WD2. Start at upper left slot using 2 strands of Item [4] for WD3. Mandrel direction is clockwise. Wind all 4 wires simultaneously for 8 turns. Exit at middle right slot. Place start of insulating tape Item [8] as shown and bend back all 4 wires to upper left slot.
Insulation	2 layers of tape Item [8]. Combine the end of WD2 to the start of WD3. Twist the wires together. This will be FL4. Cut the start of WD2. This is a No Connect. The end of WD3 will be FL3.
WD4 Secondary	Start at the middle left slot of the bobbin. Use 2 strands Item [5] and wind clockwise. Leave ~1.5" floating and mark as FL5. Wind 4 turns in 1 layer. At the last turn, exit at the middle right slot. Leave ~1.5" floating and mark as FL6. Repeat steps above to complete the secondary winding. All 4 wires are in parallel.
Insulation	2 layers of tape Item [8].
WD5 Shield 2	Start at upper left slot. Wind 8 turns using 4 strands of wire Item [4]. Exit at middle right slot.
Insulation	2 layers of tape Item [8]. Cut end of Shield 2 (WD5) for No Connect.
WD6 2nd Primary	Rotate mandrel to show bobbin side with 2 slots. Resume winding wire from WD1 14 turns from right to left. Mandrel direction is counter clockwise. Exit at left slot. This is FL1B.
Insulation	2 layers of tape Item [8]. Bend back the secondary winding through the lower slots as shown. Secure with 2 layers tape Item [8]. Bend FL1B and FL2B as shown. Cover slots with 2 layers tape Item [8] to isolate primary wires from core. Cover both slots.
Gap and Ground Core	Add gap to the middle leg of core Item [1] to get 370 uH primary inductance. Place copper tape to secure core as shown. Solder copper tape intersections to ensure good connection. Place 2 layers tape Item [8] as shown to isolate primary winding from core. Bend primary wires over tape. Solder FL4 end of Shield 2 to copper tape. Solder 1 strand of wire Item [4] to copper tape. Twist this wire together with the FL4 end of the Bias and Shield 1 winding bundle. Cover copper tape with tape Item [8]. Use 2 layers.
Finish	Cover secondary-side of transformer core using tape Item [9]
	Varnish using Item [10]. Trim all Fly-leads to at least 25 mm.

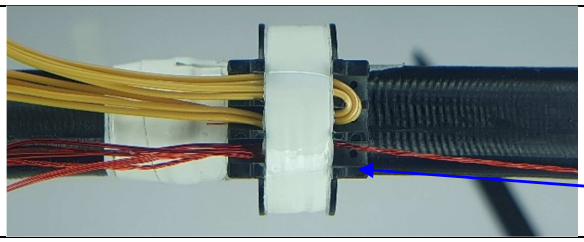
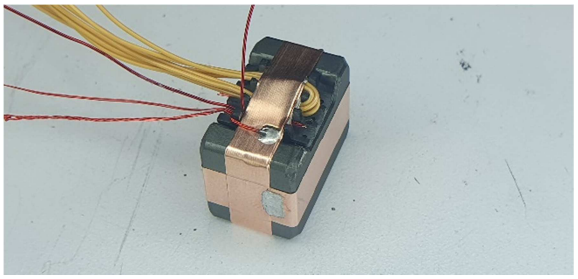
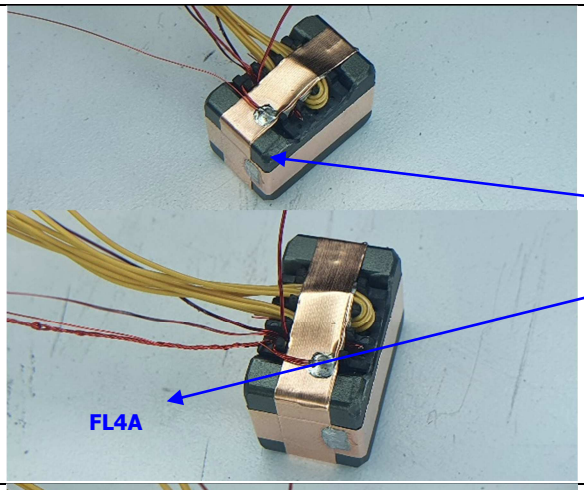
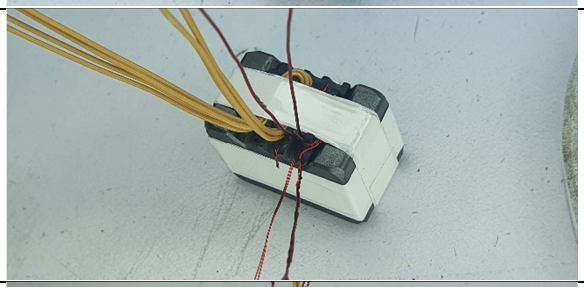
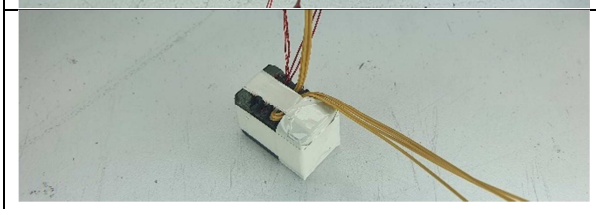
7.7 *Winding Illustrations*

7.7.1 Transformer 1 Winding Illustrations

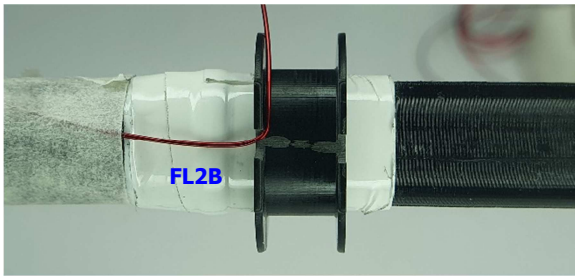
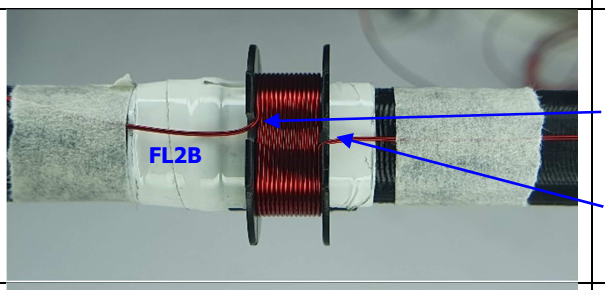
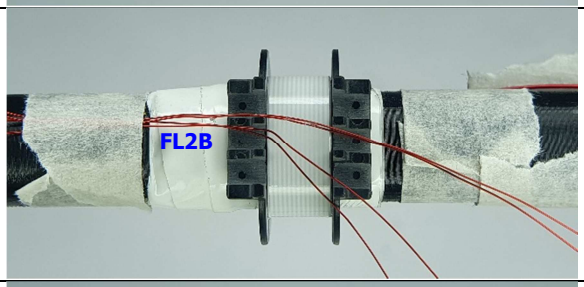
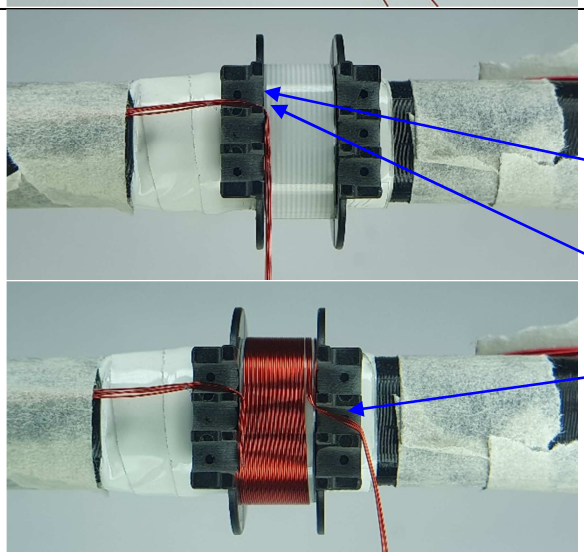
Winding Preparation		Make slots on bobbin as shown in Figure 21. Position the bobbin on the mandrel such that the pin side of the bobbin is on the left side. Rotation of mandrel is referenced as seen from the right of the setup.
WD1 **1st Primary**		Start at lower left slot, wind 14 turns of wire Item [3] in 1 layer from left to right. Rotation of mandrel is counter clockwise. Exit at lower right slot and secure the remaining wire for use later.
Insulation		2 layers of tape Item [8].
WD2: Bias **&** **WD3: Shield 1**		Start at middle left slot using 2 strands Item [4] for WD2. Start at lower left slot using 2 strands of Item [4] for WD3. Mandrel direction is clockwise. Wind all 4 wires simultaneously for 8 turns. Exit at lower right slot.

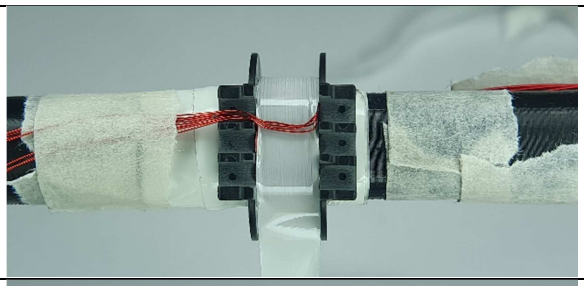
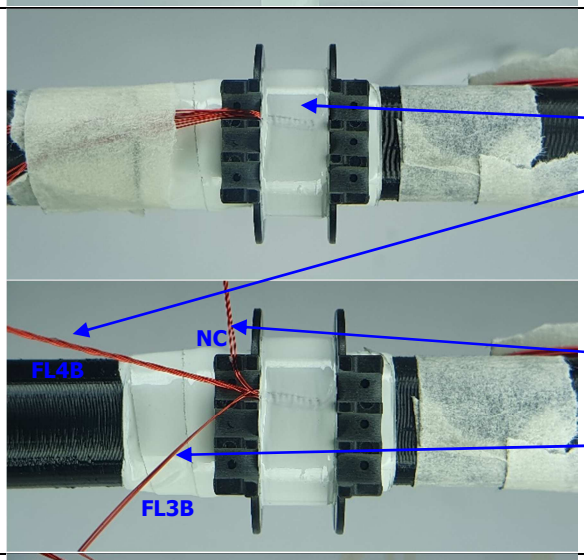
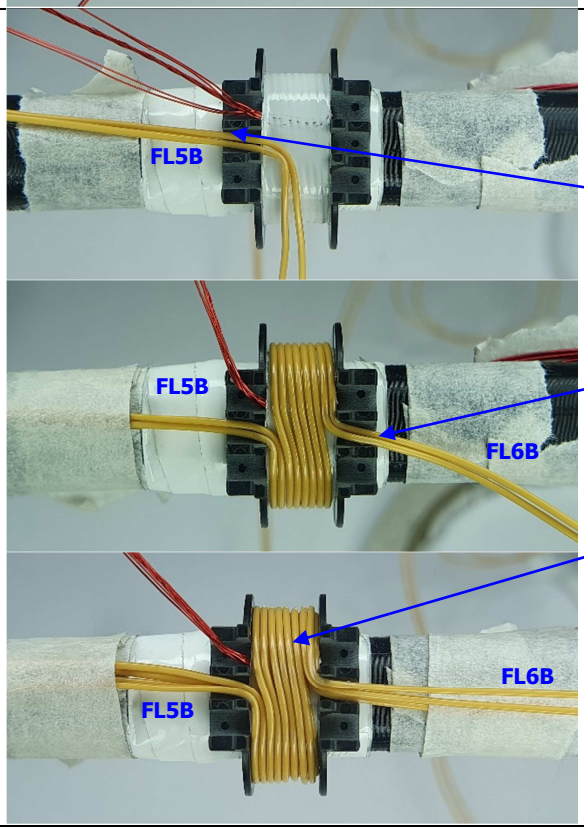
WD2: Bias & WD3: Shield 1		Place start of insulating tape Item [8] as shown and bend back all 4 wires to lower left slot. Cut the start of WD2. This is a No Connect.
Insulation		2 layers of tape Item [8]. Combine the end of WD2 to the start of WD3. Twist the wires together. This will be FL4. The end of WD3 will be FL3.
WD4 Secondary		Start at the middle left slot of the bobbin. Use 2 strands Item [5] and wind clockwise. Leave ~1.5” floating and mark as FL5. Wind 4 turns in 1 layer. At the last turn, exit at the middle right slot. Leave ~1.5” floating and mark as FL6. Repeat steps above to complete the secondary winding. All 4 wires are in parallel.
Insulation		2 layers of tape Item [8].

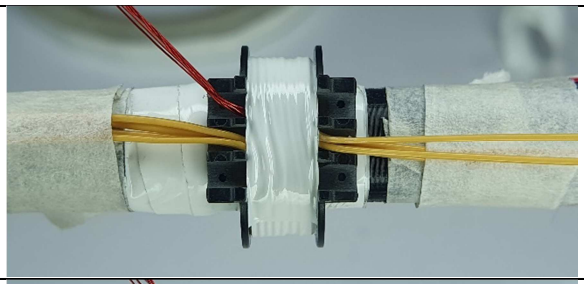
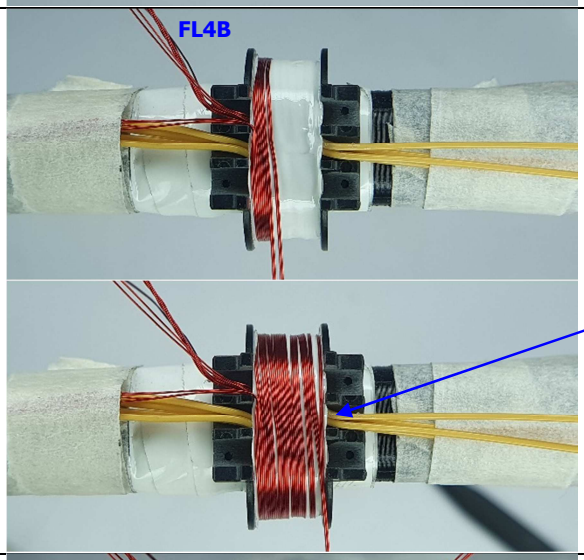
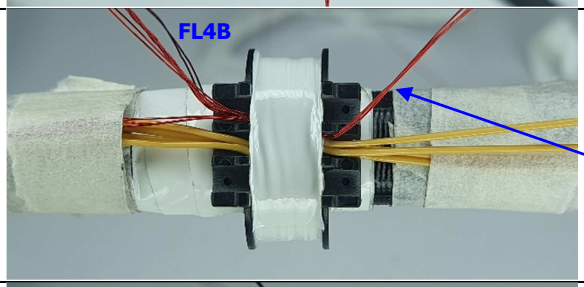
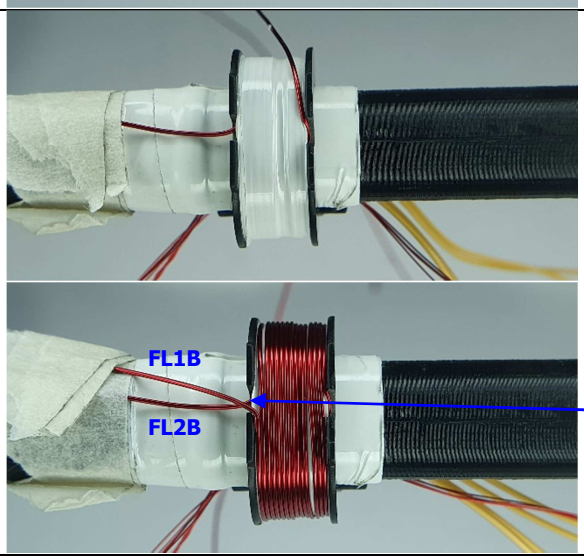
WD5 **Shield2**		Start at lower left slot. Wind 8 turns using 4 strands of wire Item [4]. Exit at lower right slot.
Insulation		2 layers of tape Item [8]. Position remaining wire for the primary winding as shown.
WD6 **2nd Primary**		Use wire hanging from WD1 and continue winding 14 turns from left to right. Mandrel direction is counter clockwise. Exit at lower left slot. This is FL1A.
Insulation		2 layers of tape Item [8]. Bend back the secondary winding through the upper slots as shown.

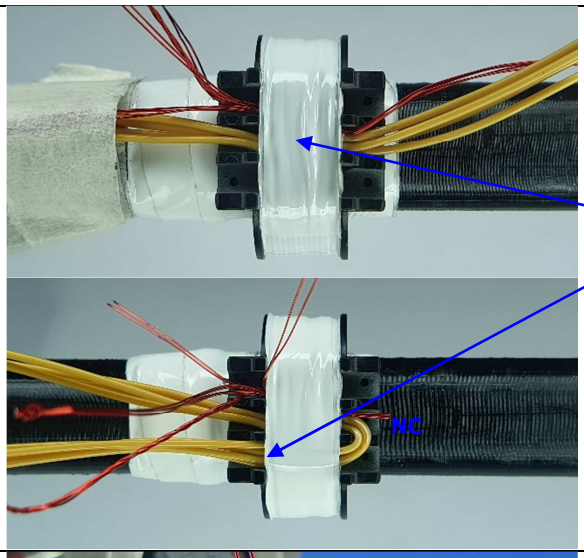
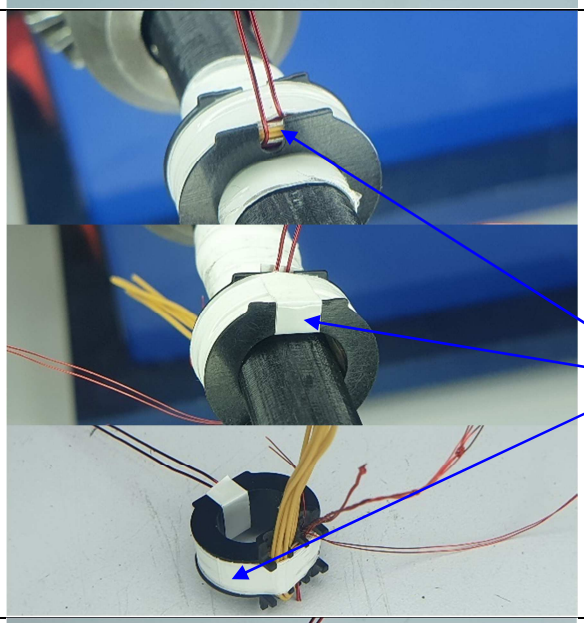
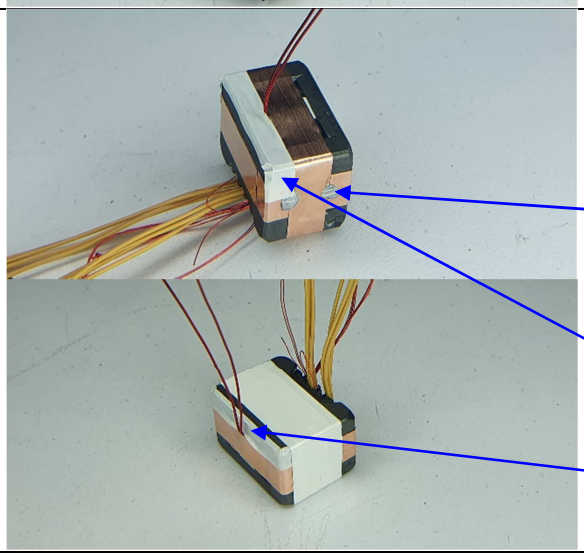
Insulation		2 layers of tape Item [8] to secure bent secondary. Cut NC end of Shield 2.
Gap core and Install		Add gap to the middle leg of core Item [1] to get 370 µH primary inductance. Place copper tape to secure core as shown. Solder copper tape intersections to ensure good connection. Solder FL4 end of Shield 2 winding to copper tape.
		Solder 1 strand of wire Item [4] to copper tape as shown. Twist this wire together with the FL4 end of the Bias and Shield 1 winding bundle.
Finish Assembly		Add another 2 layers of tape Item [8] to transformer bottom and sides to cover copper tape.
		Cover secondary-side of core with tape Item [9] Varnish using Item [10] Trim all Fly-leads to at least 25mm.

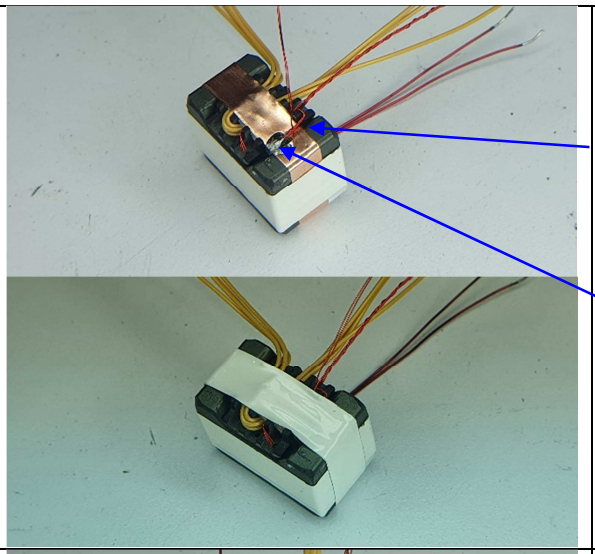
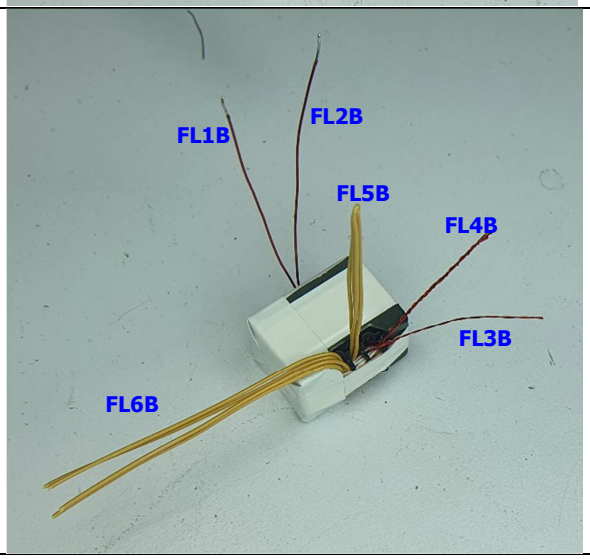
7.7.2 Transformer 2 Winding Illustrations

Winding Preparation		Make slots on bobbin as shown in Figure 22. Position the bobbin on the mandrel such that the pin side of the bobbin is on the left. Rotation of mandrel is referenced as seen from the right of the setup. Start at side of bobbin with only 2 slots.
WD1 **1st Primary**		Start at left slot, wind 14 turns of wire Item [3] in 1 layer from left to right. Rotation of mandrel is counter clockwise. Exit at right slot and secure the remaining wire for use later.
Insulation		2 layers of tape Item [8]. Rotate mandrel to show section of bobbin with 6 slots.
WD2: Bias **&** **WD3: Shield 1**		Start at upper left slot using 2 strands Item [4] for WD2. Start at upper left slot using 2 strands of Item [4] for WD3. Mandrel direction is clockwise. Wind all 4 wires simultaneously for 8 turns. Exit at middle right slot.

WD2: Bias & WD3: Shield 1		Place start of insulating tape Item [8] as shown and bend back all 4 wires to upper left slot.
Insulation		2 layers of tape Item [8]. Combine the end of WD2 to the start of WD3. Twist the wires together. This will be FL4. Cut the start of WD2. This is a No Connect. The end of WD3 will be FL3.
WD4 Secondary		Start at the middle left slot of the bobbin. Use 2 strands Item [5] and wind clockwise. Leave ~1.5” floating and mark as FL5. Wind 4 turns in 1 layer. At the last turn, exit at the middle right slot. Leave ~1.5” floating and mark as FL6. Repeat steps above to complete the secondary winding. All 4 wires are in parallel.

Insulation		2 layers of tape Item [8].
WD5 **Shield2**		Start at upper left slot. Wind 8 turns using 4 strands of wire Item [4]. Exit at middle right slot.
Insulation		2 layers of tape Item [8]. Cut end of Shield 2 (WD5) for No Connect.
WD6 **2nd Primary**		Rotate mandrel to show bobbin side with 2 slots. Resume winding wire from WD1 14 turns from right to left. Mandrel direction is counter clockwise. Exit at left slot. This is FL1B.

Insulation		2 layers of tape Item [8]. Bend back the secondary winding through the lower slots as shown. Secure with 2 layers tape Item [8]
		Bend FL1B and FL2B as shown. Cover slots with 2 layers tape Item [8] to isolate primary wires from core. Cover both slots.
Gap core and Install		Add gap to the middle leg of core Item [1] to get 370 µH primary inductance. Place copper tape to secure core as shown. Solder copper tape intersections to ensure good connection. Place 2 layers tape Item [8] as shown to isolate primary winding from core. Bend primary wires over tape.

		Solder FL4 end of Shield 2 to copper tape. Solder 1 strand of wire Item [4] to copper tape. Twist this wire together with the FL4 end of the Bias and Shield 1 winding bundle. Cover copper tape with tape Item [8]. Use 2 layers.
Finish Assembly		Cover secondary-side of transformer core using tape Item [9]
		Varnish using Item [10] Trim all Fly-leads to at least 25mm.

8 Common Mode Choke Specifications

8.1 *18 mH Common Mode Choke (L2)*

8.1.1 Electrical Diagram

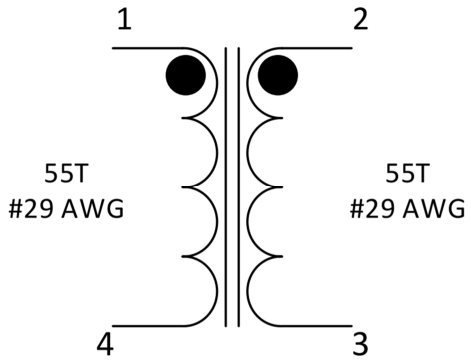


Figure 23 – Inductor Electrical Diagram.

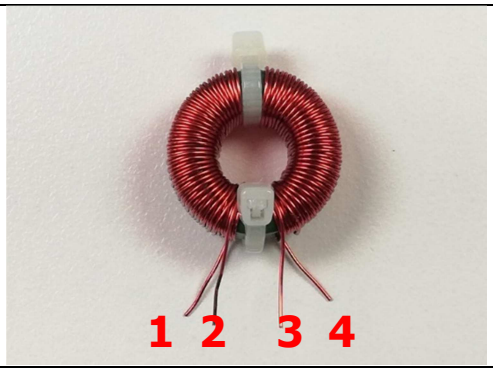
8.1.2 Electrical Specifications

Inductance	Across pin 1 to pin 4 (or pin 2 to pin 3) with the other winding open.	18 mH ±25%
Leakage Inductance	Across pin 1 to pin 4 (or pin 2 to pin 3) with the other winding shorted.	80 µH ±10%
LCR Meter Setting	L_S measurement, 100 kHz switching frequency, 1.0 V test level	

8.1.3 Material List

Item	Description
[1]	Core, Ferrite Inductor Toroid, 14 mm OD x 8 mm ID x 5.5 mm H. PI#: 32-00286-00.
[2]	Cable Tie, PLT.6SM-M, 1.8 mm Thick. PI#: 75-00202-00
[3]	Magnet Wire: #29 AWG, Double Coated.
[4]	Varnish: Dolph BC-359.
[5]	Heat Shrink: Heat Shrink 1” Inner Diameter, 0.035” Wall Thickness. PI#: 62-00002-00; cut to 0.75” length

8.1.4 Winding Instructions



Place cable ties Item [2] to divide core Item [1] into two sections.

Start as pin 1 with Item [3], wind 55 turns in two layers on half section of the core. Mark end of wire as Pin 4.

Repeat procedure on remaining half of core. Start as pin 2 and end as pin 3.

Remove cable ties and varnish the CMC using Item [4].

8.2 *250 µH Common Mode Choke (L1)*

8.2.1 Electrical Diagram

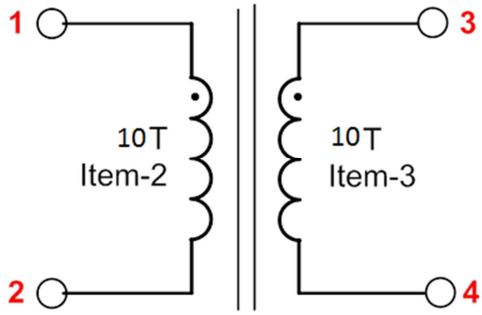


Figure 24 – Inductor Electrical Diagram.

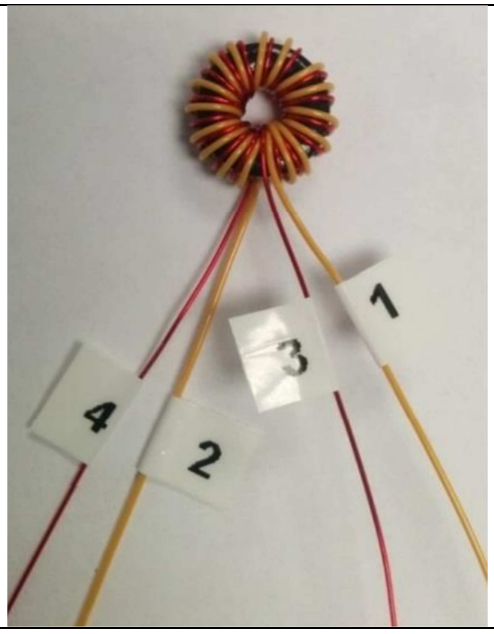
8.2.2 Electrical Specifications

Inductance	Across pin 1 to pin 2 (or pin 4 to pin 3) with the other winding open.	250 µH ±10%
LCR Meter Setting	L_S measurement, 100 kHz switching frequency, 1.0 V test level.	

8.2.3 Material List

Item	Description
[1]	Core, Ferrite Inductor Toroid; PI#: 32-00275-00.
[2]	Magnet Wire: #24 AWG, Triple Insulated Wire.
[3]	Magnet Wire: #24 AWG, Double Coated.
[4]	Varnish: Dolph BC-359.

8.2.4 Winding Instructions



Start as pin 1 for Item [2] and pin 4 for Item [3].

Wind together 10 turns on core Item [1].

Mark end of Item [2] as pin 2 and end of Item [3] as pin 3.

Varnish the CMC using Item [4].

9 Transformer Design Spreadsheet

1	ACDC_InnoSwitch3-Pro_Flyback_032521; Rev.2.1; Copyright Power Integrations 2021	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3-Pro Flyback Design Spreadsheet
2	**APPLICATION VARIABLES**					
3	VAC_MIN	100		100	V	Minimum AC line voltage
4	VAC_MAX	132		132	V	Maximum AC input voltage
5	VAC_RANGE			LOW LINE		AC line voltage range
6	FLINE			60	Hz	AC line voltage frequency
7	CAP_INPUT	120.0		120.0	uF	Input capacitance
9	**SET-POINT 1**					
10	VOUT1	20.00		20.00	V	Output voltage 1, should be the highest output voltage required
11	IOUT1	2.250		2.250	A	Output current 1
12	POUT1			45.00	W	Output power 1
13	EFFICIENCY1	0.92		0.92		Converter efficiency for output 1
14	Z_FACTOR1	0.50		0.50		Z-factor for output 1
15	TYPE	PDO		PDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO (Additional Power Delivery Object)
17	**SET-POINT 2**					
18	VOUT2	15.00		15.00	V	Output voltage 2
19	IOUT2	3.000		3.000	A	Output current 2
20	POUT2			45.00	W	Output power 2
21	EFFICIENCY2	0.92		0.92		Converter efficiency for output 2
22	Z_FACTOR2	0.50		0.50		Z-factor for output 2
23	TYPE	PDO		PDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO (Additional Power Delivery Object)
25	**SET-POINT 3**					
26	VOUT3	9.00		9.00	V	Output voltage 3
27	IOUT3	3.000		3.000	A	Output current 3
28	POUT3			27.00	W	Output power 3
29	EFFICIENCY3	0.92		0.92		Converter efficiency for output 3
30	Z_FACTOR3	0.50		0.50		Z-factor for output 3
31	TYPE	PDO		PDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO (Additional Power Delivery Object)
33	**SET-POINT 4**					
34	VOUT4	5.00		5.00	V	Output voltage 4
35	IOUT4	3.000		3.000	A	Output current 4
36	POUT4			15.00	W	Output power 4
37	EFFICIENCY4	0.92		0.92		Converter efficiency for output 4
38	Z_FACTOR4	0.50		0.50		Z-factor for output 4
39	TYPE	PDO		PDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO (Additional Power Delivery Object)
85	**PRIMARY CONTROLLER SELECTION**					
86	ENCLOSURE	ADAPTER		ADAPTER		Power supply enclosure
87	ILIMIT_MODE	STANDARD		STANDARD		Device current limit mode
88	VDRAIN_BREAKDOWN	750		750	V	Device breakdown voltage
89	DEVICE_GENERIC	INN33X0		INN33X0		Device selection
90	DEVICE_CODE			INN3370C		Device code
91	PDEVICE_MAX			75	W	Device maximum power capability
92	RDSON_25DEG			0.39	Ω	Primary switch on-time resistance at 25°C
93	RDSON_100DEG			0.54	Ω	Primary switch on-time resistance at

						100°C
94	ILIMIT_MIN			2.139	A	Primary switch minimum current limit
95	ILIMIT_TYP			2.300	A	Primary switch typical current limit
96	ILIMIT_MAX			2.461	A	Primary switch maximum current limit
97	VDRAIN_ON_PRSW			0.21	V	Primary switch on-time voltage drop
98	VDRAIN_OFF_PRSW			395.248	V	Peak drain voltage on the primary switch during turn-off
102	**WORST CASE ELECTRICAL PARAMETERS**					
103	FSWITCHING_MAX	65000		65000	Hz	Maximum switching frequency at full load and the valley of the minimum input AC voltage
104	VOR	140.0		140.0	V	Voltage reflected to the primary winding (corresponding to set-point 1) when the primary switch turns off
105	VMIN			120.24	V	Valley of the rectified minimum input AC voltage at full load
106	KP			1.369		Measure of continuous/discontinuous mode of operation
107	MODE_OPERATION			DCM		Mode of operation
108	DUTYCYCLE			0.390		Primary switch duty cycle
109	TIME_ON			7.17	us	Primary switch on-time
110	TIME_OFF			9.45	us	Primary switch off-time
111	LPRIMARY_MIN			350.8	uH	Minimum primary magnetizing inductance
112	LPRIMARY_TYP			369.2	uH	Typical primary magnetizing inductance
113	LPRIMARY_TOL			5.0	%	Primary magnetizing inductance tolerance
114	LPRIMARY_MAX			387.7	uH	Maximum primary magnetizing inductance
116	**PRIMARY CURRENT**					
117	IAVG_PRIMARY			0.391	A	Primary switch average current
118	IPEAK_PRIMARY			2.251	A	Primary switch peak current
119	IPEDESTAL_PRIMARY			0.000	A	Primary switch current pedestal
120	IRIPPLE_PRIMARY			2.251	A	Primary switch ripple current
121	IRMS_PRIMARY			0.766	A	Primary switch RMS current
123	**SECONDARY CURRENT**					
124	IPEAK_SECONDARY			15.760	A	Secondary winding peak current
125	IPEDESTAL_SECONDARY			0.000	A	Secondary winding pedestal current
126	IRMS_SECONDARY			5.730	A	Secondary winding RMS current
127	IRIPPLE_CAP_OUT			4.882	A	Output capacitor ripple current
131	**TRANSFORMER CONSTRUCTION PARAMETERS**					
132	**CORE SELECTION**					
133	CORE	CUSTOM	Info	CUSTOM		Refer to the Transformer Parameters tab to verify fit factor
134	CORE NAME	ATQ23.7/14.6		ATQ23.7/14.6		Core code
135	AE	103.0		103.0	mm^2	Core cross sectional area
136	LE	38.2		38.2	mm	Core magnetic path length
137	AL	7200		7200	nH	Ungapped core effective inductance per turns squared
138	VE	3934		3934	mm^3	Core volume
139	BOBBIN NAME	ATQ Bobbin		ATQ Bobbin		Bobbin name
140	AW	29.5		29.5	mm^2	Bobbin window area
141	BW	15.20		15.20	mm	Bobbin width
142	MARGIN			0.0	mm	Bobbin safety margin
144	**PRIMARY WINDING**					
145	NPRIMARY			28		Primary winding number of turns
146	BPEAK			3386	Gauss	Peak flux density
147	BMAX			2983	Gauss	Maximum flux density
148	BAC			1491	Gauss	AC flux density (0.5 x Peak to Peak)

149	ALG			471	nH	Typical gapped core effective inductance per turns squared
150	LG			0.257	mm	Core gap length
151	LAYERS_PRIMARY			1		Primary winding number of layers
152	AWG_PRIMARY			25		Primary wire gauge
153	OD_PRIMARY_INSULATED			0.518	mm	Primary wire insulated outer diameter
154	OD_PRIMARY_BARE			0.455	mm	Primary wire bare outer diameter
155	CMA_PRIMARY			418.1	Cmils/A	Primary winding wire CMA
157	**SECONDARY WINDING**					
158	NSECONDARY			4		Secondary winding number of turns
159	AWG_SECONDARY			19		Secondary wire gauge
160	OD_SECONDARY_INSULATED			1.217	mm	Secondary wire insulated outer diameter
161	OD_SECONDARY_BARE			0.912	mm	Secondary wire bare outer diameter
162	CMA_SECONDARY			224.8	Cmils/A	Secondary winding wire CMA
164	**BIAS WINDING**					
165	NBIAS			8		Bias winding number of turns
169	**PRIMARY COMPONENTS SELECTION**					
170	**LINE UNDERVOLTAGE**					
171	BROWN-IN REQURED			80.00	V	Required line brown-in threshold
172	RLS			4.00	MΩ	Connect two 2 MOhm resistors to the V-pin for the required UV/OV threshold
173	BROWN-IN ACTUAL			80.16	V	Actual brown-in threshold using standard resistors
174	BROWN-OUT ACTUAL			72.50	V	Actual brown-out threshold using standard resistors
176	**LINE OVERVOLTAGE**					
177	OVERVOLTAGE_LINE		Warning	334.21	V	The device voltage stress will be higher than 650V when overvoltage is trigerred
179	**BIAS WINDING**					
180	VBIAS			9.00	V	Rectified bias voltage at the lowest output set-point
181	VF_BIAS			0.70	V	Bias winding diode forward drop
182	VREVERSE_BIASDIODE			61.93	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
183	CBIAS			22	uF	Bias winding rectification capacitor
184	CBPP			0.47	uF	BPP pin capacitor
188	**SECONDARY COMPONENTS SELECTION**					
189	RECTIFIER					
190	VDRAIN_OFF_SRFET			46.46	V	Secondary rectifier reverse voltage (not accounting parasitic voltage ring)
191	SRFET	AONS62922		AONS62922		Secondary rectifier (Logic MOSFET)
192	VBREAKDOWN_SRFET			120	V	Secondary rectifier breakdown voltage
193	RDSON_SRFET			7.0	mΩ	SRFET on time drain resistance at 25degC for VGS=4.4V

10 Performance Data

Note: 1. Tests made on open frame board without adapter case and heat spreader.
2. Output voltage measured on the PCB.
3. Measurements taken at room temperature ambient (approximately 25 °C).

10.1 *No-Load Input Power*

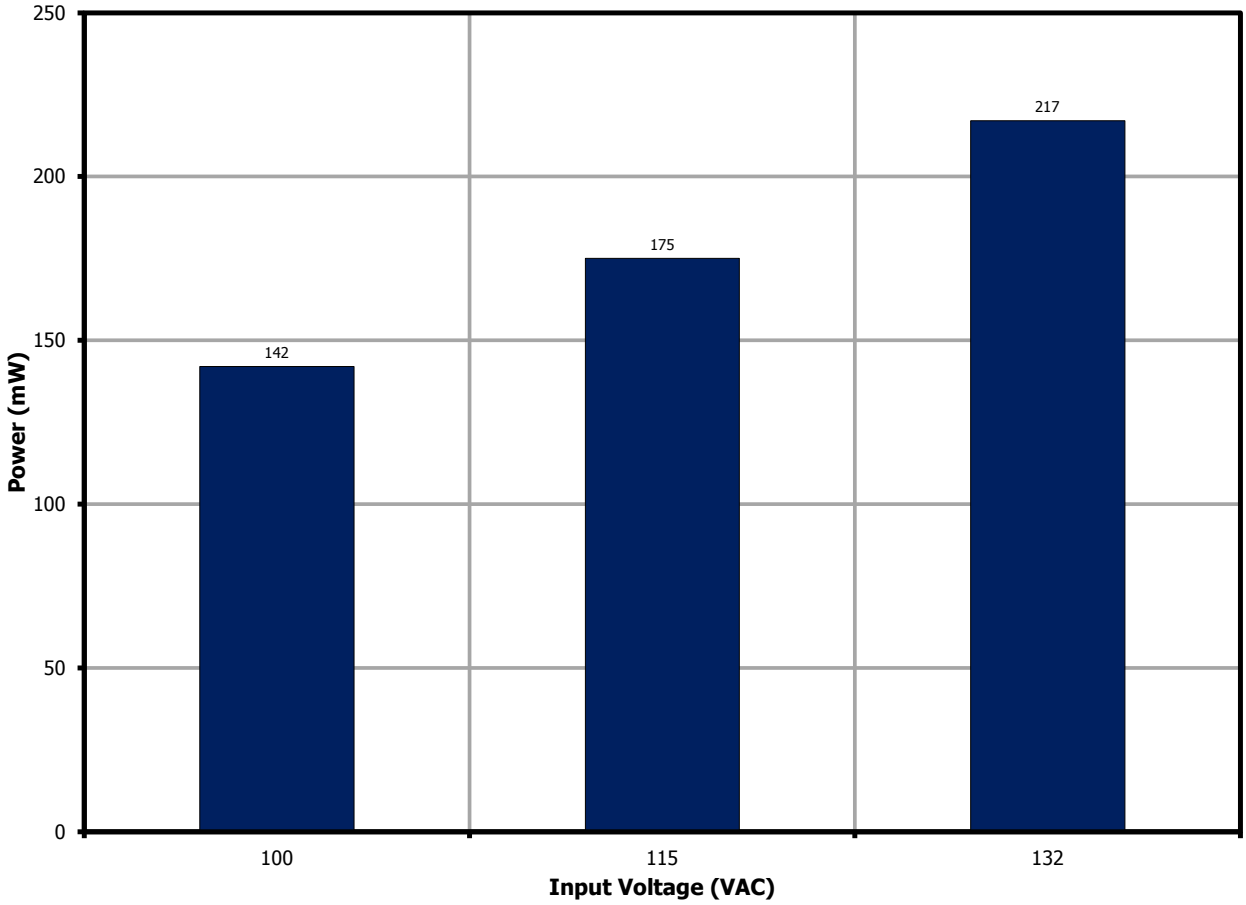


Figure 25 – No-Load Input Power vs. Input Line Voltage.

10.2 *Average and 10% Load Efficiency*

10.2.1 Efficiency Requirements

		Test	Average	Average	10% Load
		Effective	2016	Jan-16	Jan-16
V_{OUT} (V)	Model (V)	Power (W)	New EISA2007	CoC v5 Tier 2	CoC v5 Tier 2
5	<6	15	84.25%	85.00%	75.47%
9	>6	27	87.73%	88.85%	78.85%
12	>6	36	87.73%	88.85%	78.85%
15	>6	45	87.73%	88.85%	78.85%
20	>6	60	87.73%	88.85%	78.85%

10.2.2 Efficiency Performance Summary (On Board)

V_{OUT}	Power	Average Efficiency (%)	10% Load Efficiency (%)
(V)	(W)	115 VAC	
5	15	91.77	87.01
9	27	92.37	87.28
12	36	92.42	86.95
15	45	92.38	86.45
20	65	92.25	86.24

10.2.3 Average and 10% Load Efficiency Measurements

10.2.3.1 Output: 5 V / 3 A

Input (VAC)	Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)	DOE6 Requirement (%)	CoC v5 Tier 2 Requirement (%)	Remarks
115	100	14.96	92.19	**91.77**	**84.25**	**85.00**	**PASS**
	75	11.25	92.25				
	50	7.51	91.88				
	25	3.75	90.74				
	10	1.50	**87.01**			**75.47**	**PASS**

10.2.3.2 Output: 9 V / 3 A

Input (VAC)	Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)	DOE6 Requirement (%)	CoC v5 Tier 2 Requirement (%)	Remarks
115	100	27.12	92.87	**92.37**	**87.73**	**88.85**	**PASS**
	75	20.34	92.78				
	50	13.57	92.52				
	25	6.77	91.32				
	10	2.71	**87.28**			**78.85**	**PASS**

10.2.3.3 Output: 12 V / 3 A

Input (VAC)	Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)	DOE6 Requirement (%)	CoC v5 Tier 2 Requirement (%)	Remarks
115	100	36.17	92.98	**92.42**	**87.73**	**88.85**	**PASS**
	75	27.13	92.86				
	50	18.10	92.57				
	25	9.04	91.28				
	10	3.61	**86.95**			**78.85**	**PASS**

10.2.3.4 Output: 15 V / 3 A

Input (VAC)	Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)	DOE6 Requirement (%)	CoC v5 Tier 2 Requirement (%)	Remarks
115	100	45.19	92.98	**92.38**	**87.73**	**88.85**	**PASS**
	75	33.91	92.87				
	50	22.61	92.53				
	25	11.30	91.12				
	10	4.51	**86.45**			**78.85**	**PASS**

10.2.3.5 Output: 20 V / 3.25 A

Input (VAC)	Load (%)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)	DOE6 Requirement (%)	CoC v5 Tier 2 Requirement (%)	Remarks
115	100	65.17	92.87	**92.25**	**87.73**	**88.85**	**PASS**
	75	48.89	92.80				
	50	32.61	92.40				
	25	16.30	90.93				
	10	6.51	**86.24**			**78.85**	**PASS**

10.3 *Efficiency Across Line at 100% Load (On Board)*

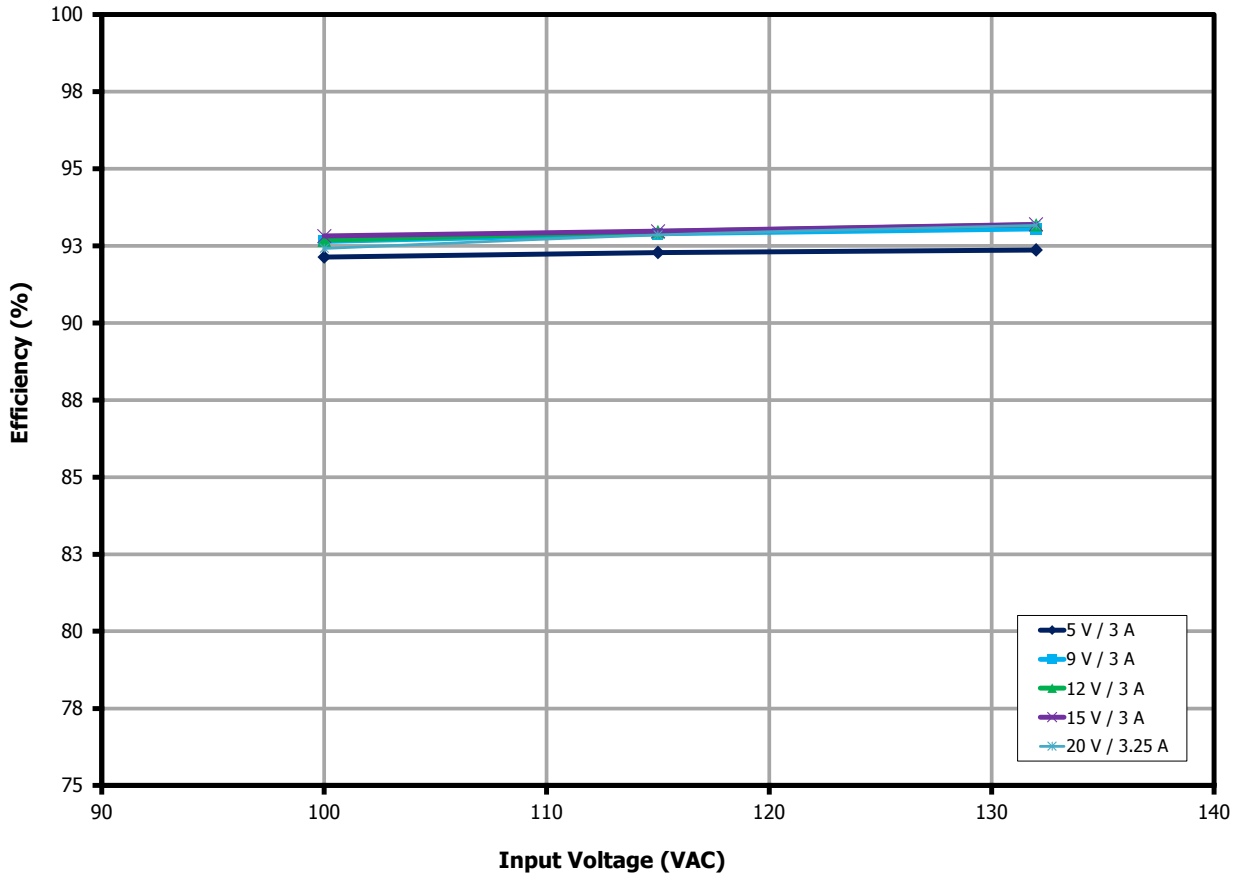


Figure 26 – Full Load Efficiency vs. Input Line for 5 V, 9 V, 12 V, 15 V, and 20 V Output, Room Temperature.

10.4 *Efficiency Across Load (On Board)*

10.4.1 Output: 5 V / 3 A

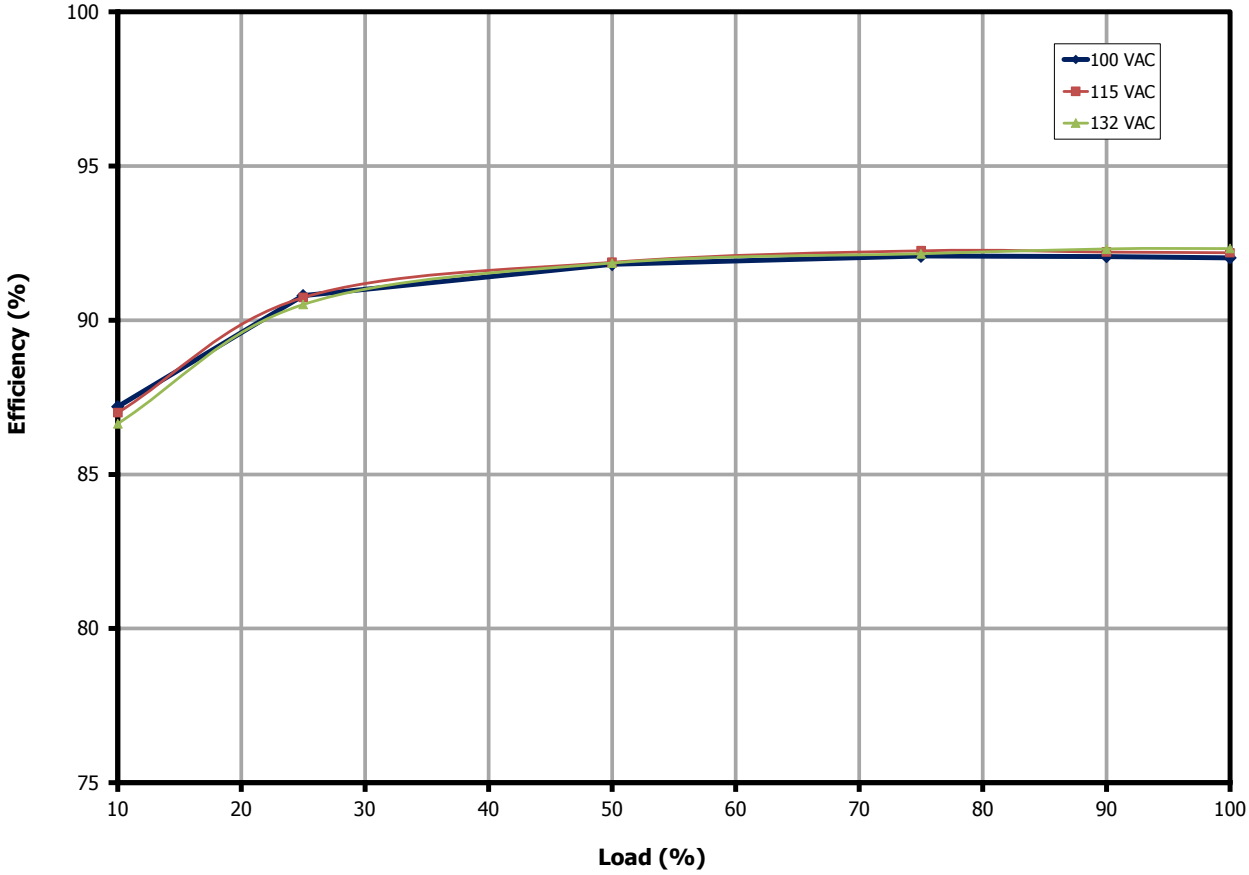


Figure 27 – Efficiency vs. Load for 5 V Output, Room Temperature.

10.4.2 Output: 9 V / 3 A

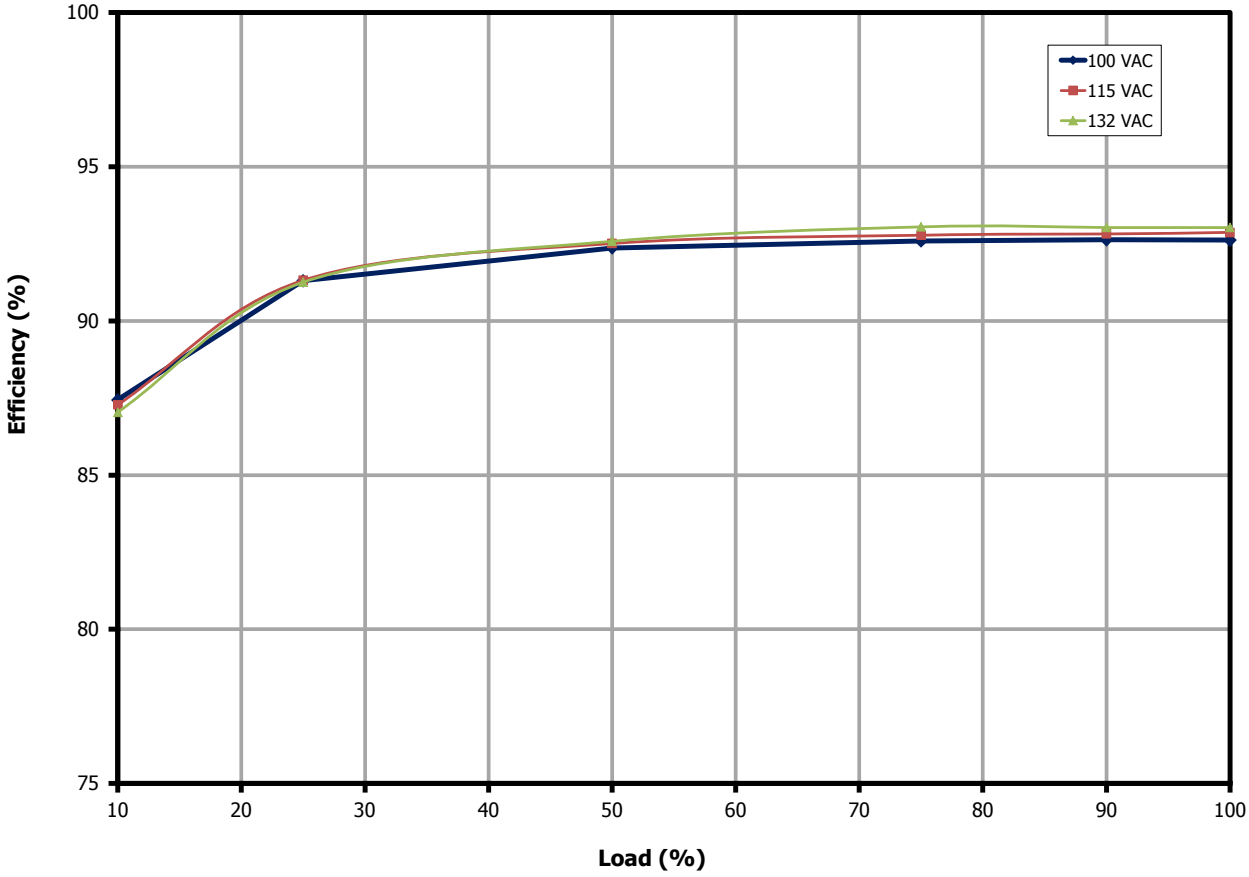


Figure 28 – Efficiency vs. Load for 9 V Output, Room Temperature.

10.4.3 Output: 12 V / 3 A

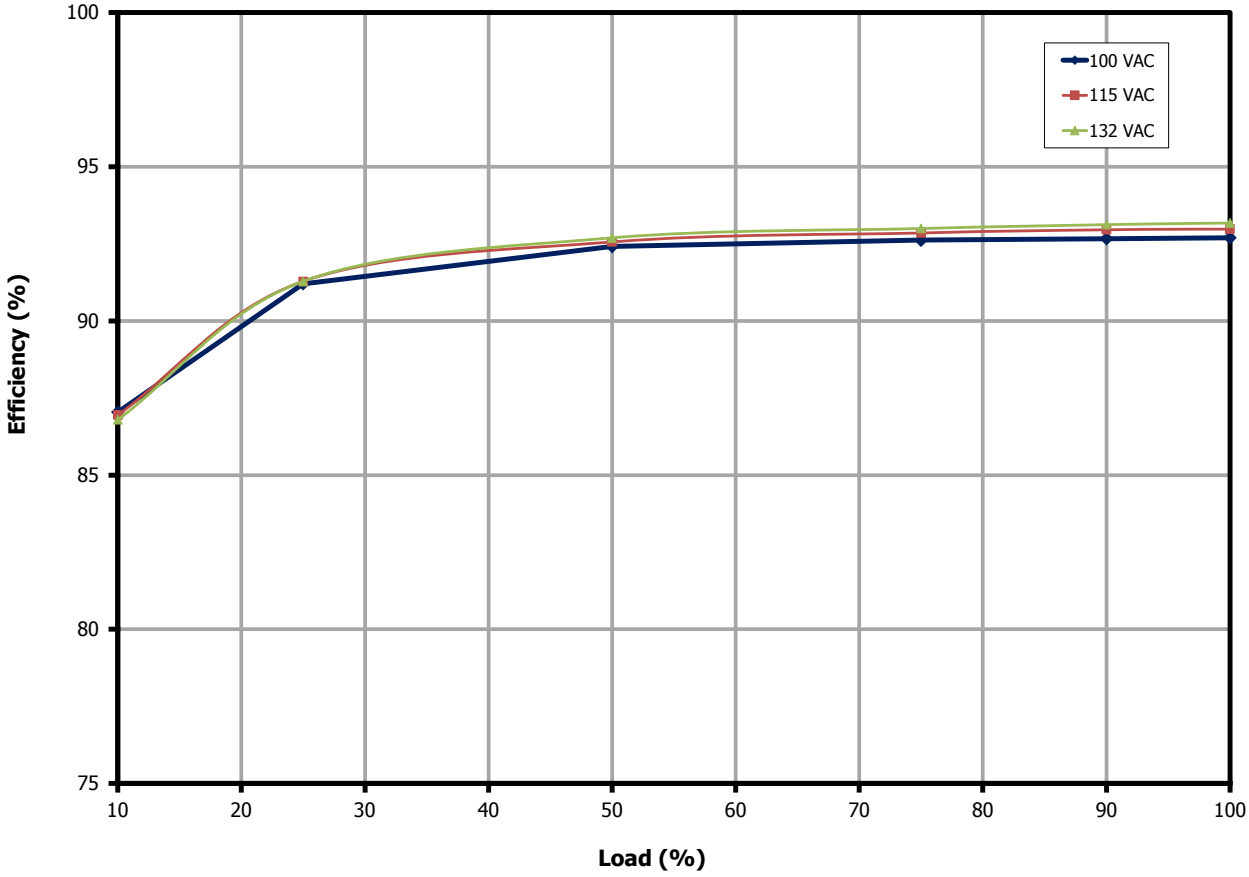


Figure 29 – Efficiency vs. Load for 12 V Output, Room Temperature.

10.4.4 Output: 15 V / 3 A

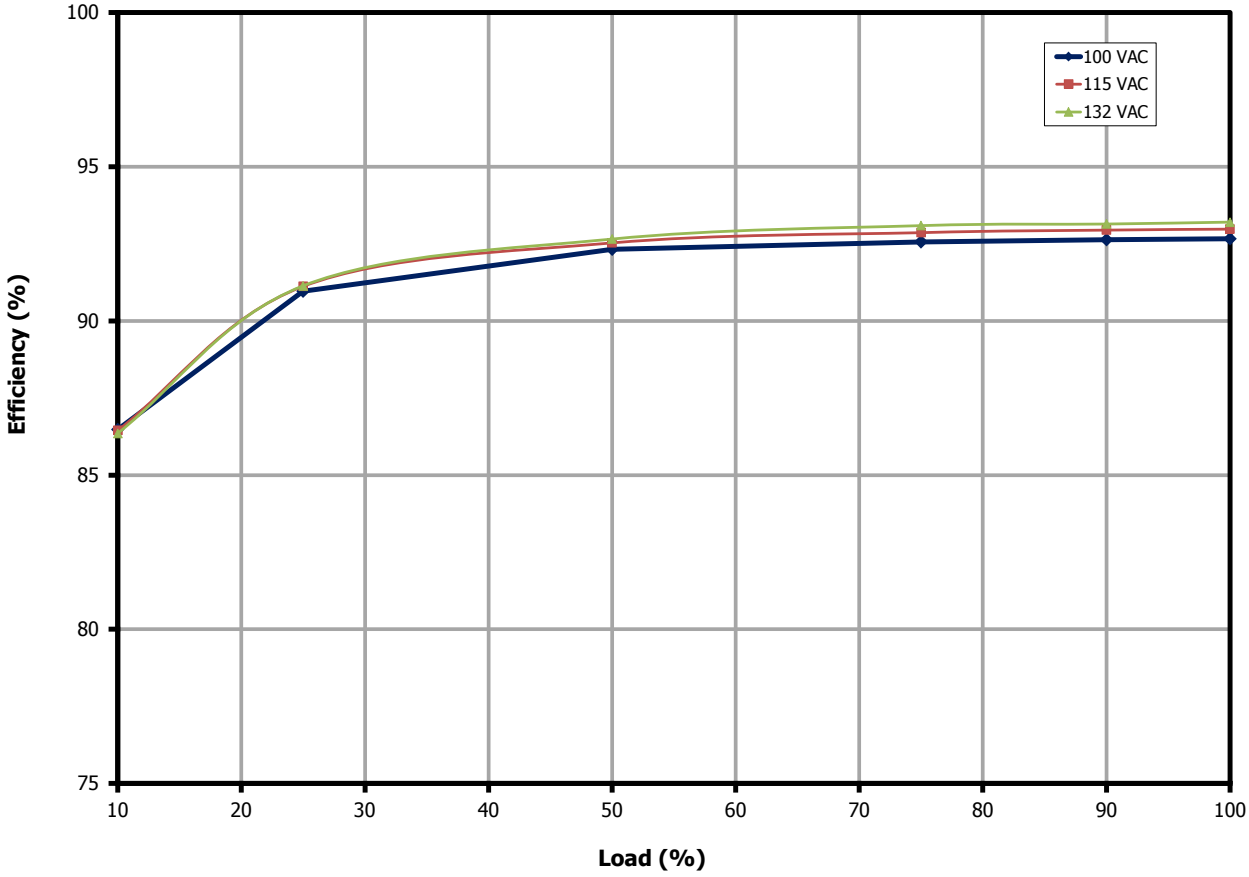


Figure 30 – Efficiency vs. Load for 15 V Output, Room Temperature.

10.4.5 Output: 20 V / 3.25 A

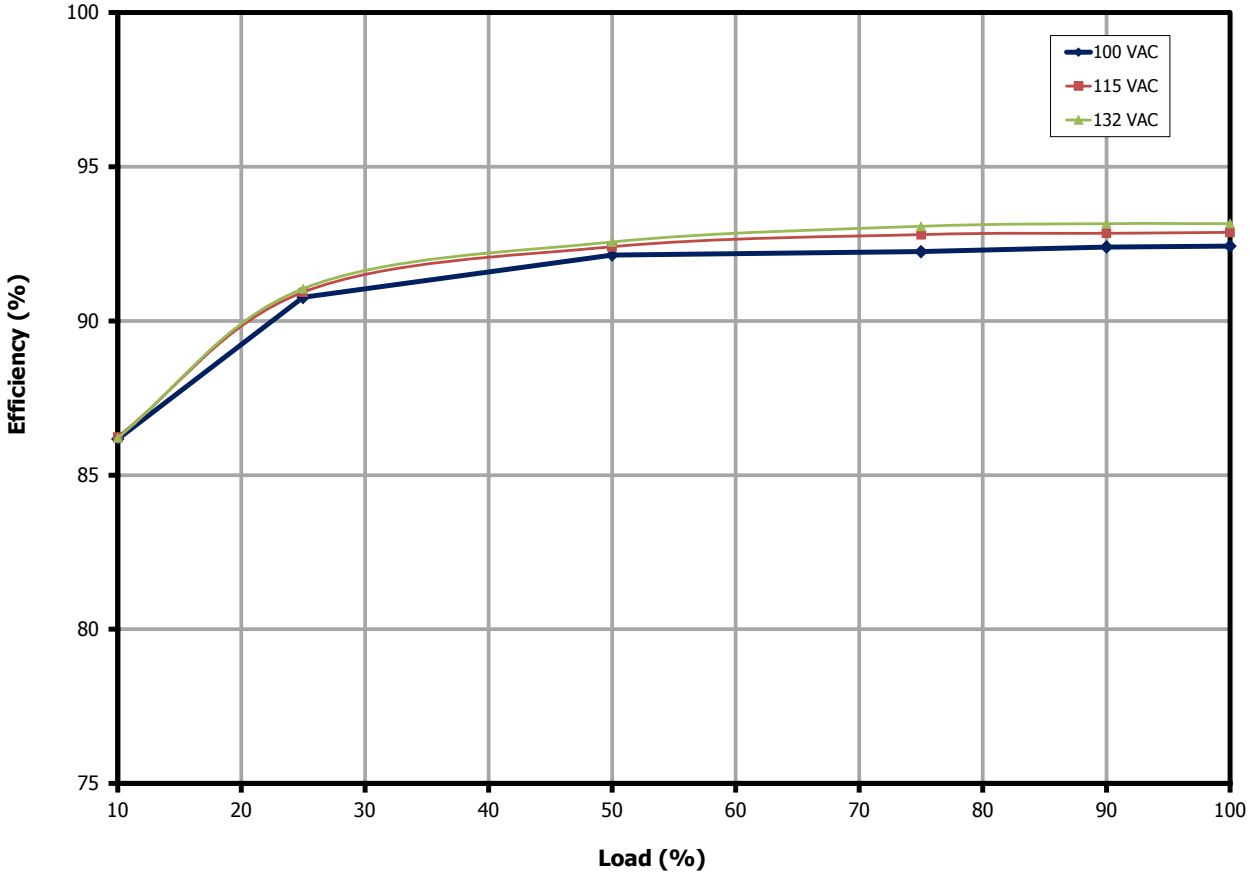


Figure 31 – Efficiency vs. Load for 20 V Output, Room Temperature.

10.4.6 Dual Output Mode Efficiency Spread

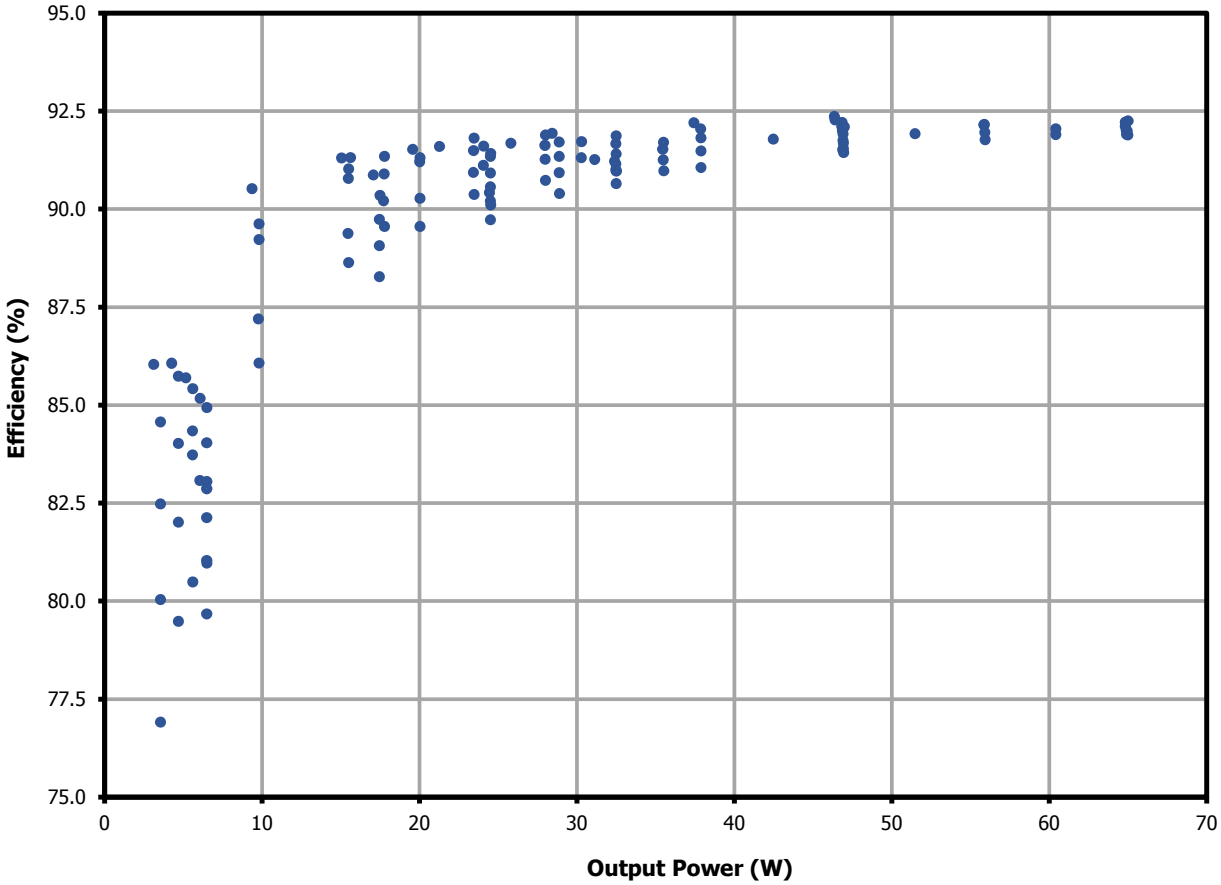


Figure 32. DER-916 Efficiency vs Load across various combinations of Vout and Iout at 115 VAC Input

10.5 *Load Regulation (On Board)*

10.5.1 Output: 5 V / 3 A

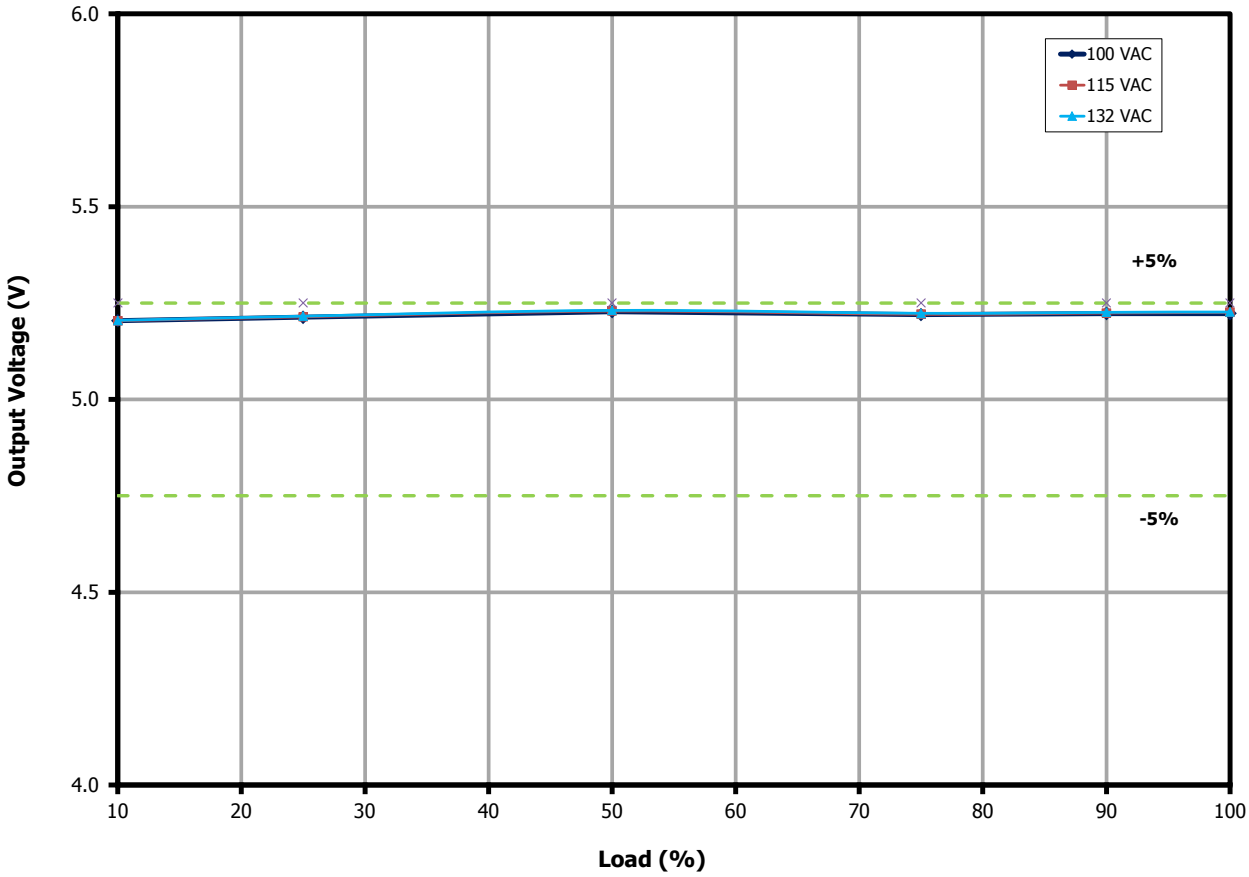


Figure 33 – Output Voltage vs. Output Load for 5 V Output, Room Temperature.

10.5.2 Output: 9 V / 3 A

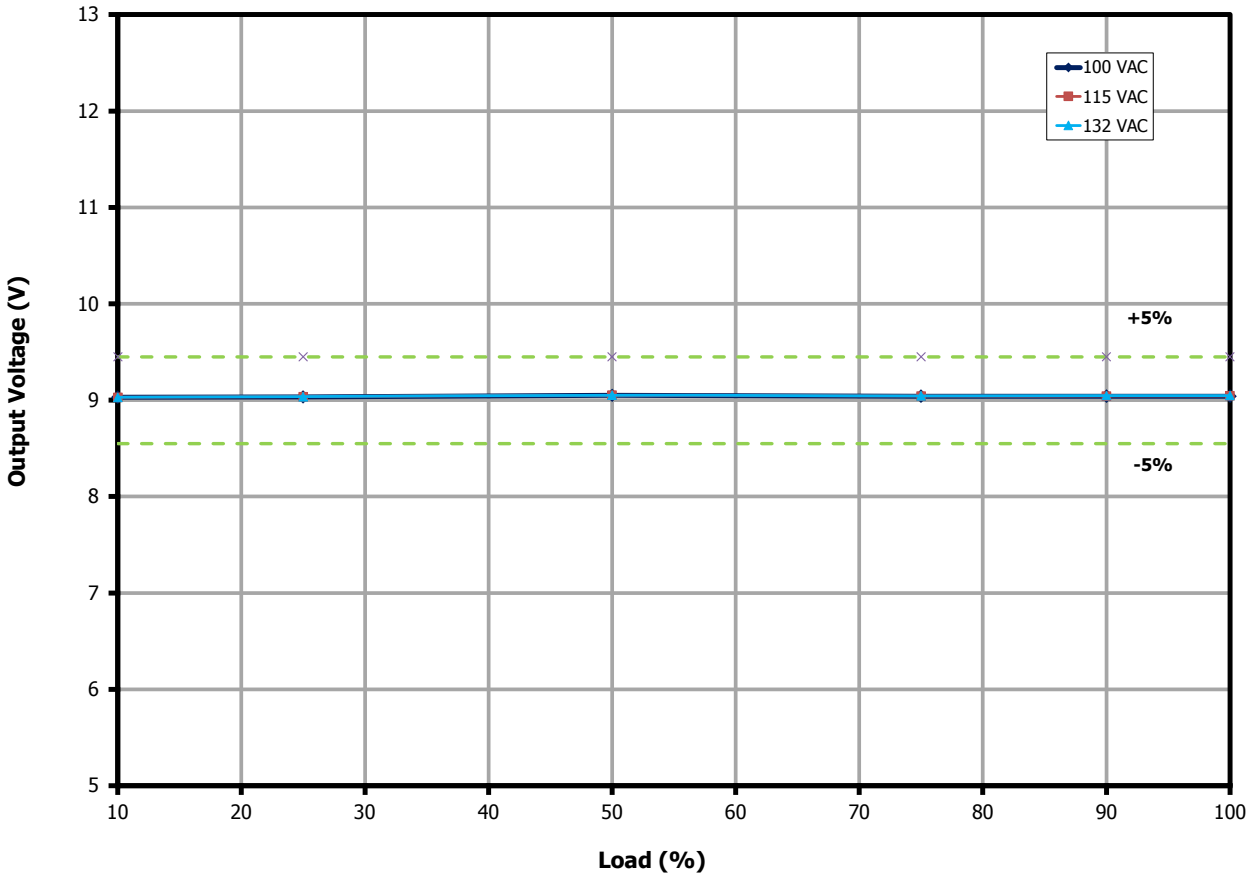


Figure 34 – Output Voltage vs. Output Load for 9 V Output, Room Temperature.

10.5.3 Output: 12 V / 3 A

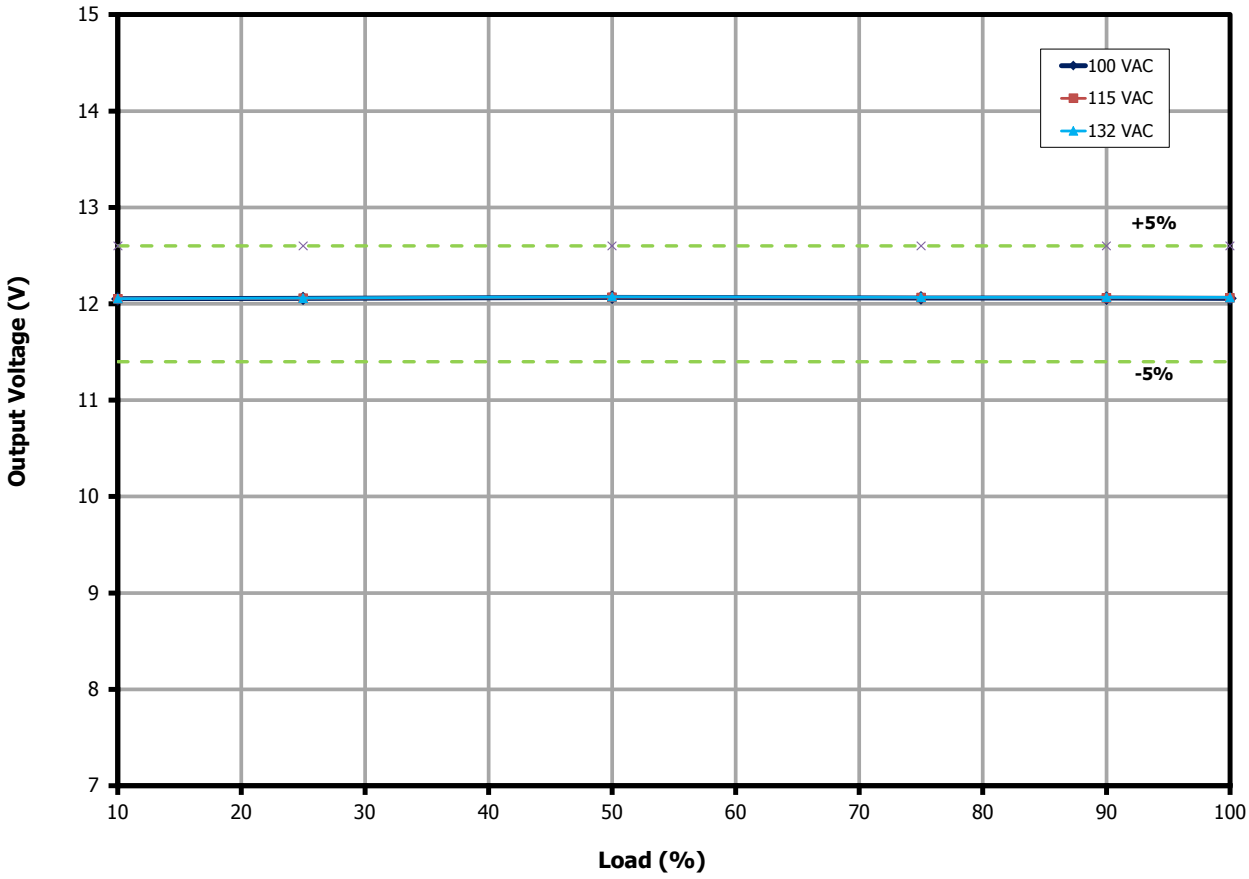


Figure 35 – Output Voltage vs. Output Load for 12 V Output, Room Temperature.

10.5.4 Output: 15 V / 3 A

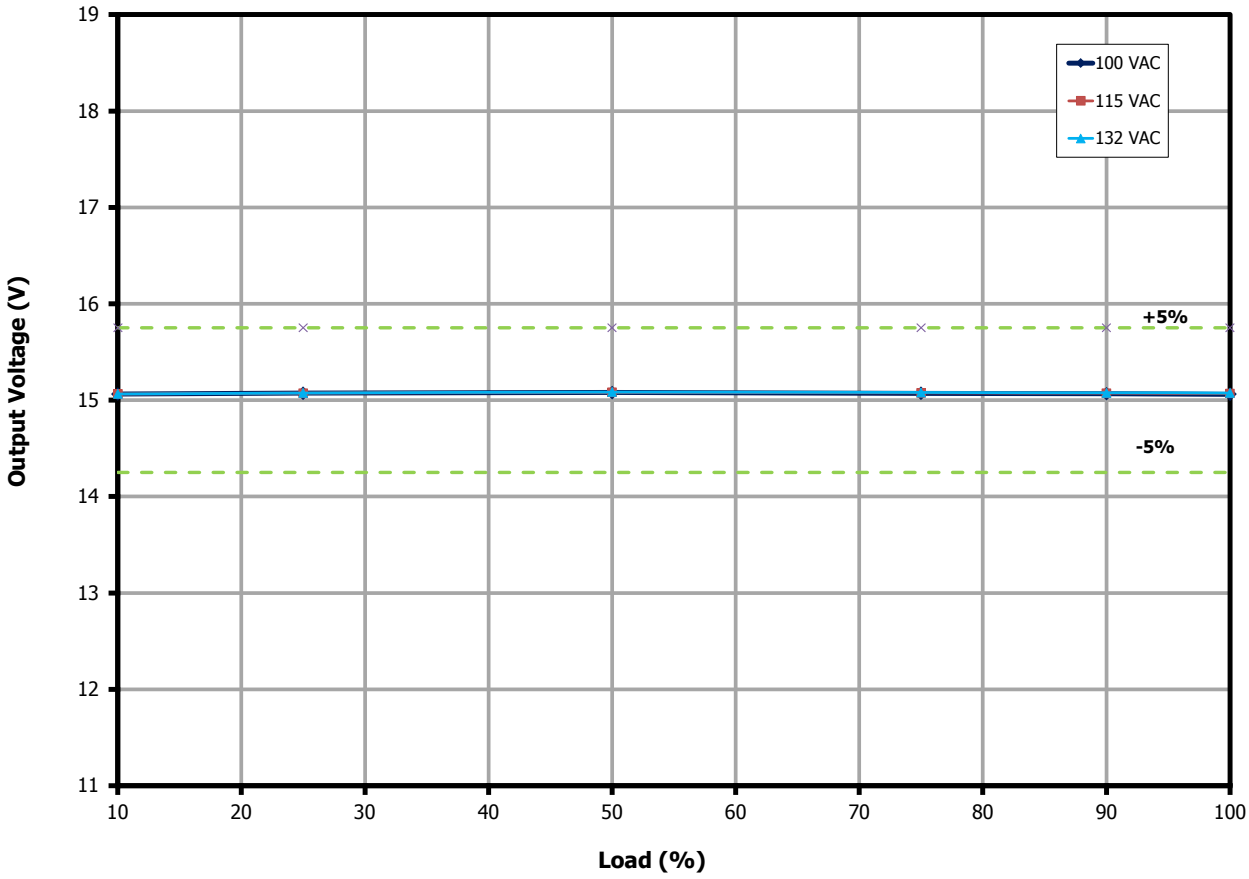


Figure 36 – Output Voltage vs. Output Load for 15 V Output, Room Temperature.

10.5.5 Output: 20 V / 3.25 A

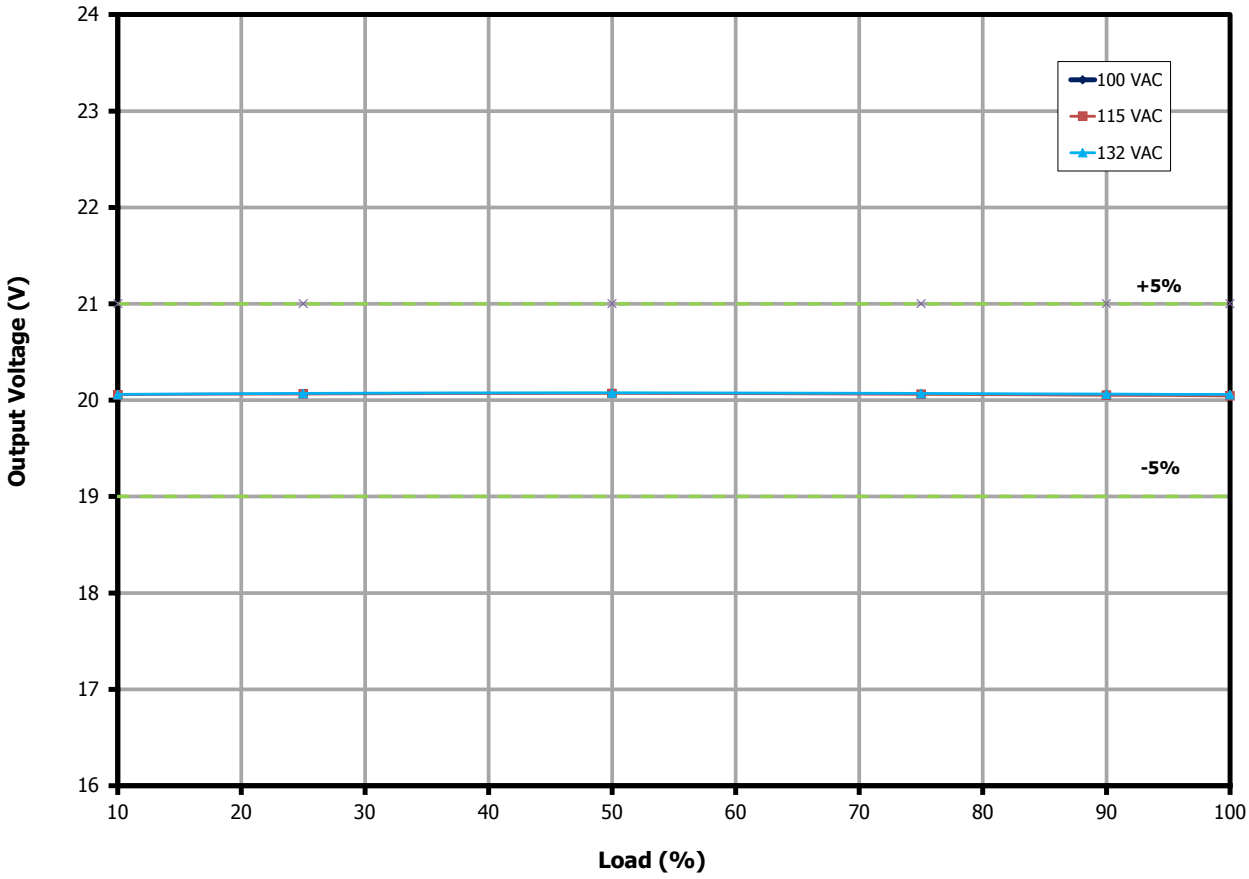


Figure 37 – Output Voltage vs. Output Load for 20 V Output, Room Temperature.

10.6 *Line Regulation (On Board)*

10.6.1 Output: 5 V / 3 A

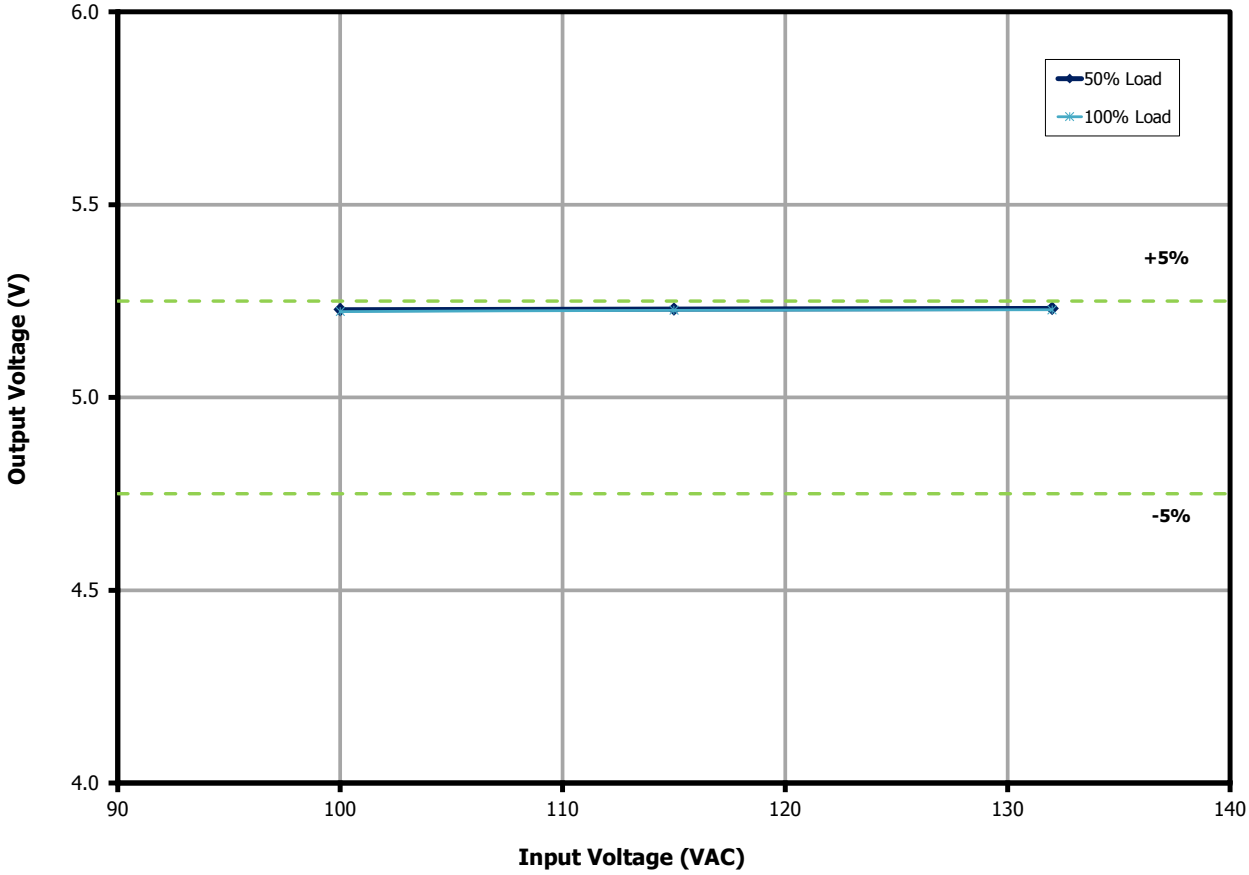


Figure 38 – Output Voltage vs. Input Line Voltage for 5 V Output, Room Temperature.

10.6.2 Output: 9 V / 3 A

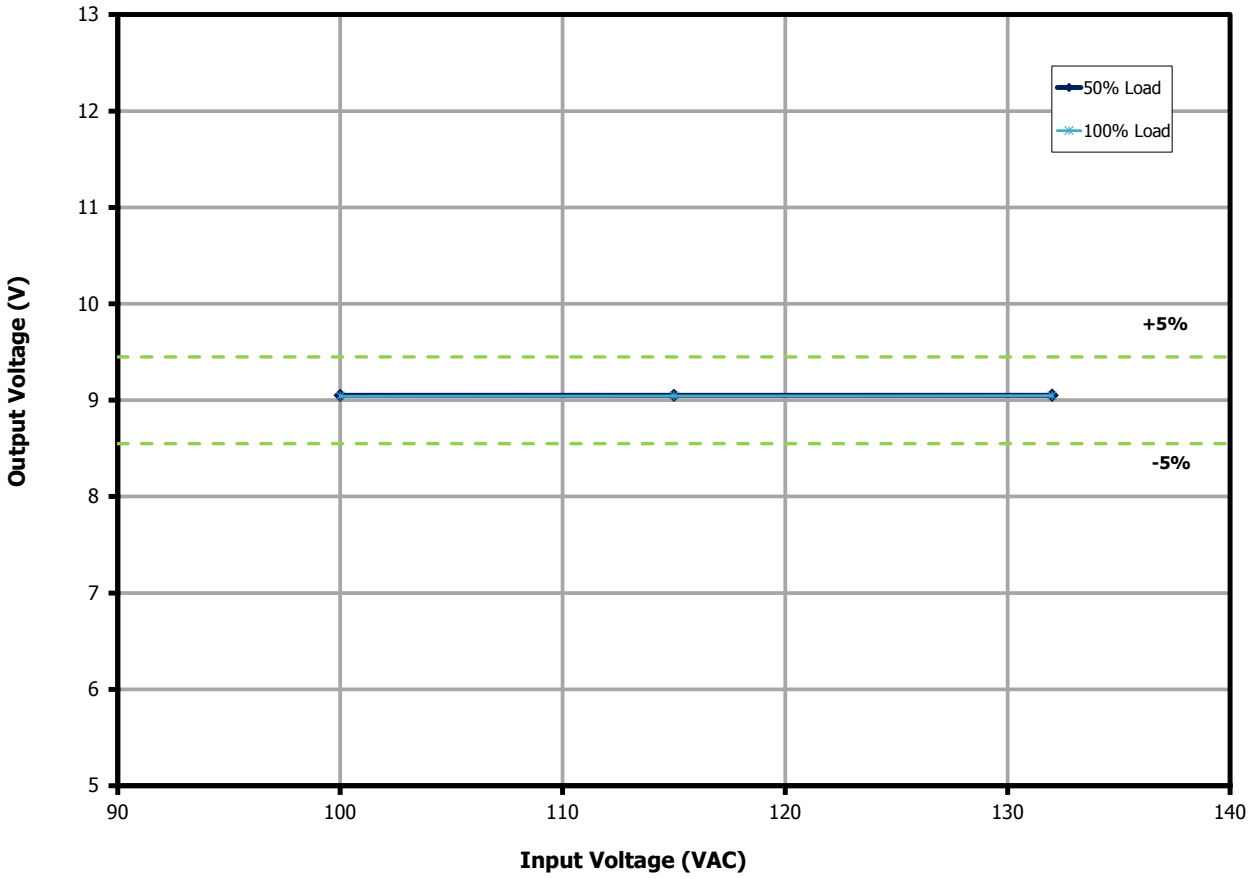


Figure 39 – Output Voltage vs. Input Line Voltage for 9 V Output, Room Temperature.

10.6.3 Output: 12 V / 3 A

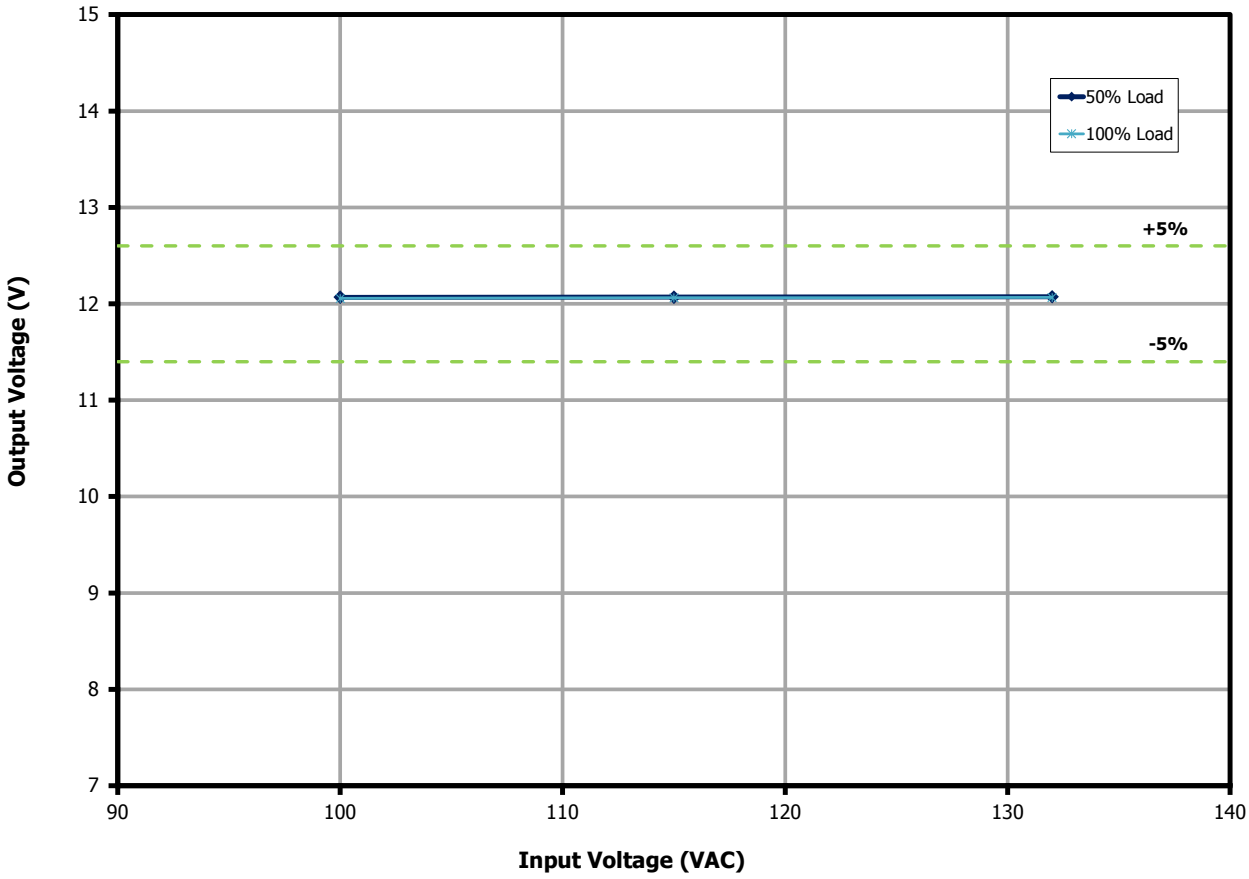


Figure 40 – Output Voltage vs. Input Line Voltage for 12 V Output, Room Temperature.

10.6.4 Output: 15 V / 3 A

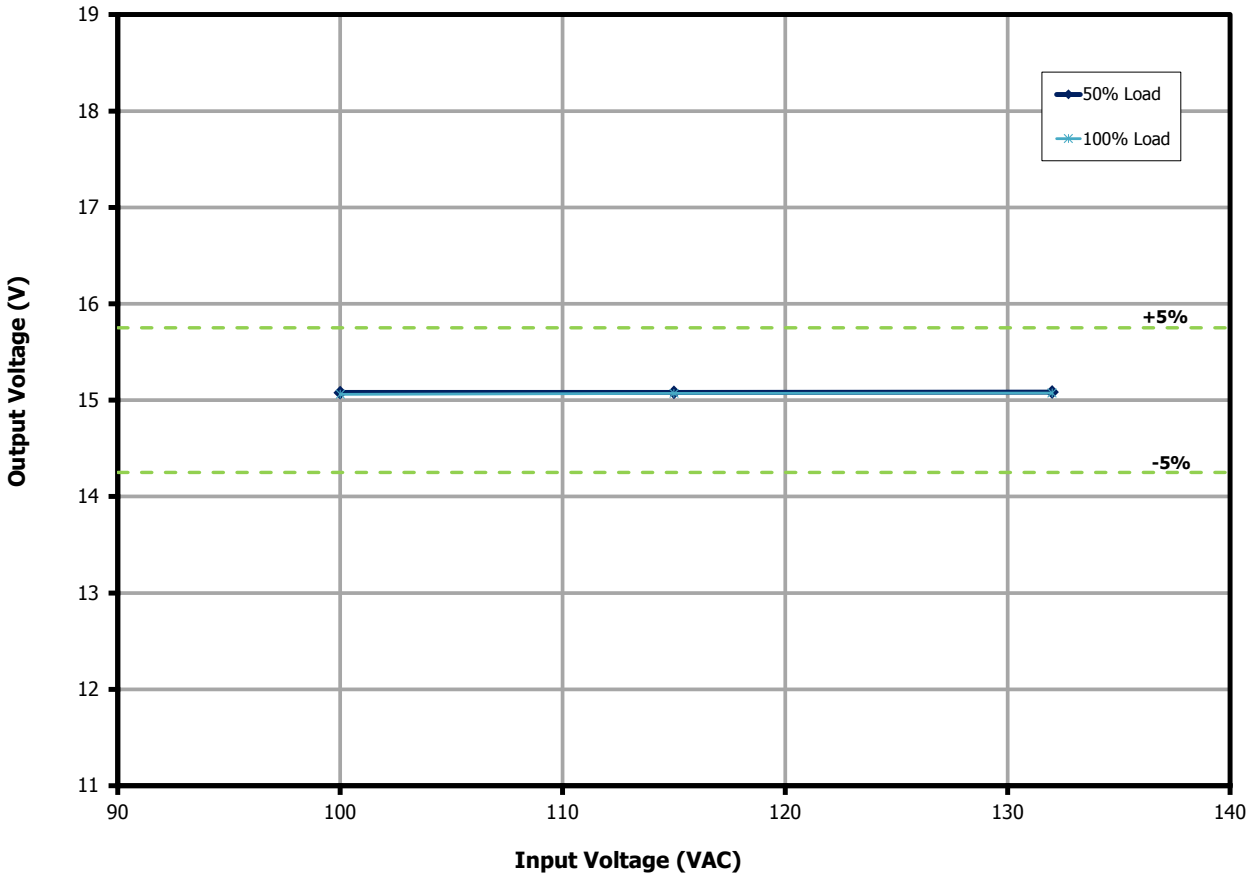


Figure 41 – Output Voltage vs. Input Line Voltage for 15 V Output, Room Temperature.

10.6.5 Output: 20 V / 3.25 A

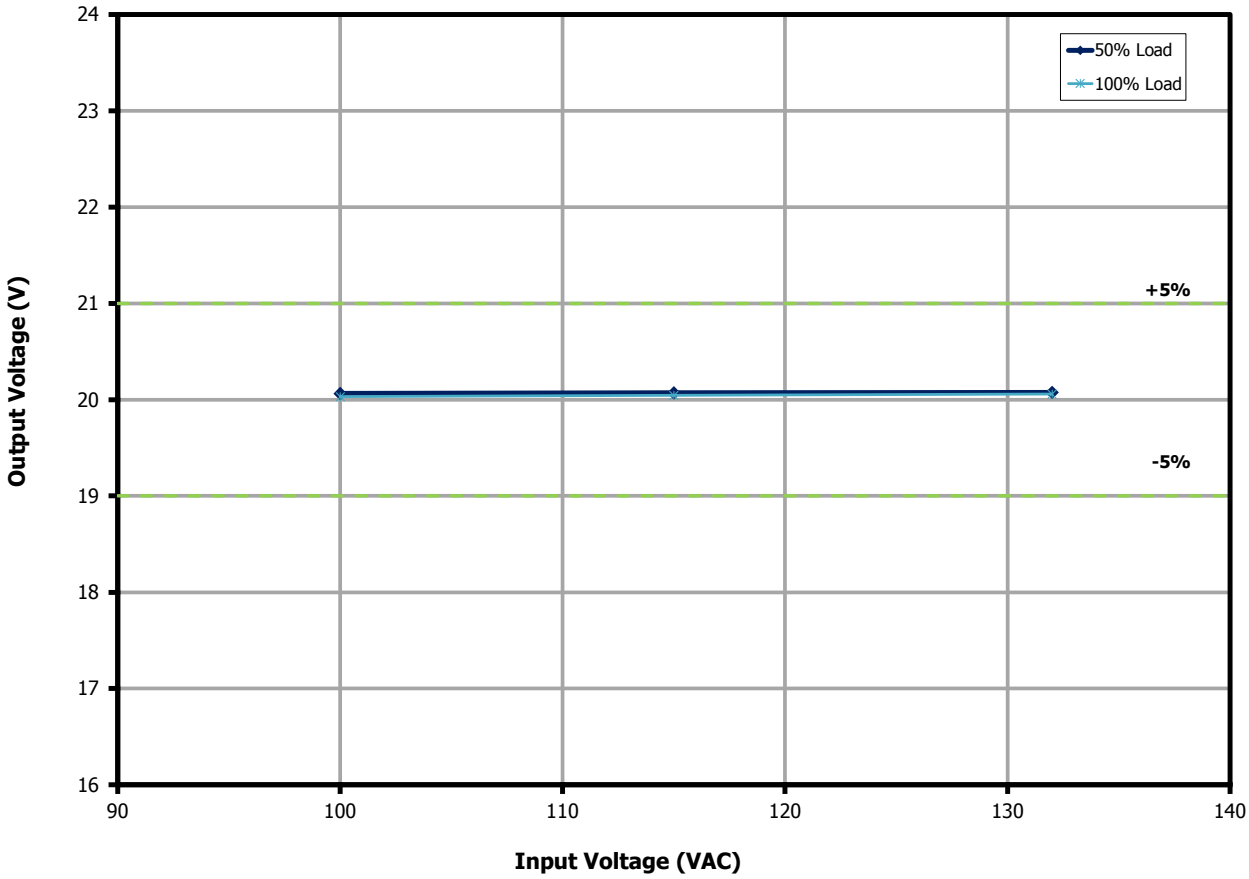


Figure 42 – Output Voltage vs. Input Line Voltage for 20 V Output, Room Temperature.

11 Thermal Performance

11.1 *Thermal Performance in Open Case*

Note: Measurements taken at room temperature ambient (approximately 25 °C).

11.1.1 Output: 65 W Single Port 20 V / 3.25 A (100 VAC)

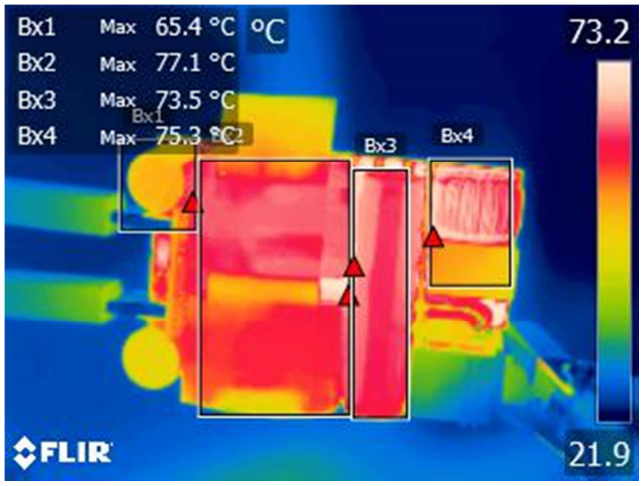


Figure 43 – Top Thermal Image.
Bx1: Output Capacitor, C_{OUT1} = 65.4 ºC.
Bx2: Transformer 1, T1 = 77.1 ºC.
Bx3: Input Capacitor, C_{IN} = 73.5 ºC.
Bx4: CMC, L1 = 75.3 ºC.

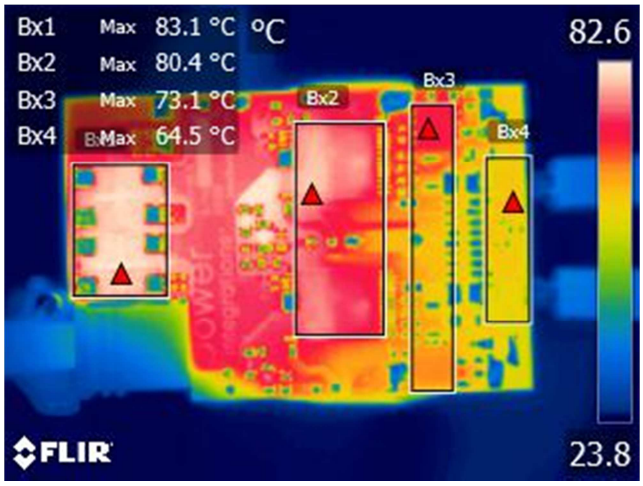


Figure 44 – Bottom Thermal Image.
Bx1: Bridge Rectifier, BR1 = 83.1 ºC.
Bx2: InnoSwitch3-Pro, U1 = 80.4 ºC.
Bx3: SR FET 1, Q2 = 73.1 ºC.
Bx4: Bus Switch, Q3 = 64.5 ºC

11.1.2 Output: 65 W Dual Port - Port A 20 V / 2.25 A and Port B 20 V / 1 A (100 VAC)

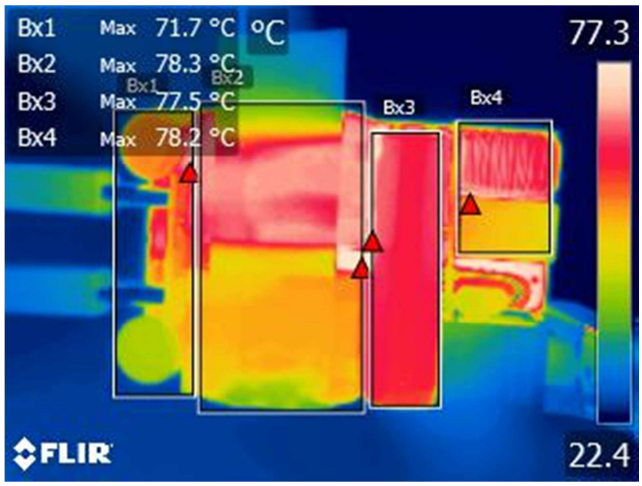


Figure 45 – Top Thermal Image.
Bx1: Output Capacitor, C_{OUT1} = 71.1 ºC.
Bx2: Transformer 1, T1 = 78.3 ºC.
Bx3: Input Capacitor, C_{IN} = 77.5 ºC.
Bx4: CMC, L1 = 78.2 ºC.

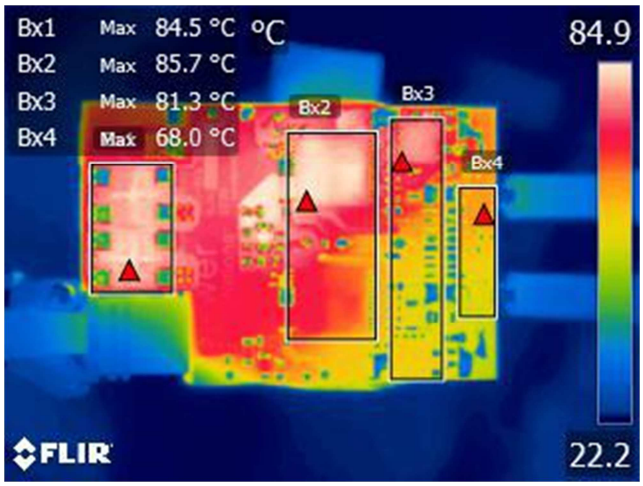


Figure 46 – Bottom Thermal Image.
Bx1: Bridge Rectifier, BR1 = 84.5 ºC.
Bx2: InnoSwitch3-Pro, U1 = 85.7 ºC.
Bx3: SR FET 1, Q2 = 81.3 ºC.
Bx4: Bus Switch, Q3 = 68.0 ºC.

11.2 *Thermal Performance, 50 ºC Ambient*

11.2.1 Components Temperature Summary

Condition	Component	Temperature (°C) 65 W Dual Port Port A: 20 V / 2.25 A Port B: 20 V / 1 A
No Enclosure 50 °C Ambient	INN3370 A	108.1
	INN3370 B	103
	SR A	97.1
	SR B	86.6
	Tx A	96.5
	Tx B	86.1
	C_{OUT} A	88.9
	C_{OUT} B	76.6
	C_{IN}	89.3
	Bridge	104.1
	CMC	98.3

11.2.2 Output: Port A 45 W 20 V / 2.25 A and Port B 20 W 20 V / 1 A (100 VAC)

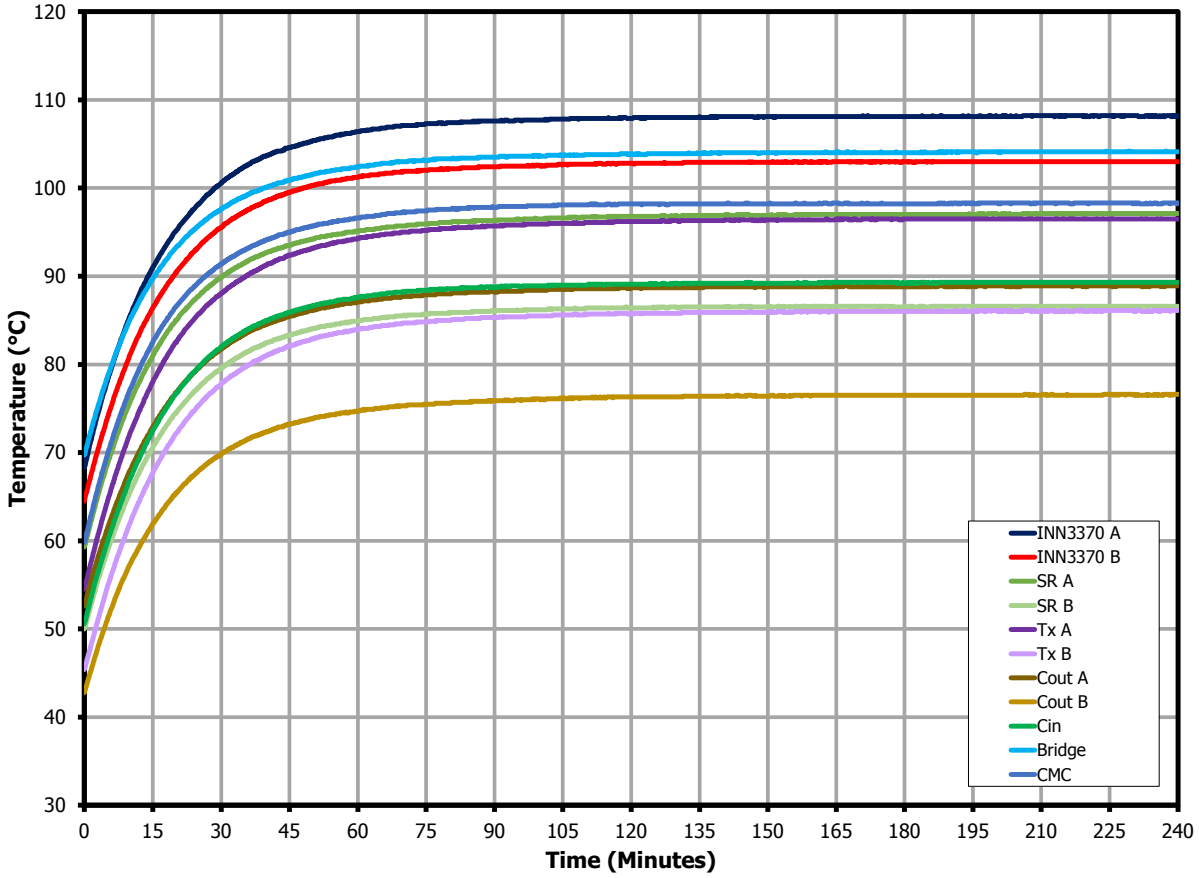


Figure 47 – Unit Thermal Performance at 65 W Dual Port Operation, 100 VAC, 50 °C Ambient.

12 Waveforms

Note: Waveforms taken at room temperature ambient (approximately 25 °C)

12.1 *Start-up Waveforms*

12.1.1 Output Voltage and Current

Note: Output voltage waveforms captured at the end of 100 mΩ cable.

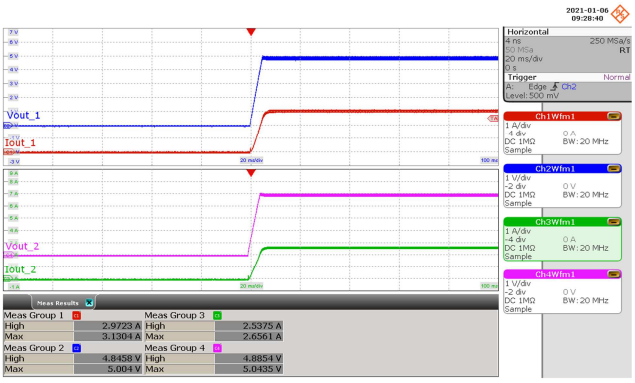


Figure 48 – Output Voltage and Current.
100 VAC, 5.0 V, 3 A Load (5.04 V_{MAX}).
CH2: V_{OUT1}, 1 V / div.
CH1: I_{LOAD1}, 1 A / div.
CH4: V_{OUT2}, 1 V / div.
CH3: I_{LOAD2}, 1 A / div.
Time: 20 ms / div.

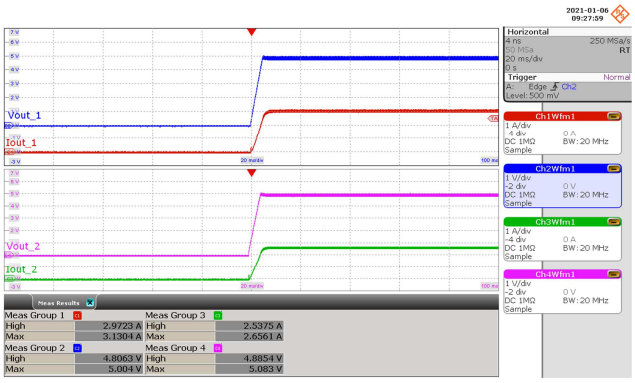


Figure 49 – Drain Voltage and Current.
132 VAC, 5.0 V, 3 A Load (5.08 V_{MAX}).
CH2: V_{OUT1}, 1 V / div.
CH1: I_{LOAD1}, 1 A / div.
CH4: V_{OUT2}, 1 V / div.
CH3: I_{LOAD2}, 1 A / div.
Time: 20 ms / div.

12.1.2 Primary Drain Voltage and Current

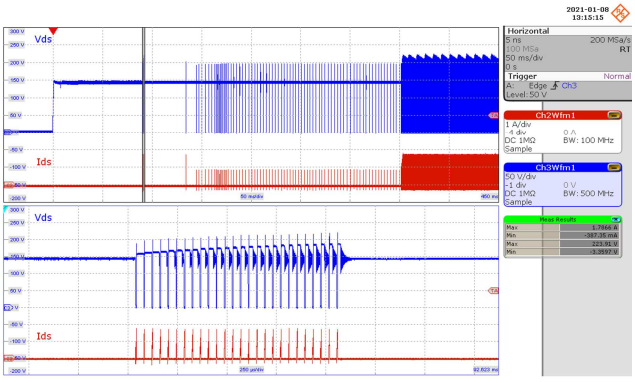


Figure 50 – Primary Drain Voltage and Current.
100 VAC, 5.0 V, 5 A Load (223.91 V_{MAX}).
CH3: V_{DRAIN}, 50 V / div.
CH2: I_{DRAIN}, 1 A / div.
Time: 50 ms / div. (250 µs / div. Zoom)

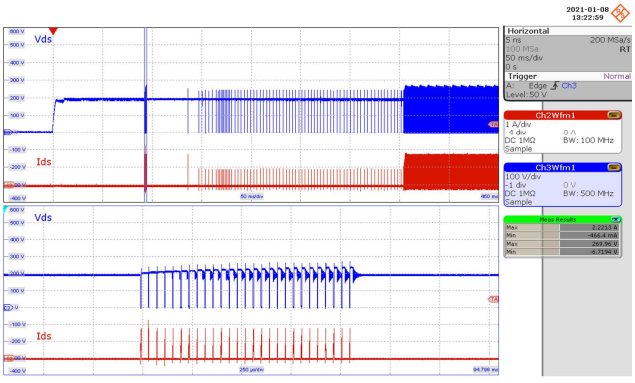


Figure 51 – Primary Drain Voltage and Current.
132 VAC, 5.0 V, 3 A Load (269.96 V_{MAX}).
CH3: V_{DRAIN}, 100 V / div.
CH2: I_{DRAIN}, 1 A / div.
Time: 50 ms / div. (250 µs / div. Zoom)

12.1.3 SR FET Drain Voltage and Current

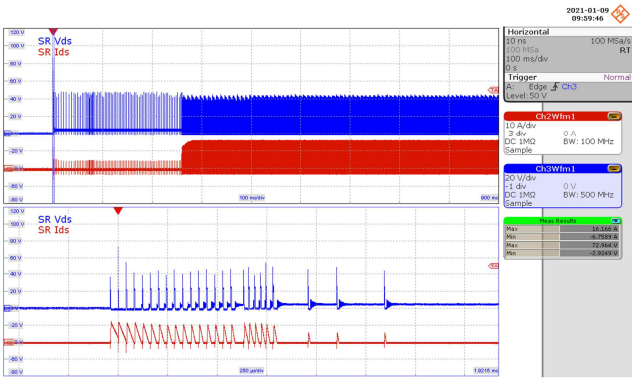


Figure 52 – SR FET Drain Voltage and Current.
100 VAC, 5.0 V, 3 A Load (72.964 V_{MAX}).
CH3: $V_{DRAIN(SR)}$, 20 V / div.
CH2: $I_{DRAIN(SR)}$, 10 A / div.
Time: 100 ms / div. (250 µs / div. Zoom)

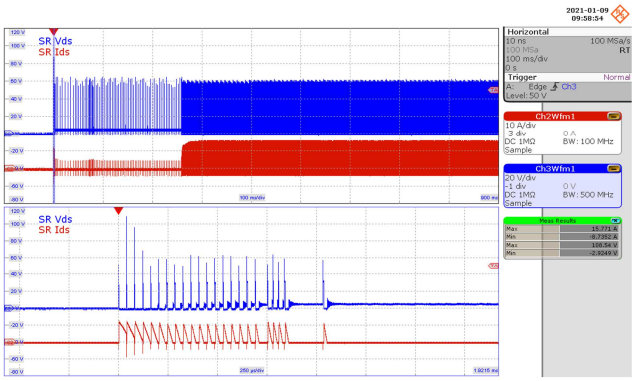


Figure 53 – SR FET Drain Voltage and Current.
132 VAC, 5.0 V, 3 A Load (108.54 V_{MAX}).
CH3: $V_{DRAIN(SR)}$, 20 V / div.
CH2: $I_{DRAIN(SR)}$, 10 A / div.
Time: 100 ms / div. (250 µs / div. Zoom)

12.2 *Load Transient Response*

Note: Output voltage waveforms captured on the PCB.

12.2.1 Output: 5 V / 3 A

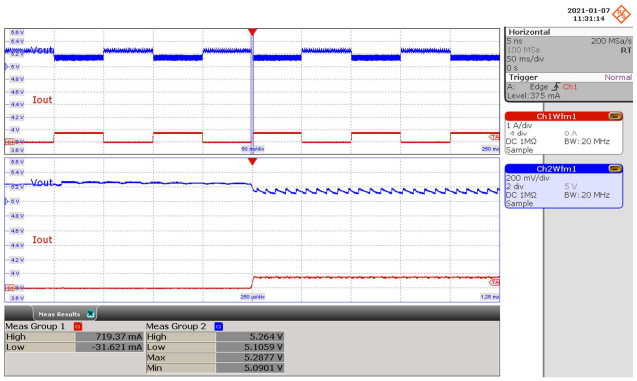


Figure 54 – Transient Response.
100 VAC, 5.0 V, 0 – 0.75 A Load Step.
V_{MIN}: 5.0901 V, V_{MAX}: 5.2877 V.
CH2: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (250 µs / div. Zoom)

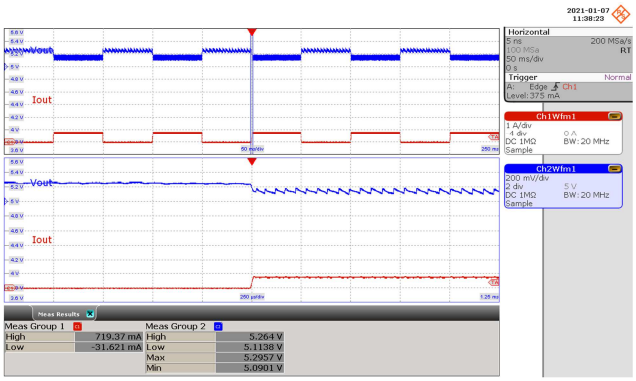


Figure 55 – Transient Response.
132 VAC, 5.0 V, 0 – 0.75 A Load Step.
V_{MIN}: 5.0901 V, V_{MAX}: 5.2957 V.
CH2: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (250 µs / div. Zoom)

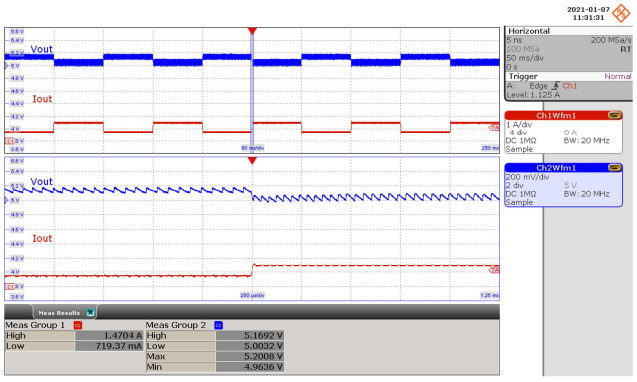


Figure 56 – Transient Response.
100 VAC, 5.0 V, 0.75 – 1.5 A Load Step.
V_{MIN}: 4.9636 V, V_{MAX}: 5.2008 V.
CH2: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (250 µs / div. Zoom)

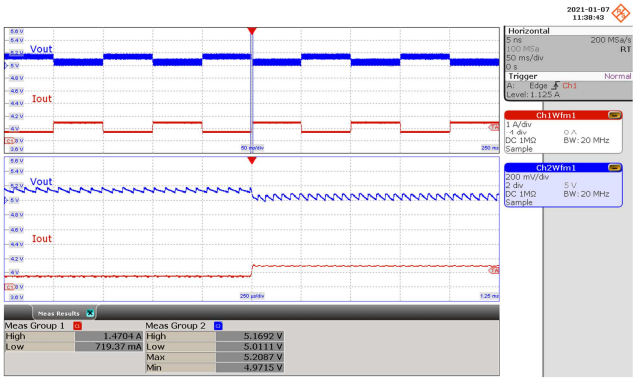


Figure 57 – Transient Response.
132 VAC, 5.0 V, 0.75 – 175 A Load Step.
V_{MIN}: 4.9715 V, V_{MAX}: 5.2087 V.
CH2: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (250 µs / div. Zoom)

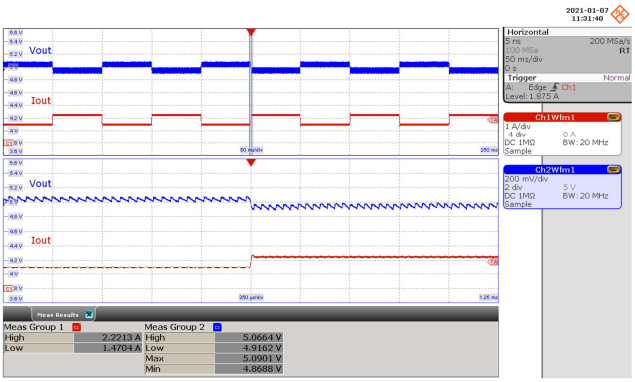


Figure 58 – Transient Response.
100 VAC, 5.0 V, 1.5 – 2.25 A Load Step.
V_{MIN}: 4.8688 V, V_{MAX}: 5.0901 V.
CH2: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (250 µs / div. Zoom)

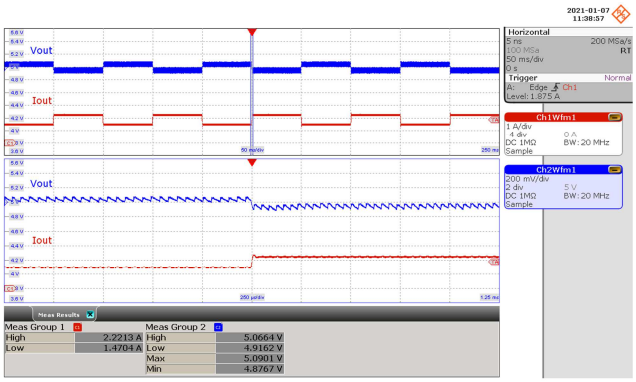


Figure 59 – Transient Response.
132 VAC, 5.0 V, 1.5 – 2.25 A Load Step.
V_{MIN}: 4.8767 V, V_{MAX}: 5.0901 V.
CH2: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (250 µs / div. Zoom)

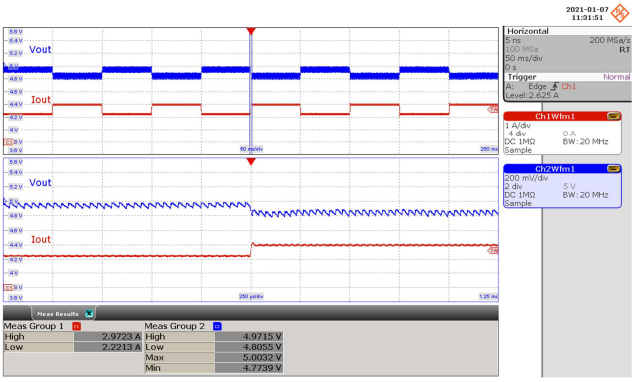


Figure 60 – Transient Response.
100 VAC, 5.0 V, 2.25 – 3.0 A Load Step.
V_{MIN}: 4.7739 V, V_{MAX}: 5.0032 V.
CH2: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (250 µs / div. Zoom)

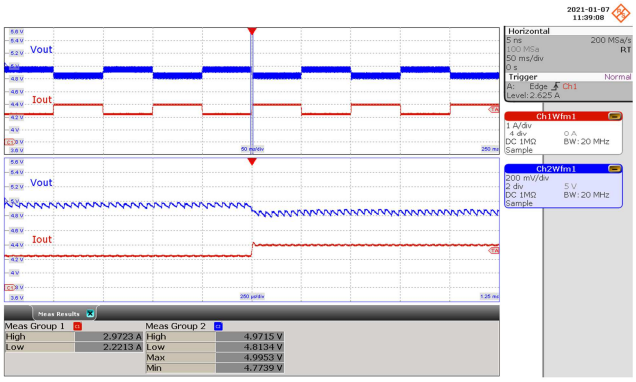


Figure 61 – Transient Response.
132 VAC, 5.0 V, 2.25 – 3.0 A Load Step.
V_{MIN}: 4.7739 V, V_{MAX}: 4.9953 V.
CH2: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (250 µs / div. Zoom)

12.2.2 Output: 9 V / 3 A

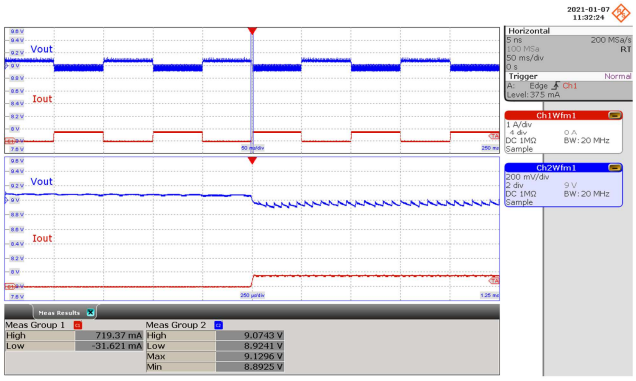


Figure 62 – Transient Response.
100 VAC, 9.0 V, 0 – 0.75 A Load Step.
V_{MIN}: 8.8925 V, V_{MAX}: 9.1296 V.
CH2: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (250 µs / div. Zoom)

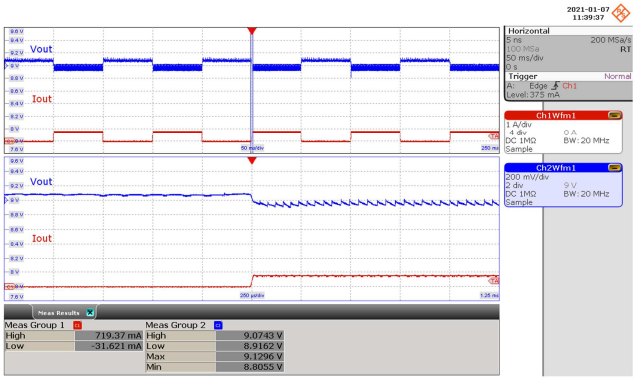


Figure 63 – Transient Response.
132 VAC, 9.0 V, 0 – 0.75 A Load Step.
V_{MIN}: 8.8055 V, V_{MAX}: 9.1296 V.
CH2: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (250 µs / div. Zoom)

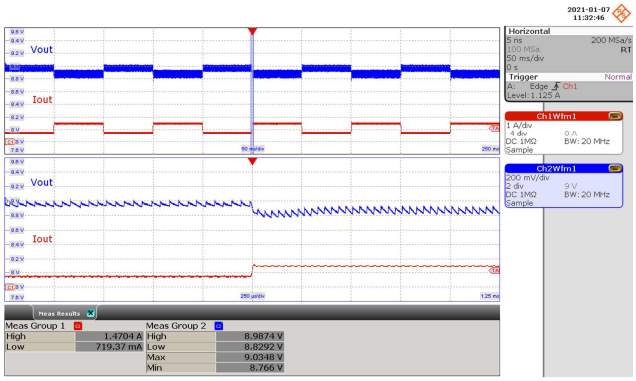


Figure 64 – Transient Response.
100 VAC, 9.0 V, 0.75 – 1.5 A Load Step.
V_{MIN}: 8.766 V, V_{MAX}: 9.0348 V.
CH2: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (250 µs / div. Zoom)

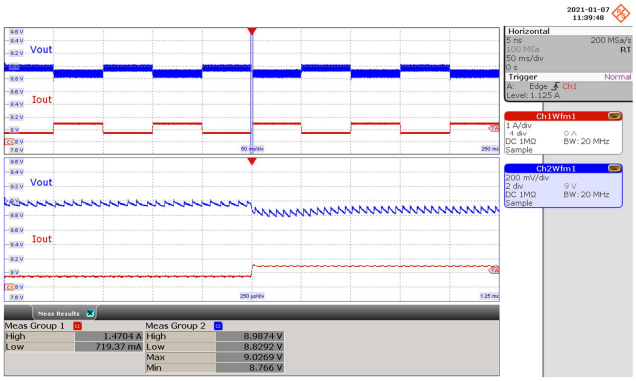


Figure 65 – Transient Response.
132 VAC, 9.0 V, 0 – 0.75 A Load Step.
V_{MIN}: 8.766 V, V_{MAX}: 9.0269 V.
CH2: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (250 µs / div. Zoom)

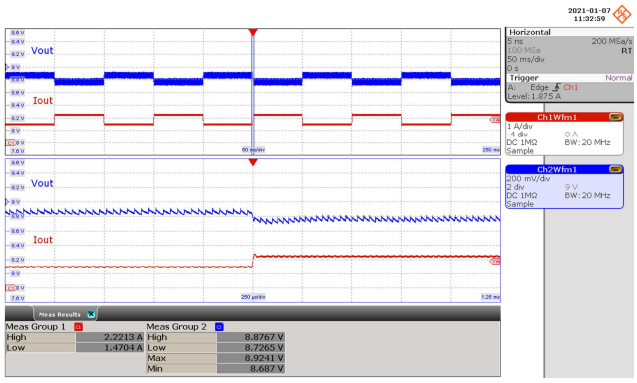


Figure 66 – Transient Response.
100 VAC, 9.0 V, 1.5 – 2.25 A Load Step.
V_{MIN}: 8.687 V, V_{MAX}: 8.9241 V.
CH2: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (250 µs / div. Zoom)

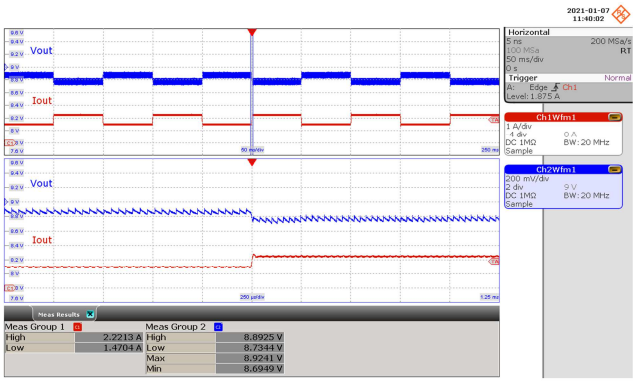


Figure 67 – Transient Response.
132 VAC, 9.0 V, 0 – 0.75 A Load Step.
V_{MIN}: 8.6949 V, V_{MAX}: 8.9241 V.
CH2: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (250 µs / div. Zoom)

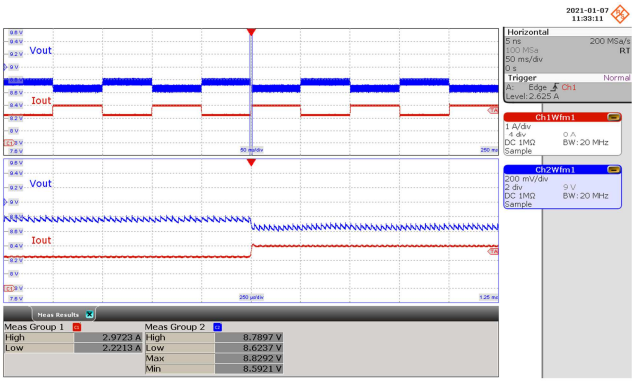


Figure 68 – Transient Response.
100 VAC, 9.0 V, 2.25 – 3.0 A Load Step.
V_{MIN}: 8.5921 V, V_{MAX}: 8.8292 V.
CH4: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (250 µs / div. Zoom)

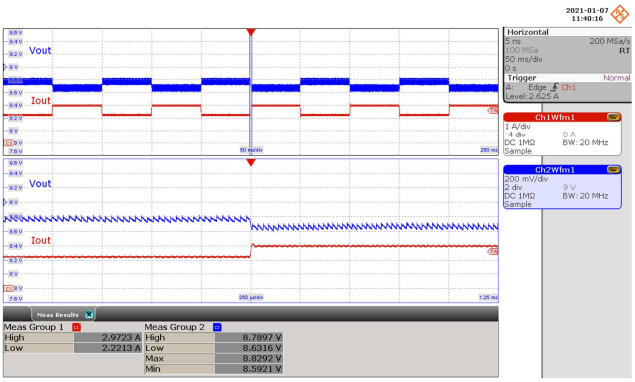


Figure 69 – Transient Response.
132 VAC, 9.0 V, 2.25 – 3.0 A Load Step.
V_{MIN}: 8.5921 V, V_{MAX}: 8.8292 V.
CH4: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (250 µs / div. Zoom)

12.2.3 Output: 12 V / 3 A

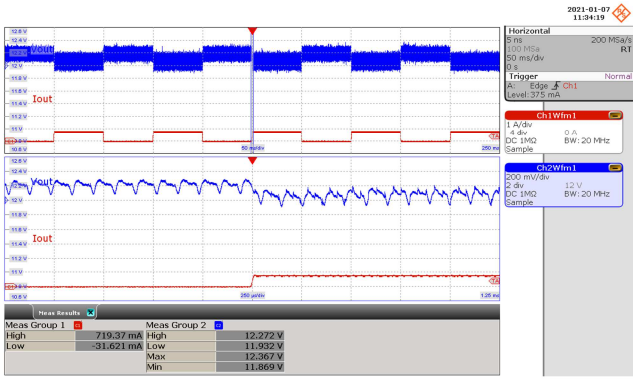


Figure 70 – Transient Response.
100 VAC, 12 V, 0 – 0.75 A Load Step.
V_{MIN}: 11.869 V, V_{MAX}: 12.367 V.
CH4: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (250 µs / div. Zoom)

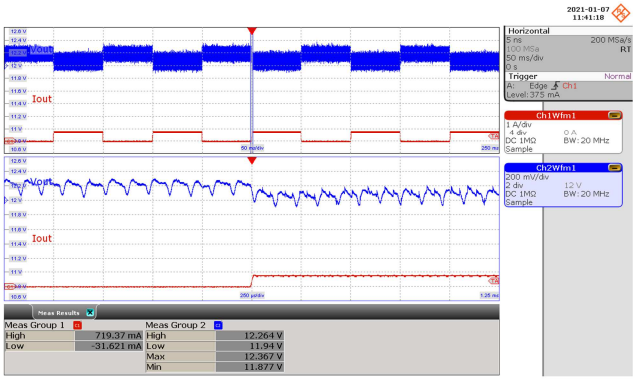


Figure 71 – Transient Response.
132 VAC, 12 V, 0 – 0.75 A Load Step.
V_{MIN}: 11.877 V, V_{MAX}: 12.367 V.
CH4: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (250 µs / div. Zoom)

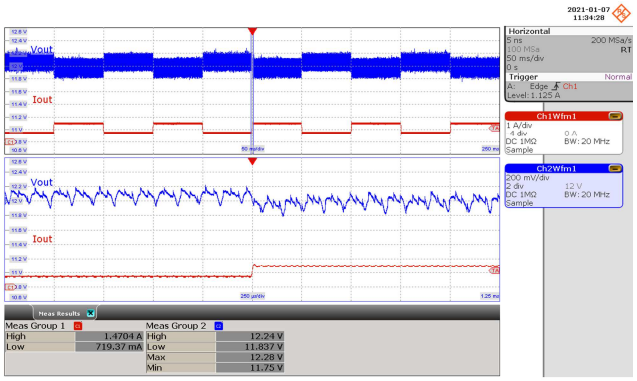


Figure 72 – Transient Response.
100 VAC, 12 V, 0.75 – 1.5 A Load Step.
V_{MIN}: 11.75 V, V_{MAX}: 12.28 V.
CH4: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (250 µs / div. Zoom)

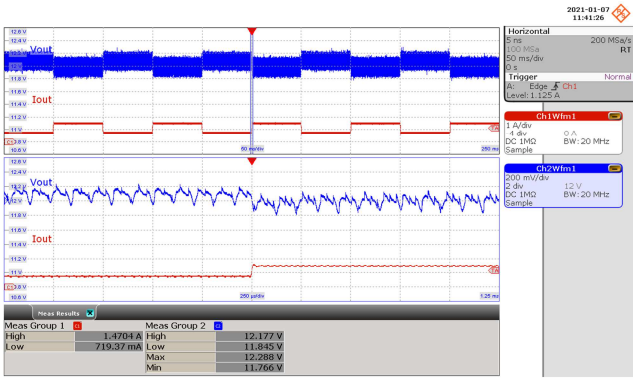


Figure 73 – Transient Response.
132 VAC, 12 V, 0.75 – 1.5 A Load Step.
V_{MIN}: 11.766 V, V_{MAX}: 12.288 V.
CH4: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (250 µs / div. Zoom)

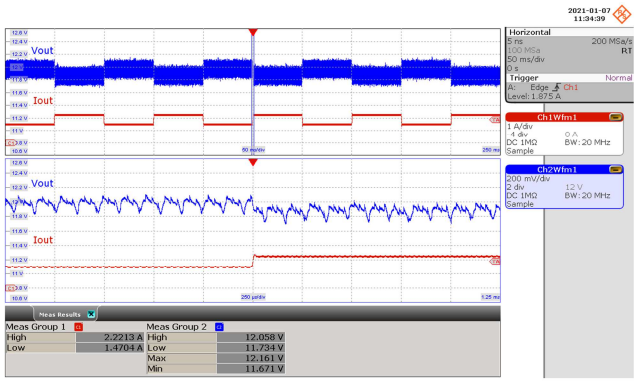


Figure 74 – Transient Response.
100 VAC, 12.0 V, 1.5 – 2.25 A Load Step.
V_{MIN}: 11.671 V, V_{MAX}: 12.161 V.
CH4: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (250 µs / div. Zoom)

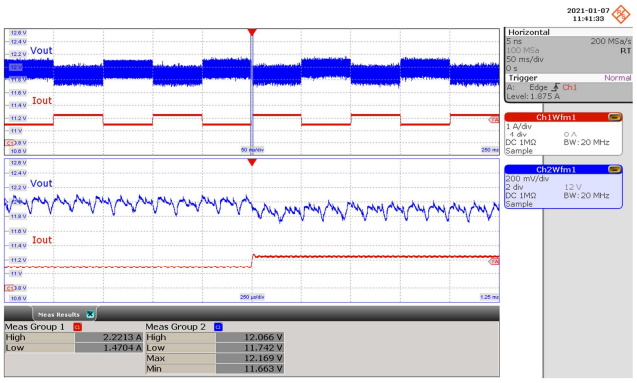


Figure 75 – Transient Response.
132 VAC, 12.0 V, 1.5 – 2.25 A Load Step.
V_{MIN}: 11.663 V, V_{MAX}: 12.169 V.
CH4: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (250 µs / div. Zoom)

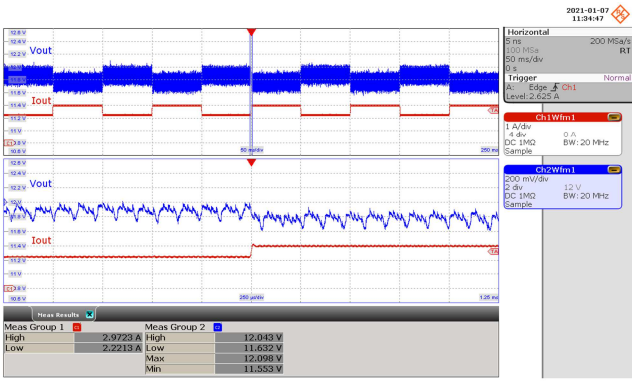


Figure 76 – Transient Response.
100 VAC, 12.0 V, 2.25 – 3 A Load Step.
V_{MIN}: 11.553 V, V_{MAX}: 12.098 V.
CH4: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (250 µs / div. Zoom)

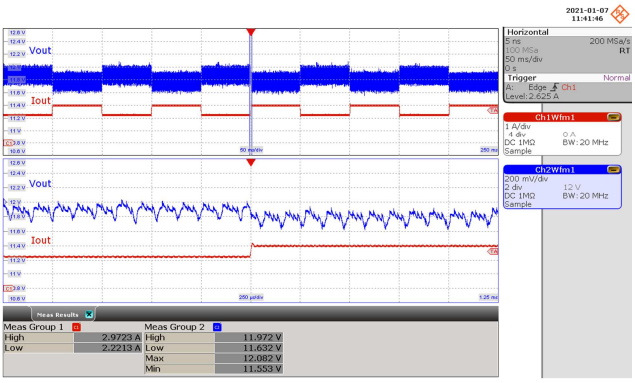


Figure 77 – Transient Response.
132 VAC, 12.0 V, 2.25 – 3 A Load Step.
V_{MIN}: 11.553 V, V_{MAX}: 12.082 V.
CH4: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (250 µs / div. Zoom)

12.2.4 Output: 15 V / 3 A

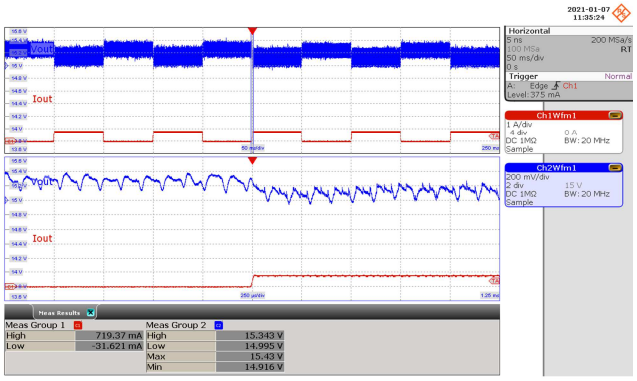


Figure 78 – Transient Response.
100 VAC, 15 V, 0 – 0.75 A Load Step.
V_{MIN}: 14.916 V, V_{MAX}: 15.43 V.
CH4: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (250 µs / div. Zoom)

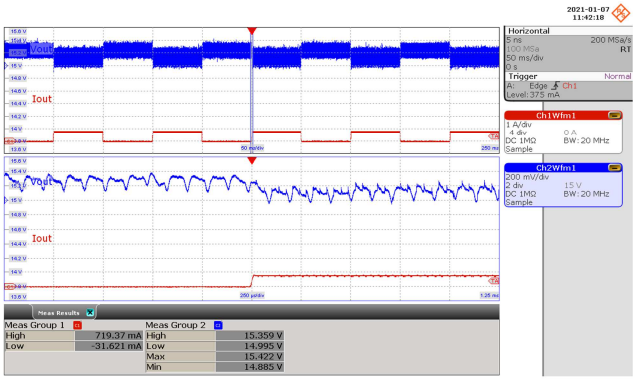


Figure 79 – Transient Response.
132 VAC, 15 V, 0 – 0.75 A Load Step.
V_{MIN}: 14.885 V, V_{MAX}: 15.422 V.
CH4: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (250 µs / div. Zoom)

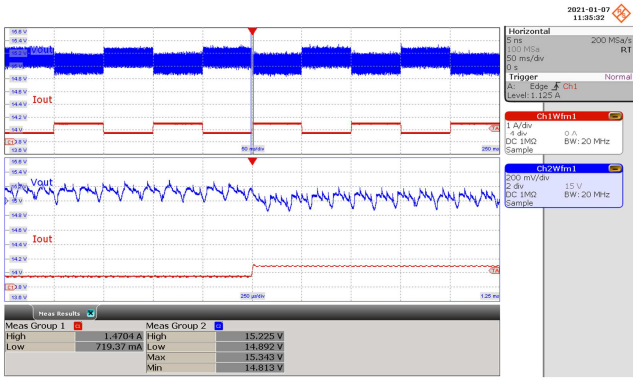


Figure 80 – Transient Response.
90 VAC, 15 V, 0.75 – 1.5 A Load Step.
V_{MIN}: 14.813 V, V_{MAX}: 15.343 V.
CH4: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (250 µs / div. Zoom)

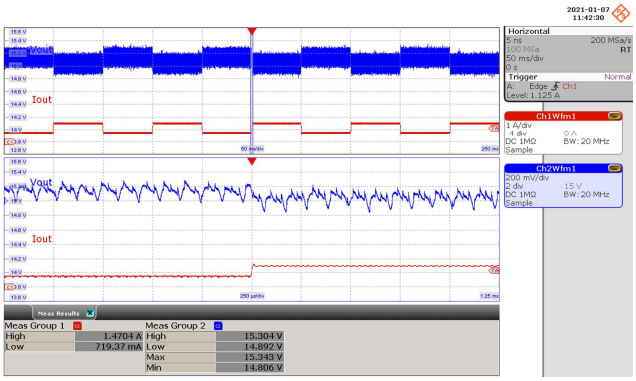


Figure 81 – Transient Response.
132 VAC, 15 V, 0.75 – 1.5 A Load Step.
V_{MIN}: 14.806 V, V_{MAX}: 15.343 V.
CH4: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (250 µs / div. Zoom)

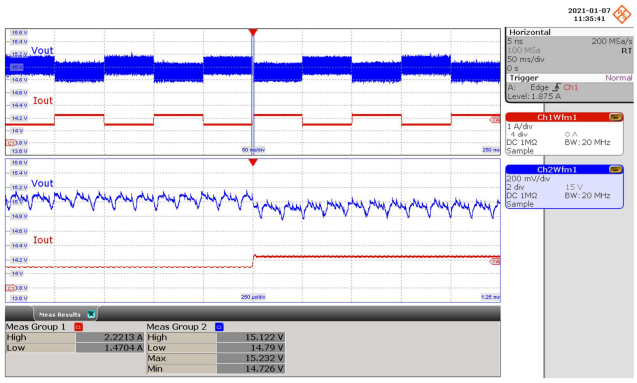


Figure 82 – Transient Response.
90 VAC, 15 V, 1.5 – 2.25 A Load Step.
V_{MIN}: 14.726 V, V_{MAX}: 15.232 V.
CH4: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (250 µs / div. Zoom)

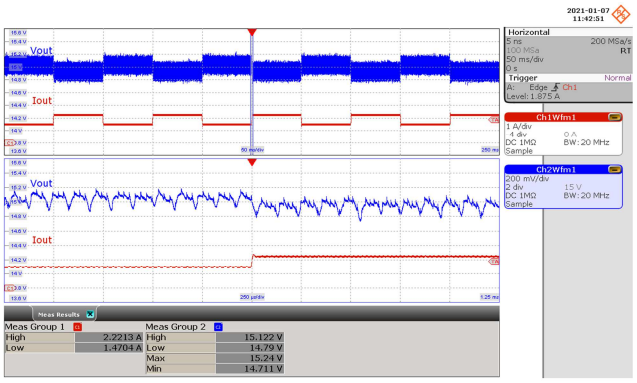


Figure 83 – Transient Response.
132 VAC, 15 V, 1.5 – 2.25 A Load Step.
V_{MIN}: 14.711 V, V_{MAX}: 15.24 V.
CH4: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (250 µs / div. Zoom)

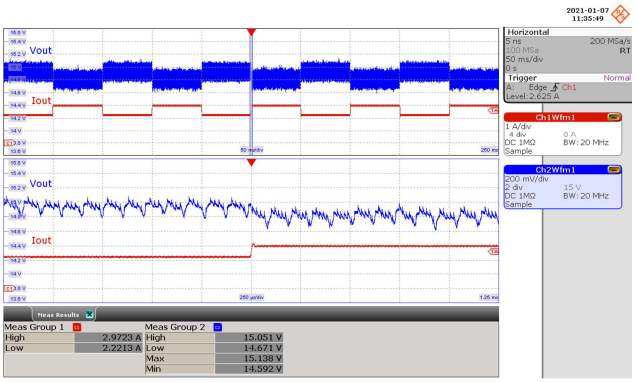


Figure 84 – Transient Response.
90 VAC, 15 V, 2.25 – 3 A Load Step.
V_{MIN}: 14.592 V, V_{MAX}: 15.138 V.
CH4: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (250 µs / div. Zoom)

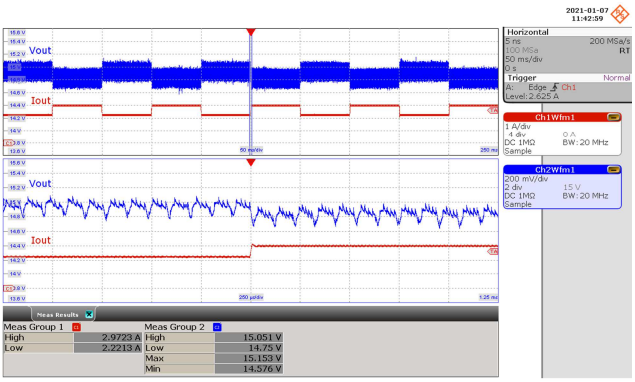


Figure 85 – Transient Response.
132 VAC, 12.0 V, 2.25 – 3 A Load Step.
V_{MIN}: 14.576 V, V_{MAX}: 15.153 V.
CH4: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (250 µs / div. Zoom)

12.2.5 Output: 20 V / 3.25 A

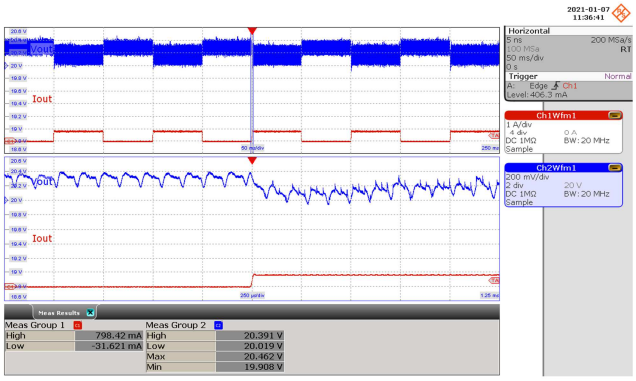


Figure 86 – Transient Response.
100 VAC, 20.0 V, 0 – 0.813 A Load Step.
V_{MIN}: 19.908 V, V_{MAX}: 20.462 V.
CH2: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (250 µs / div. Zoom)

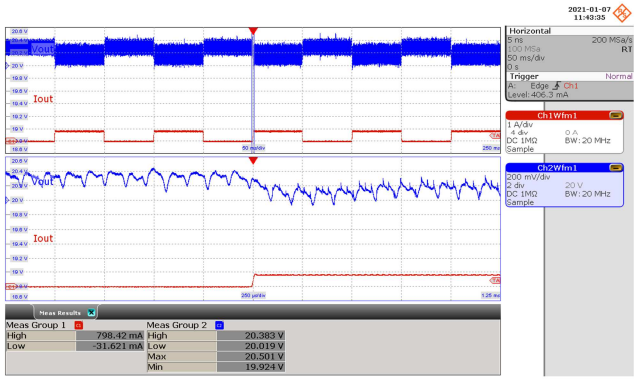


Figure 87 – Transient Response.
132 VAC, 20.0 V, 0 – 0.813 A Load Step.
V_{MIN}: 19.924 V, V_{MAX}: 20.501 V.
CH2: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (250 µs / div. Zoom)

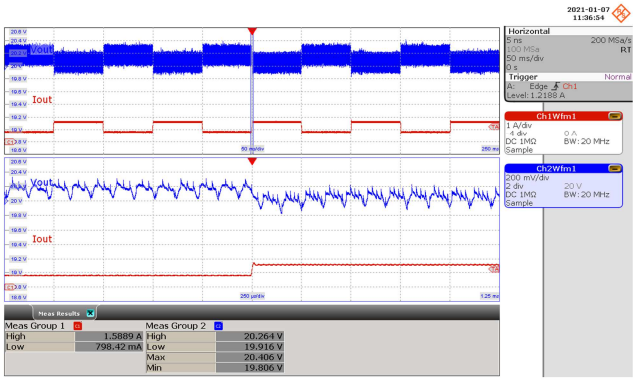


Figure 88 – Transient Response.
100 VAC, 20.0 V, 0.813 – 1.625 A Load Step.
V_{MIN}: 19.806 V, V_{MAX}: 20.406 V.
CH4: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 5 ms / div. (250 µs / div. Zoom)

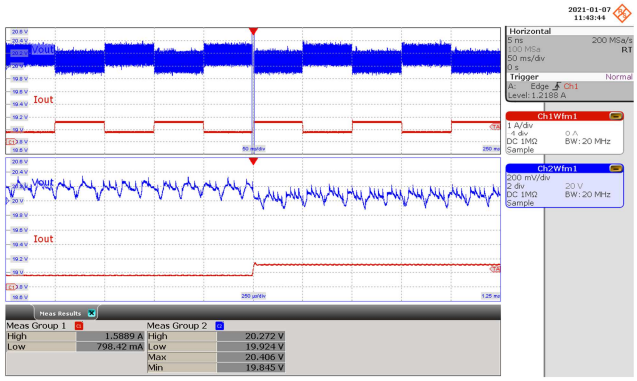


Figure 89 – Transient Response.
132 VAC, 20.0 V, 0.813 – 1.625 A Load Step.
V_{MIN}: 19.845 V, V_{MAX}: 20.406 V.
CH4: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (250 µs / div. Zoom)

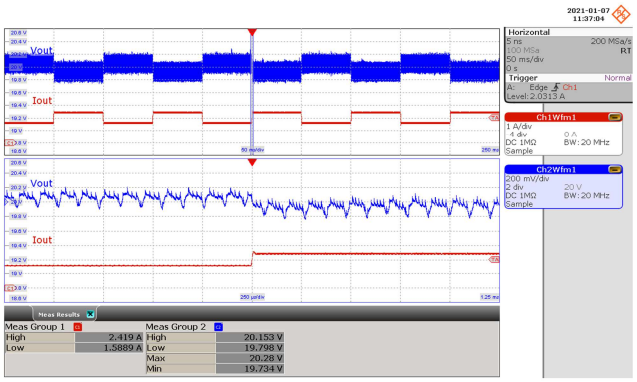


Figure 90 – Transient Response.
100 VAC, 20.0 V, 1.625 – 2.438 A Load Step.
V_{MIN}: 19.734 V, V_{MAX}: 20.18 V.
CH4: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (250 µs / div. Zoom)

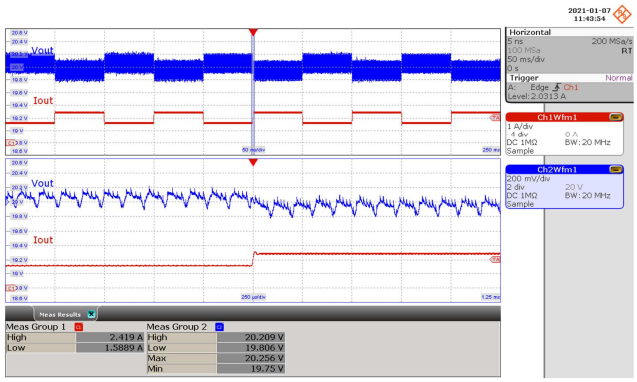


Figure 91 – Transient Response.
132 VAC, 20.0 V, 1.625 – 2.438 A Load Step.
V_{MIN}: 19.75 V, V_{MAX}: 20.256 V.
CH4: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (250 µs / div. Zoom)

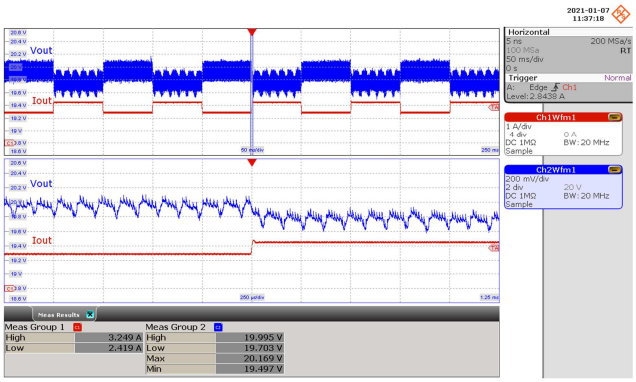


Figure 92 – Transient Response.
100 VAC, 20.0 V, 2.438 – 3.25 A Load Step.
V_{MIN}: 19.497 V, V_{MAX}: 20.169 V.
CH4: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (250 µs / div. Zoom)

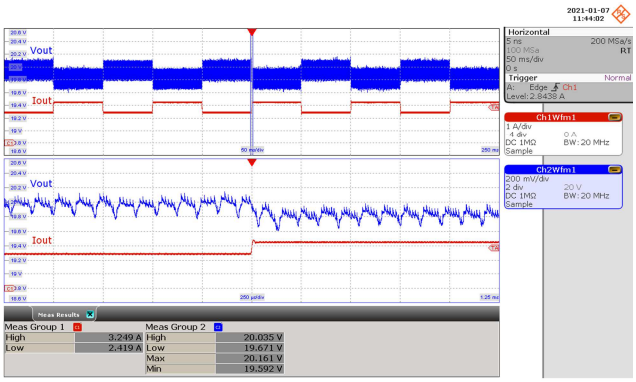


Figure 93 – Transient Response.
132 VAC, 20.0 V, 2.438 – 3.25 A Load Step.
V_{MIN}: 19.592 V, V_{MAX}: 20.161 V.
CH4: V_{OUT}, 0.2 V / div.
CH1: I_{LOAD}, 1 A / div.
Time: 50 ms / div. (250 µs / div. Zoom)

12.3 *Primary Drain Voltage and Current (Steady-State)*

12.3.1 Output: 5 V / 3 A

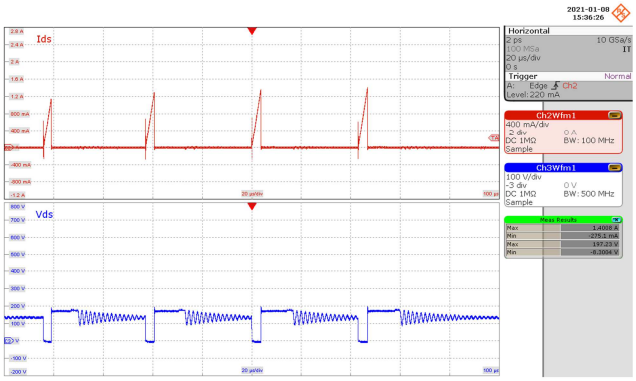


Figure 94 – Primary Drain Voltage and Current.
100 VAC, 5.0 V, 3 A Load (197.23 V_{MAX}).
CH3: V_{DRAIN}, 100 V / div.
CH2: I_{DRAIN}, 0.4 A / div.
Time: 20 µs / div.

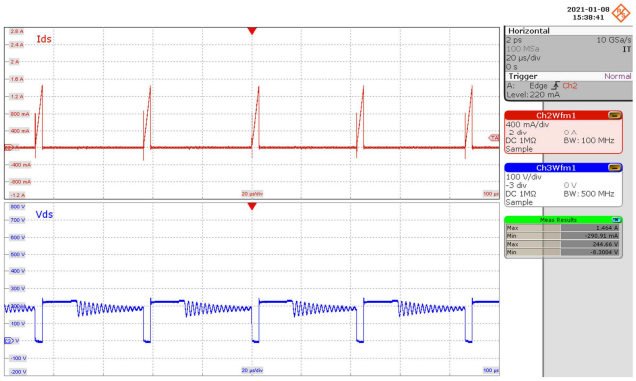


Figure 95 – Primary Drain Voltage and Current.
132 VAC, 5.0 V, 3 A Load (244.46 V_{MAX}).
CH3: V_{DRAIN}, 100 V / div.
CH2: I_{DRAIN}, 0.4 A / div.
Time: 20 µs / div.

12.3.2 Output: 9 V / 3 A

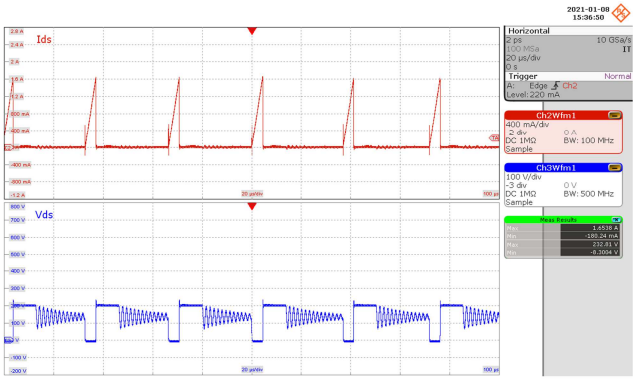


Figure 96 – Primary Drain Voltage and Current.
100 VAC, 9.0 V, 3 A Load (232.81 V_{MAX}).
CH3: V_{DRAIN}, 100 V / div.
CH2: I_{DRAIN}, 0.4 A / div.
Time: 20 µs / div.

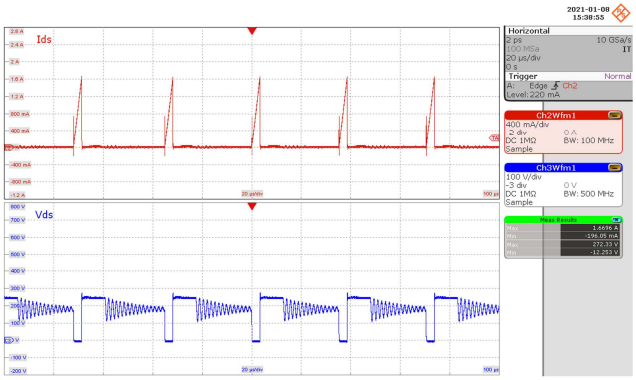


Figure 97 – Primary Drain Voltage and Current.
132 VAC, 9.0 V, 3 A Load (272.33 V_{MAX}).
CH3: V_{DRAIN}, 100 V / div.
CH2: I_{DRAIN}, 0.4 A / div.
Time: 20 µs / div.

12.3.3 Output: 12 V / 3 A

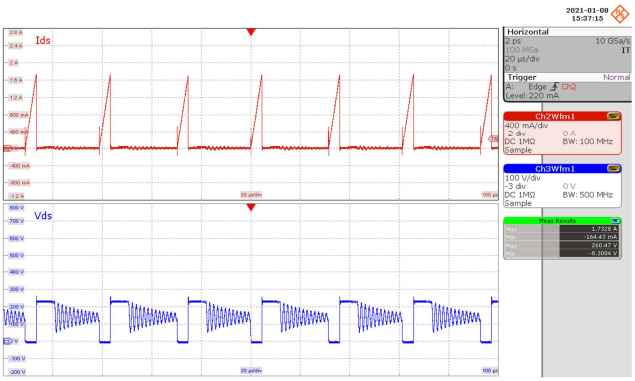


Figure 98 – Primary Drain Voltage and Current.
100 VAC, 12.0 V, 3 A Load (260.47 V_{MAX}).
CH3: V_{DRAIN}, 100 V / div.
CH2: I_{DRAIN}, 0.4 A / div.
Time: 20 µs / div.

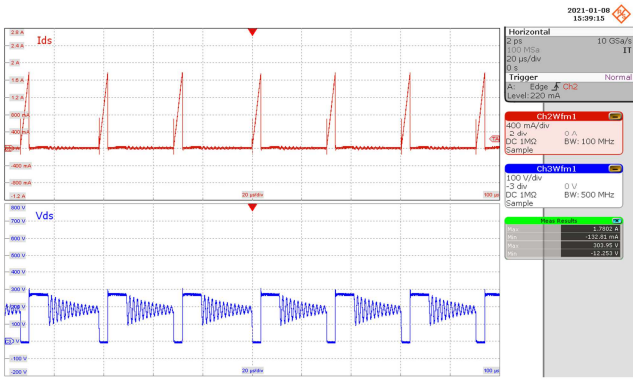


Figure 99 – Primary Drain Voltage and Current.
132 VAC, 12.0 V, 3 A Load (303.95 V_{MAX}).
CH3: V_{DRAIN}, 100 V / div.
CH2: I_{DRAIN}, 0.4 A / div.
Time: 20 µs / div.

12.3.4 Output: 15 V / 3 A

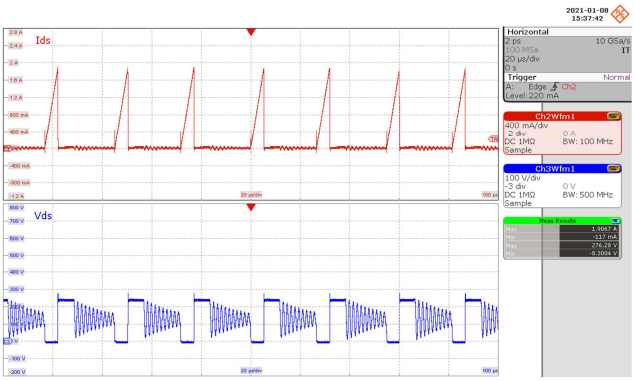


Figure 100 – Primary Drain Voltage and Current.
100 VAC, 15.0 V, 3 A Load (276.28 V_{MAX}).
CH3: V_{DRAIN}, 100 V / div.
CH2: I_{DRAIN}, 0.4 A / div.
Time: 20 µs / div.

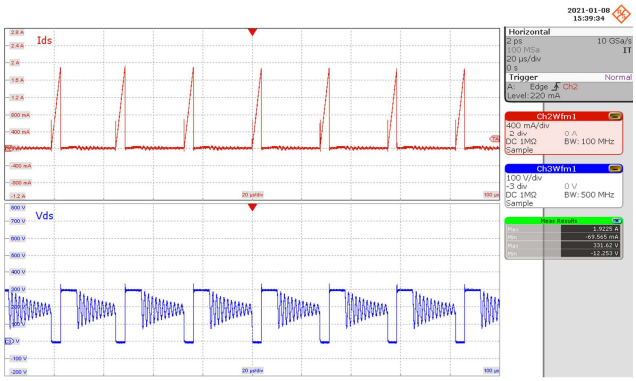


Figure 101 – Primary Drain Voltage and Current.
132 VAC, 15.0 V, 3 A Load (331.62 V_{MAX}).
CH3: V_{DRAIN}, 100 V / div.
CH2: I_{DRAIN}, 0.4 A / div.
Time: 20 µs / div.

12.3.5 Output: 20 V / 3.25 A

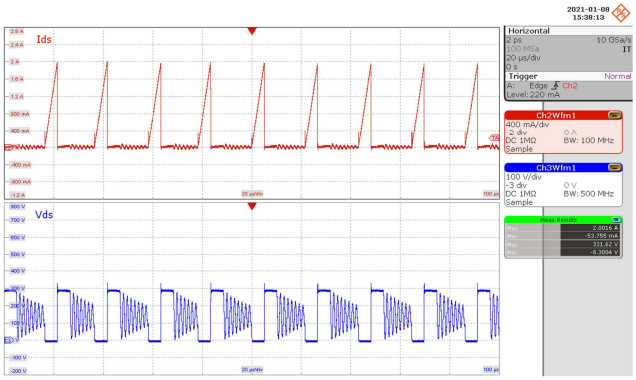


Figure 102 – Primary Drain Voltage and Current.
100 VAC, 20.0 V, 3.25 A Load (331.62 V_{MAX}).
CH3: V_{DRAIN}, 100 V / div.
CH2: I_{DRAIN}, 0.4 A / div.
Time: 20 µs / div.

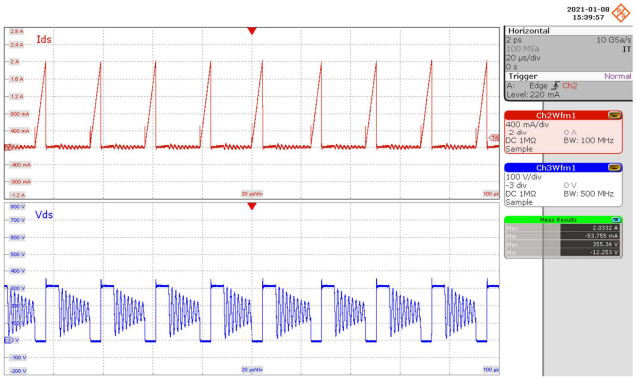


Figure 103 – Primary Drain Voltage and Current.
132 VAC, 20.0 V, 3.25 A Load (355.34 V_{MAX}).
CH3: V_{DRAIN}, 100 V / div.
CH2: I_{DRAIN}, 0.4 A / div.
Time: 20 µs / div.

12.4 *SR FET Drain Voltage and Current (Steady-State)*

12.4.1 Output: 5 V / 3 A

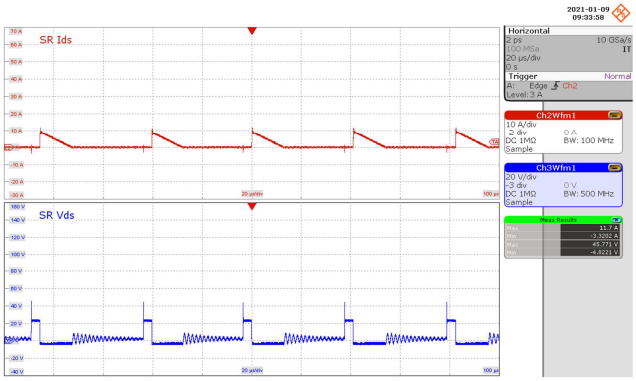


Figure 104 – SR FET Drain Voltage and Current.
100 VAC, 5.0 V, 3 A Load (45.77 V_{MAX}).
CH3: $V_{DRAIN(SR)}$, 20 V / div.
CH2: $I_{DRAIN(SR)}$, 10 A / div.
Time: 20 µs / div.

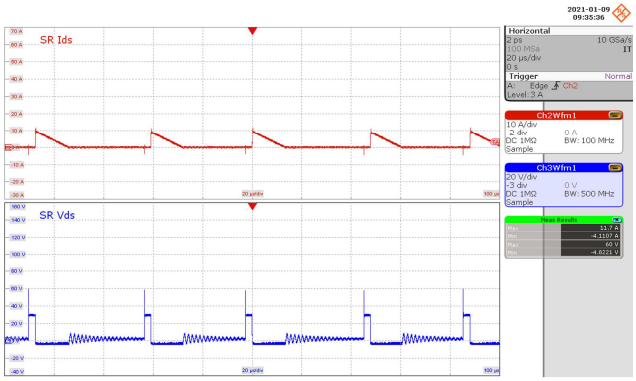


Figure 105 – SR FET Drain Voltage and Current.
132 VAC, 5.0 V, 3 A Load (60 V_{MAX}).
CH3: $V_{DRAIN(SR)}$, 20 V / div.
CH2: $I_{DRAIN(SR)}$, 10 A / div.
Time: 20 µs / div.

12.4.2 Output: 9 V / 3 A

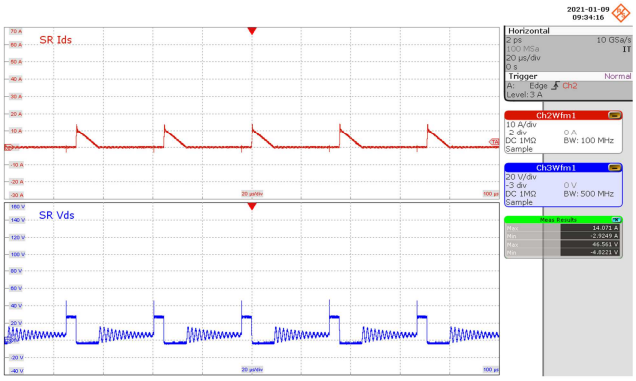


Figure 106 – SR FET Drain Voltage and Current.
100 VAC, 9.0 V, 3 A Load (46.56 V_{MAX}).
CH3: $V_{DRAIN(SR)}$, 20 V / div.
CH2: $I_{DRAIN(SR)}$, 10 A / div.
Time: 20 µs / div.

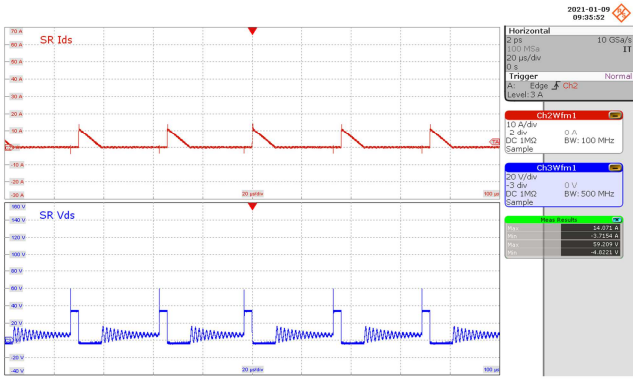


Figure 107 – SR FET Drain Voltage and Current.
132 VAC, 9.0 V, 3 A Load (59.21 V_{MAX}).
CH3: $V_{DRAIN(SR)}$, 20 V / div.
CH2: $I_{DRAIN(SR)}$, 10 A / div.
Time: 20 µs / div.

12.4.3 Output: 12 V / 3 A

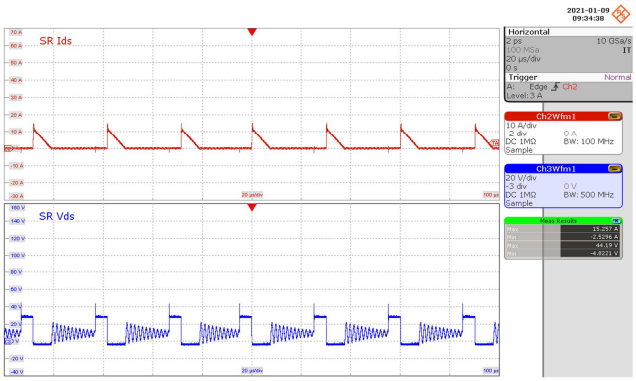


Figure 108 – SR FET Drain Voltage and Current.
100 VAC, 12.0 V, 3 A Load (44.19 V_{MAX}).
CH3: $V_{DRAIN(SR)}$, 20 V / div.
CH2: $I_{DRAIN(SR)}$, 10 A / div.
Time: 20 µs / div.

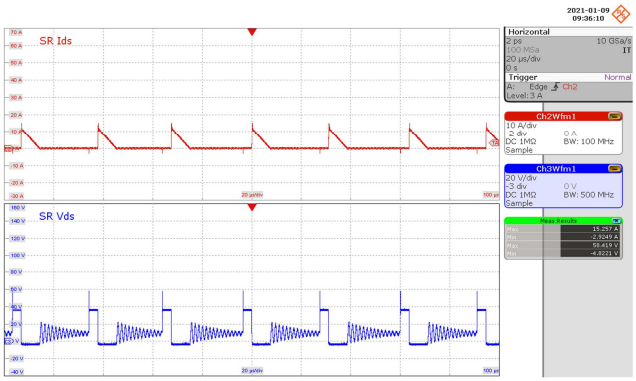


Figure 109 – SR FET Drain Voltage and Current.
132 VAC, 12.0 V, 3 A Load (58.42 V_{MAX}).
CH3: $V_{DRAIN(SR)}$, 20 V / div.
CH2: $I_{DRAIN(SR)}$, 10 A / div.
Time: 20 µs / div.

12.4.4 Output: 15 V / 3 A

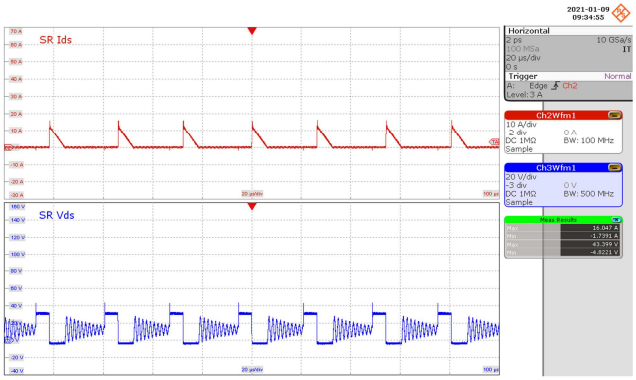


Figure 110 – SR FET Drain Voltage and Current.
100 VAC, 15.0 V, 3 A Load (43.4 V_{MAX}).
CH3: $V_{DRAIN(SR)}$, 20 V / div.
CH2: $I_{DRAIN(SR)}$, 10 A / div.
Time: 20 µs / div.

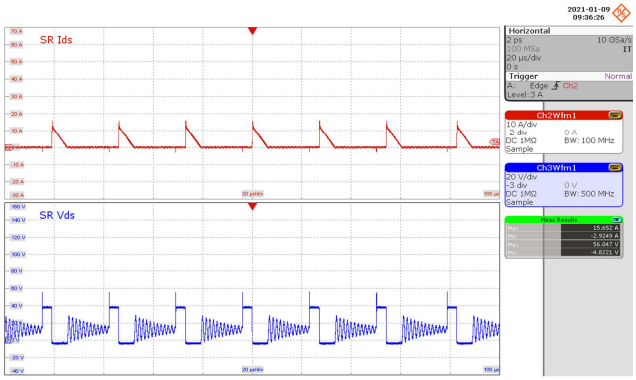


Figure 111 – SR FET Drain Voltage and Current.
132 VAC, 15.0 V, 3 A Load (56.05 V_{MAX}).
CH3: $V_{DRAIN(SR)}$, 20 V / div.
CH2: $I_{DRAIN(SR)}$, 10 A / div.
Time: 20 µs / div.

12.4.5 Output: 20 V / 3.25 A

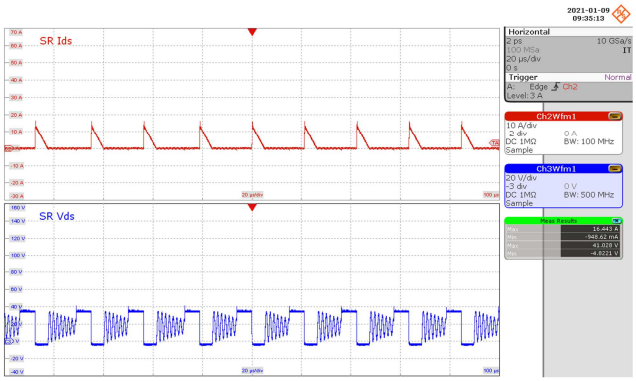


Figure 112 – SR FET Drain Voltage and Current.
100 VAC, 20.0 V, 3.25 A Load (41.03 V_{MAX}).
CH3: $V_{DRAIN(SR)}$, 20 V / div.
CH2: $I_{DRAIN(SR)}$, 10 A / div.
Time: 20 µs / div.

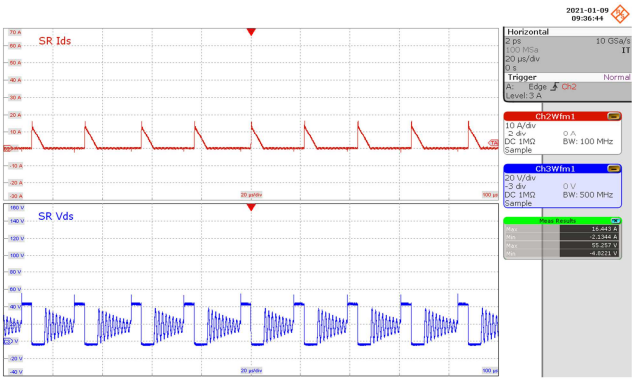


Figure 113 – SR FET Drain Voltage and Current.
132 VAC, 20.0 V, 3.25 A Load (55.26 V_{MAX}).
CH3: $V_{DRAIN(SR)}$, 20 V / div.
CH2: $I_{DRAIN(SR)}$, 10 A / div.
Time: 20 µs / div.

13 Output Ripple Measurements

13.1 *Ripple Measurement Technique*

For DC output ripple measurements, a modified oscilloscope test probe must be utilized to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 µF / 50 V ceramic type and one (1) 47 µF / 50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

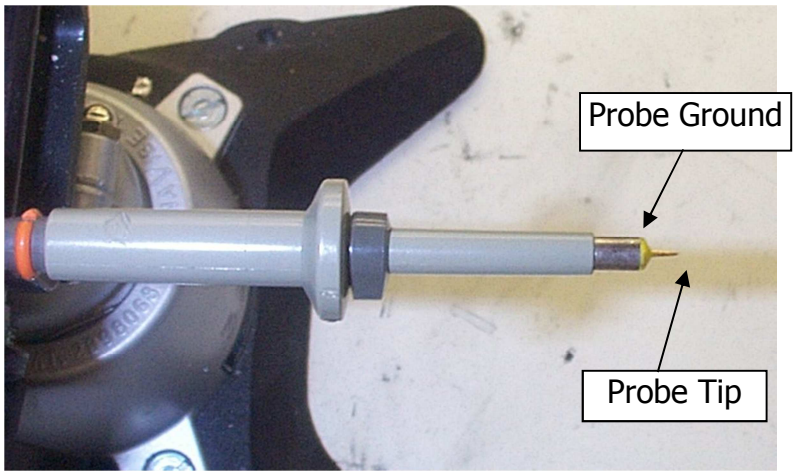


Figure 114 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

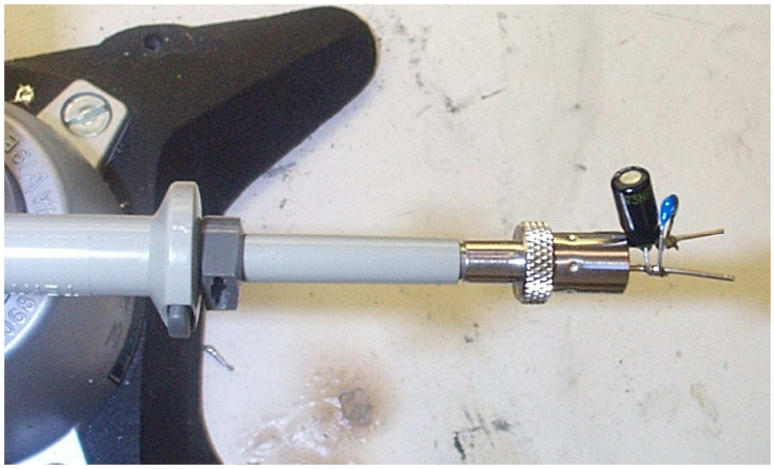


Figure 115 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

13.2 *Output Voltage Ripple Waveforms*

Note: 1. Output voltages captured at the end of 100 mΩ cable.
2. Measurements taken at room temperature ambient (approximately 25 °C).

13.2.1 Output: 5 V / 3 A

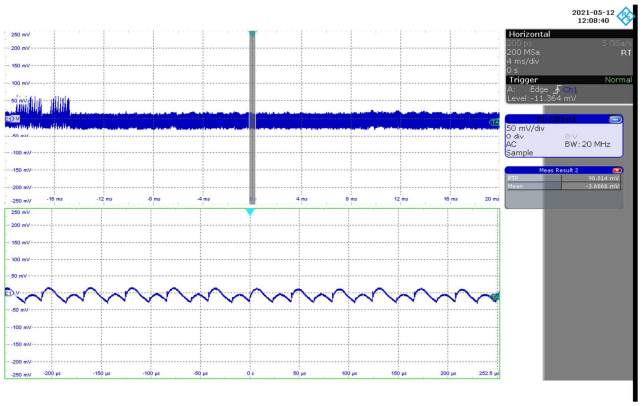


Figure 116 – Output Voltage Ripple.
100 VAC, 5.0 V,
3 A Load (98.814 mV_{PP}).
CH2: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (50 µs / div. Zoom)

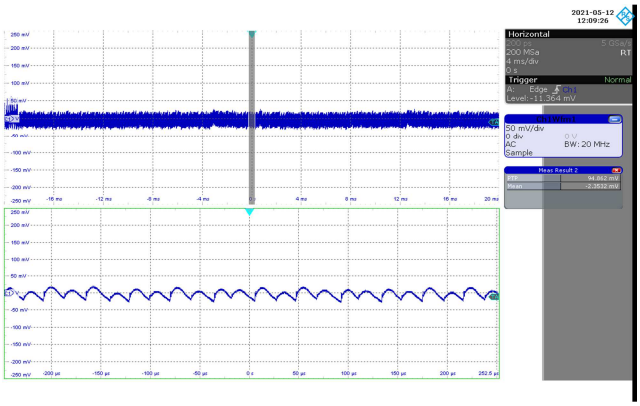


Figure 117 – Output Voltage Ripple.
132 VAC, 5.0 V,
3 A Load (94.862 mV_{PP}).
CH2: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (50 µs / div. Zoom)

13.2.2 Output: 9 V / 3 A

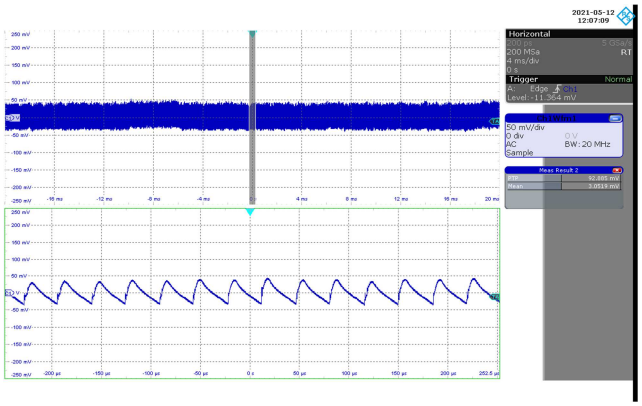


Figure 118 – Output Voltage Ripple.
100 VAC, 9.0 V,
3 A Load (92.885 mV_{PP}).
CH2: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (50 µs / div. Zoom)

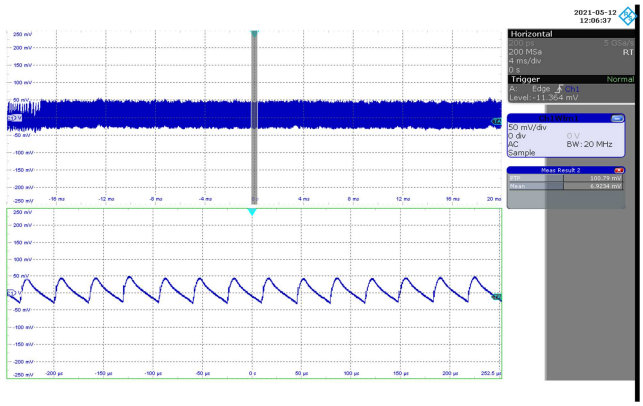


Figure 119 – Output Voltage Ripple.
132 VAC, 9.0 V,
3 A Load (100.79 mV_{PP}).
CH2: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (50 µs / div. Zoom)

13.2.3 Output: 12 V / 3 A

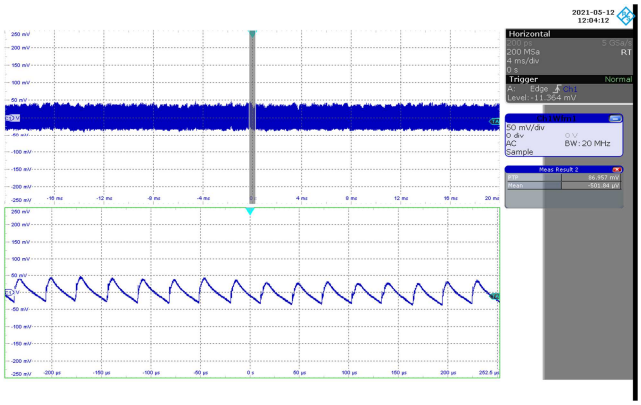


Figure 120 – Output Voltage Ripple.
100 VAC, 12.0 V,
3 A Load (86.957 mV_{PP}).
CH2: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (50 µs / div. Zoom)

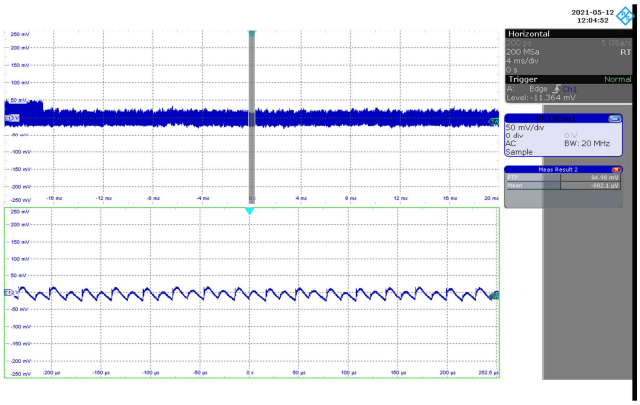


Figure 121 – Output Voltage Ripple.
132 VAC, 12.0 V,
3 A Load (84.98 mV_{PP}).
CH2: $V_{DRAIN(AC)}$, 50 mV / div.
Time: 5 ms / div. (50 µs / div. Zoom)

13.2.4 Output: 15 V / 3 A

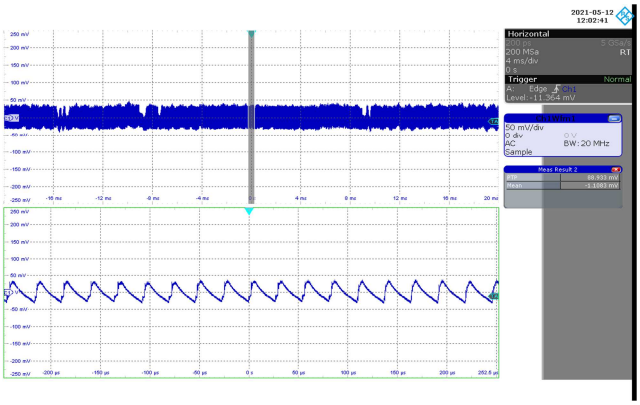


Figure 122 – Output Voltage Ripple.
100 VAC, 15.0 V,
3 A Load (88.933 mV_{PP}).
CH2: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (50 µs / div. Zoom)

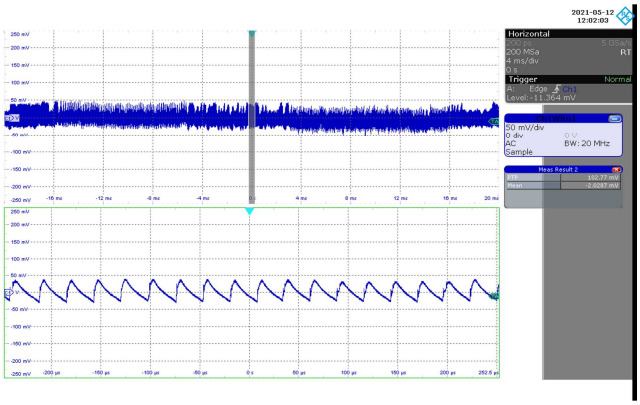


Figure 123 – Output Voltage Ripple.
132 VAC, 15.0 V,
3 A Load (102.77 mV_{PP}).
CH2: $V_{DRAIN(AC)}$, 50 mV / div.
Time: 5 ms / div. (50 µs / div. Zoom)

13.2.5 Output: 20 V / 3.25 A

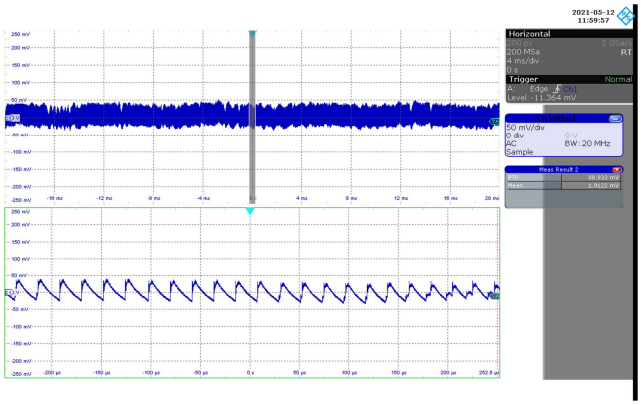


Figure 124 – Output Voltage Ripple.
100 VAC, 20.0 V,
3.25 A Load (88.933 mV_{PP}).
CH2: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (50 µs / div. Zoom)

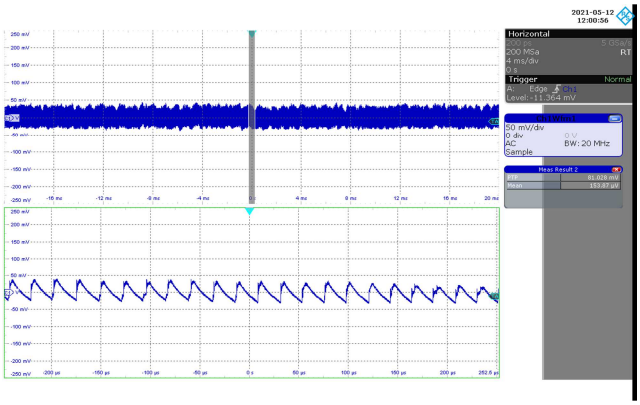


Figure 125 – Output Voltage Ripple.
100 VAC, 20.0 V,
3.25 A Load (81.028 mV_{PP}).
CH2: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (50 µs / div. Zoom)

13.3 *Output Voltage Ripple Amplitude vs. Load*

13.3.1 Output: 5 V / 3 A

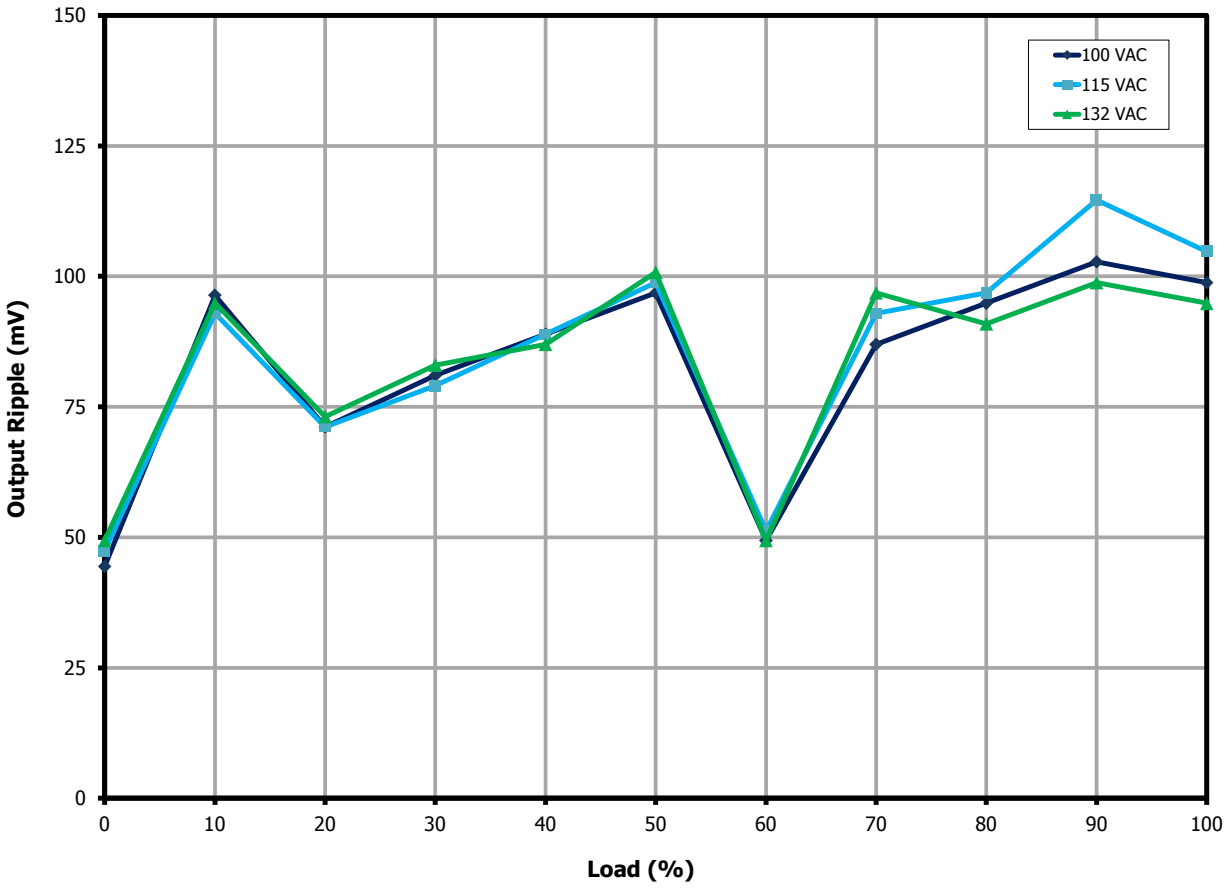


Figure 126 – Peak-to-Peak Output Voltage Ripple Amplitude vs. Load for 5 V Output.

13.3.2 Output: 9 V / 5 A

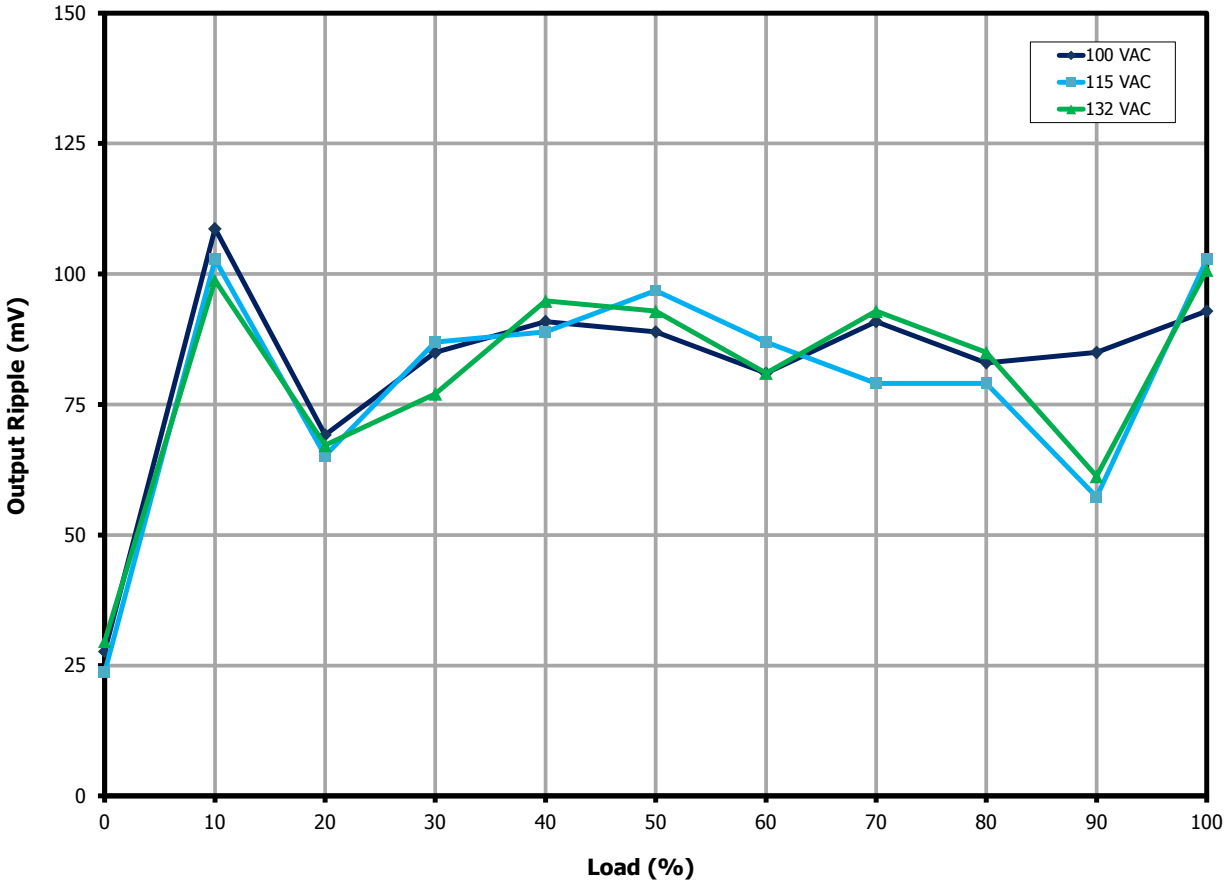


Figure 127 – Peak-to-Peak Output Voltage Ripple Amplitude vs. Load for 9 V Output.

13.3.3 Output: 12 V / 3 A

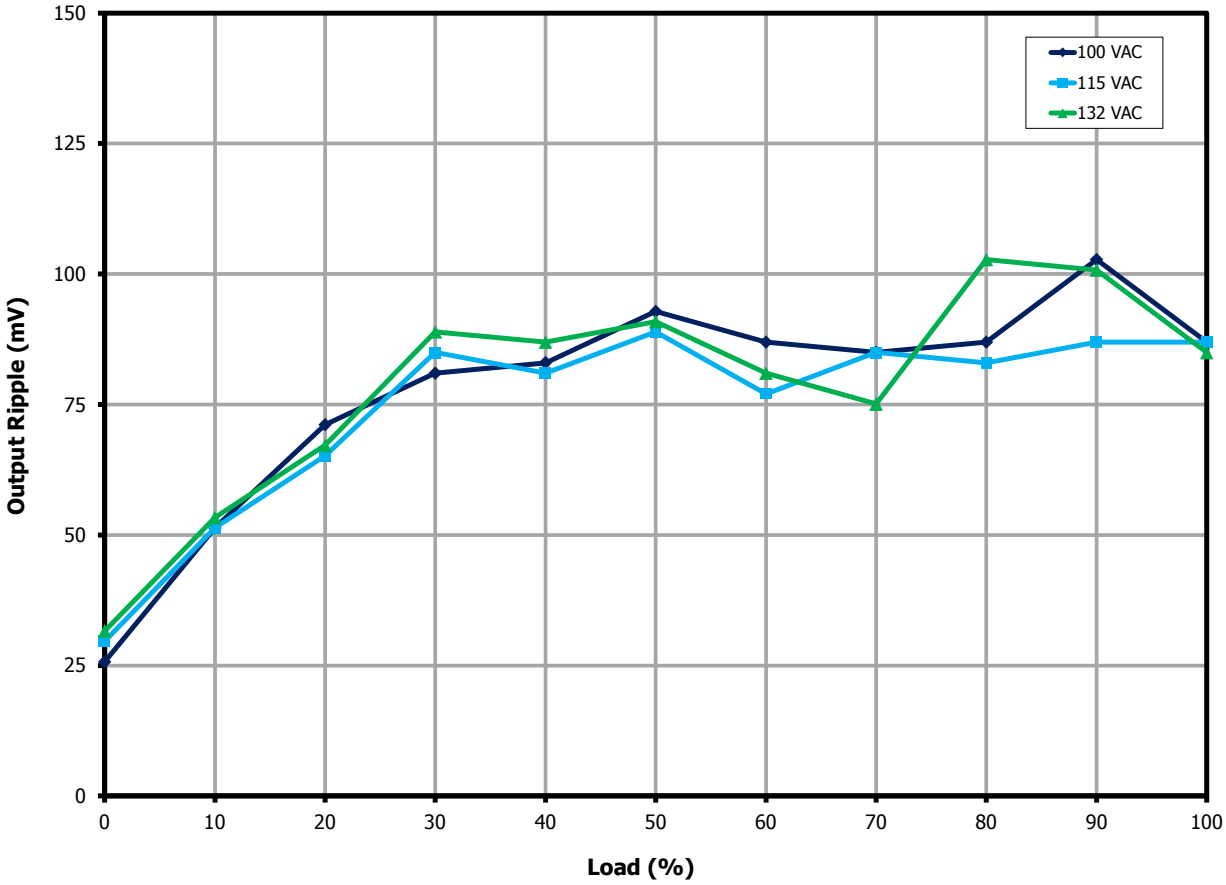


Figure 128 – Peak-to-Peak Output Voltage Ripple Amplitude vs. Load for 12 V Output.

13.3.4 Output: 15 V / 3 A

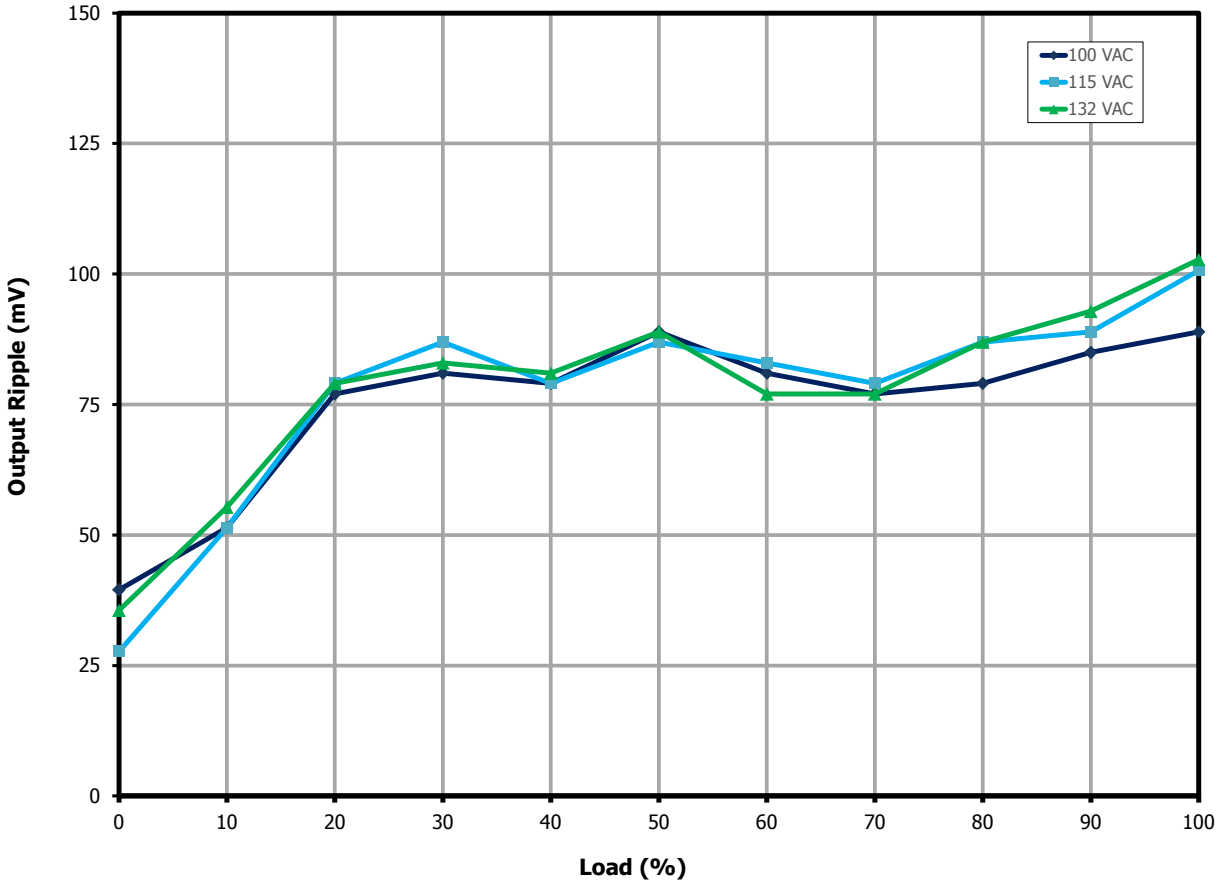


Figure 129 – Peak-to-Peak Output Voltage Ripple Amplitude vs. Load for 15 V Output.

13.3.5 Output: 20 V / 3.25 A

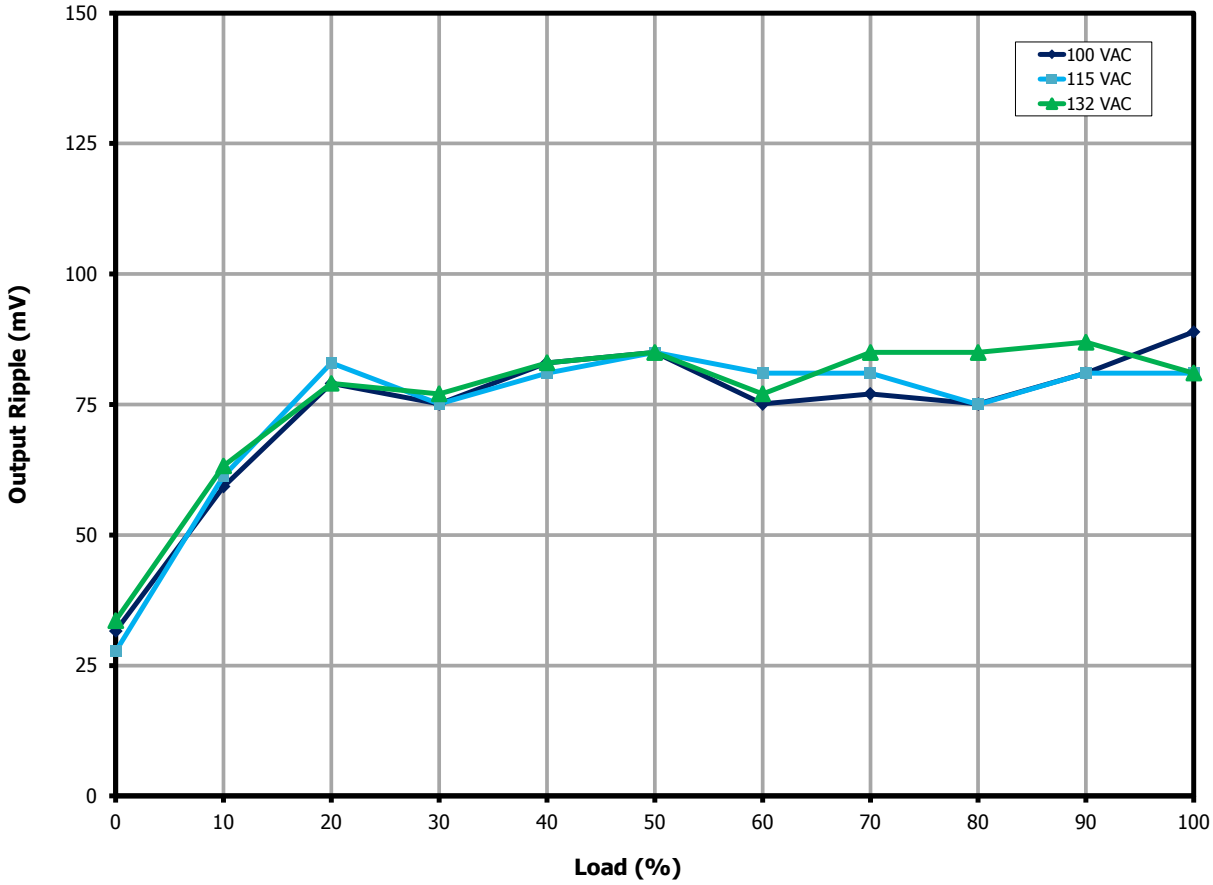


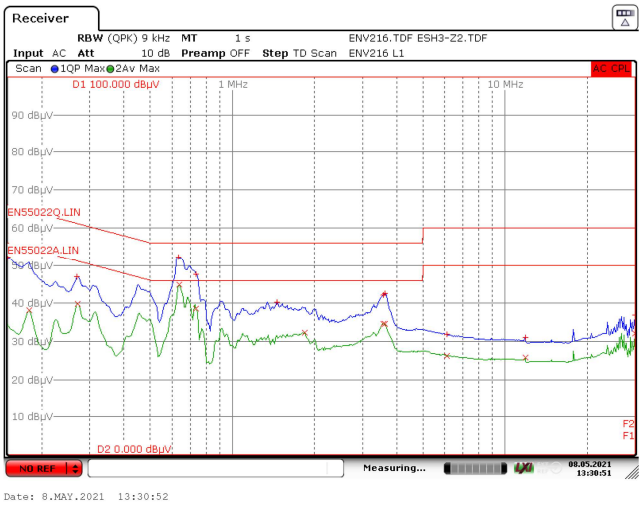
Figure 130. Peak-to-Peak Output Voltage Ripple Amplitude vs. Load for 20 V Output.

14 Conducted EMI

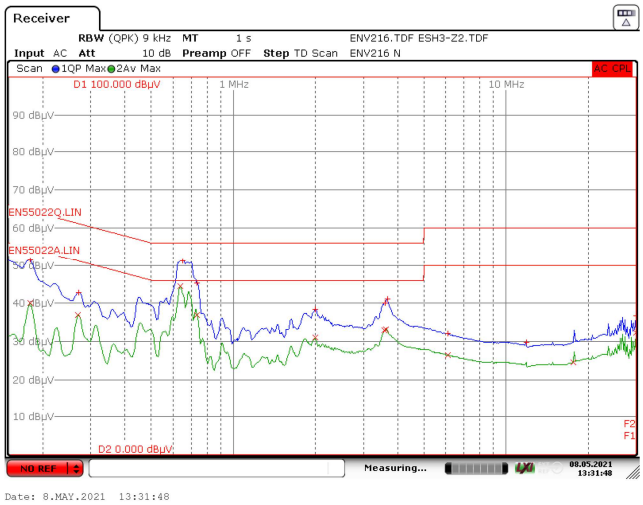
Note: EMI plots captured with heat spreader and adapter case enclosed.

14.1 *Floating Ground (QPK / AV)*

14.1.1 Single Port Output: Port A 65 W 20 V / 3.25 A and Port B Open



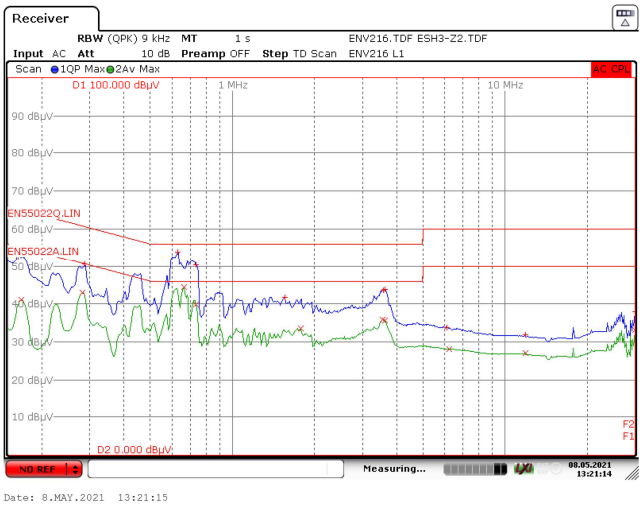
115 VAC Line Scan



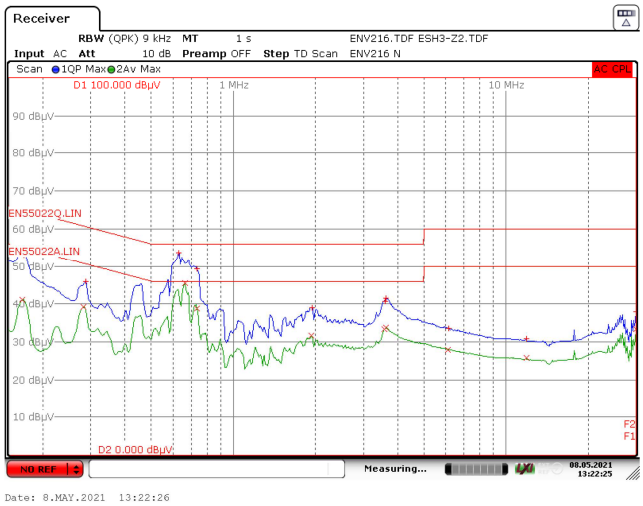
115 VAC Neutral Scan

Figure 131 – Floating Ground EMI, 20 V / 3.25 A Load.

14.1.2 Dual Port Output: Port A 45 W 20 V / 2.25 A and Port B 20 W 20 V / 1 A



115 VAC Line Scan.



115 VAC Neutral Scan

Figure 132 – Floating Ground EMI, 20 V / 2.25 A and 20 V / 1 A Load.

15 Combination Wave Surge

The unit was subjected to ±1000 V differential mode and ±2000 V common mode combination wave surge at several line phase angles with 10 strikes for each condition.

A test failure was defined as an output latch-off that needs operator intervention to recover, or a complete loss of function that is not recoverable.

Note: Surge tested on the power supply with heat spreader and adapter case enclosed.

15.1 *Differential Mode Surge (L1 to L2), 115 VAC Input*

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result Open Ports 5 V / 0 A	Test Result Dual Port Port A: 20 V / 2.25 A Port B: 20 V / 1A	Test Result Single Port 20 V / 3.25 A
+1000	L1 to L2	0	Pass	Pass	Pass
-1000	L1 to L2	0	Pass	Pass	Pass
+1000	L1 to L2	90	Pass	Pass	Pass
-1000	L1 to L2	90	Pass	Pass	Pass
+1000	L1 to L2	270	Pass	Pass	Pass
-1000	L1 to L2	270	Pass[1]	Pass	Pass

[1]Power supply might initiate Auto-Restart

15.2 *Common Mode Surge (L1, L2 to PE), 115 VAC Input*

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result Open Ports 5 V / 0 A	Test Result Dual Port 65 W Port A: 20 V / 2.25 A Port B: 20 V / 1 A	Test Result Single Port 65 W 20 V / 3.25 A
+2000	L1, L2 to PE	0	Pass	Pass	Pass
-2000	L1, L2 to PE	0	Pass	Pass	Pass
+2000	L1, L2 to PE	90	Pass	Pass	Pass
-2000	L1, L2 to PE	90	Pass	Pass	Pass
+2000	L1, L2 to PE	270	Pass	Pass	Pass
-2000	L1, L2 to PE	270	Pass	Pass	Pass

15.3 *Common Mode Surge (L1 to PE), 115 VAC Input*

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result Open Ports 5 V / 0 A	Test Result Dual Port 65 W Port A: 20 V / 2.25 A Port B: 20 V / 1 A	Test Result Single Port 65 W 20 V / 3.25 A
+2000	L1 to PE	0	Pass	Pass	Pass
-2000	L1 to PE	0	Pass	Pass	Pass

+2000	L1 to PE	90	Pass	Pass	Pass
-2000	L1 to PE	90	Pass	Pass	Pass
+2000	L1 to PE	270	Pass	Pass	Pass
-2000	L1 to PE	270	Pass	Pass	Pass

15.4 *Common Mode Surge (L2 to PE), 115 VAC Input*

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result 5 V / 0 A	Test Result Port A: 20 V / 2.25 A Port B: 20 V / 1 A	Test Result 20 V / 3.25 A
+2000	L2 to PE	0	Pass	Pass	Pass
-2000	L2 to PE	0	Pass	Pass	Pass
+2000	L2 to PE	90	Pass	Pass	Pass
-2000	L2 to PE	90	Pass	Pass	Pass
+2000	L2 to PE	270	Pass	Pass	Pass
-2000	L2 to PE	270	Pass	Pass	Pass

Note: Surge events might trigger input line OV Protection and initiate an auto-restart. Auto-restart (AR) is one of the safety features of InnoSwitch3-Pro to protect the converter from fault conditions. For applications that require completely no output interruption, the design can be modified to have a higher input line OVP voltage threshold or with the input line OVP completely disabled.

16 Electrostatic Discharge

The unit was tested with ±8 kV to ±16.5 kV air discharge and ±8.8 kV contact discharge with 10 strikes for each condition at the following locations:

- End of cable +VOUT
- End of cable GND
- On-board +VOUT
- On-board GND
- End of cable CC1
- End of cable CC2

A test failure was defined as an output latch-off that needs operator intervention to recover, or a complete loss of function that is not recoverable.

Note: 1. End of cable discharge points (VOUT, GND, CC1, CC2) located on the USB-C power adapter tester Tiny-PAT
2. Type-C cable for VOUT and GND strikes: E-marked 5 A cable, 1 meter (CableCreation)
3. Type-C cable for CC1 and CC2 strikes: Passive 3 A cable, 1 meter (Google)

16.1 *Contact Discharge, +VOUT and GND, 115 VAC Input*

Discharge Voltage (kV)	ESD Strike Location		Test Result Single Port 5 V / 0 A	Test Result Port A: 20 V / 2.25 A Port B: 20 V / 1 A	Test Result Single Port 20 V / 3.25 A
+8.8	End of Cable	+VOUT	Pass	Pass	Pass
		GND	Pass	Pass	Pass
-8.8		+VOUT	Pass	Pass	Pass
		GND	Pass	Pass	Pass
+8.8	On the Board	+VOUT	Pass	Pass	Pass
		GND	Pass	Pass	Pass
-8.8		+VOUT	Pass	Pass	Pass
		GND	Pass	Pass	Pass

16.2 *Contact Discharge, CC1 and CC2, 115 VAC Input*

Discharge Voltage (kV)	ESD Strike Location		Test Result 5 V / 0 A	Test Result 20 V / 2.25 A
+8.8	End of Cable	CC1	Pass[1]	Pass[1]
		CC2	Pass[1]	Pass[1]
-8.8		CC1	Pass[1]	Pass[1]
		CC2	Pass[1]	Pass[1]

[1]Power supply might initiate Auto-Restart

16.3 *Air Discharge, +VOUT and GND, 115 VAC Input*

Discharge Voltage (kV)	ESD Strike Location (End of Type-C Cable)		Test Result 5 V / 0 A	Test Result 9 V / 5 A	Test Result 20 V / 2.25 A
+8	End of Cable	+VOUT	Pass	Pass	Pass
		GND	Pass	Pass	Pass
-8		+VOUT	Pass	Pass	Pass
		GND	Pass	Pass	Pass
+10		+VOUT	Pass[1]	Pass[1]	Pass[1]
		GND	Pass[1]	Pass[1]	Pass[1]
-10		+VOUT	Pass[1]	Pass[1]	Pass[1]
		GND	Pass[1]	Pass[1]	Pass[1]
+12		+VOUT	Pass[1]	Pass[1]	Pass[1]
		GND	Pass[1]	Pass[1]	Pass[1]
-12		+VOUT	Pass[1]	Pass[1]	Pass[1]
		GND	Pass[1]	Pass[1]	Pass[1]
+14		+VOUT	Pass[1]	Pass[1]	Pass[1]
		GND	Pass[1]	Pass[1]	Pass[1]
-14		+VOUT	Pass[1]	Pass[1]	Pass[1]
		GND	Pass[1]	Pass[1]	Pass[1]
+16.5		+VOUT	Pass[1]	Pass[1]	Pass[1]
		GND	Pass[1]	Pass[1]	Pass[1]
-16.5		+VOUT	Pass[1]	Pass[1]	Pass[1]
		GND	Pass[1]	Pass[1]	Pass[1]
+8	On the Board	+VOUT	Pass	Pass	Pass
		GND	Pass	Pass	Pass
-8		+VOUT	Pass	Pass	Pass
		GND	Pass	Pass	Pass
+10		+VOUT	Pass[1]	Pass[1]	Pass[1]
		GND	Pass[1]	Pass[1]	Pass[1]
-10		+VOUT	Pass[1]	Pass[1]	Pass[1]
		GND	Pass[1]	Pass[1]	Pass[1]
+12		+VOUT	Pass[1]	Pass[1]	Pass[1]
		GND	Pass[1]	Pass[1]	Pass[1]
-12		+VOUT	Pass[1]	Pass[1]	Pass[1]
		GND	Pass[1]	Pass[1]	Pass[1]
+14		+VOUT	Pass[1]	Pass[1]	Pass[1]
		GND	Pass[1]	Pass[1]	Pass[1]
-14		+VOUT	Pass[1]	Pass[1]	Pass[1]
		GND	Pass[1]	Pass[1]	Pass[1]
+16.5		+VOUT	Pass[1]	Pass[1]	Pass[1]
		GND	Pass[1]	Pass[1]	Pass[1]
-16.5		+VOUT	Pass[1]	Pass[1]	Pass[1]
		GND	Pass[1]	Pass[1]	Pass[1]

16.4 *Air Discharge, CC1 and CC2, 115 VAC Input*

Discharge Voltage (kV)	ESD Strike Location		Test Result 5 V / 0 A	Test Result 20 V / 2.25 A
+8	End of Cable	CC1	Pass[1]	Pass[1]
		CC2	Pass[1]	Pass[1]
-8		CC1	Pass[1]	Pass[1]
		CC2	Pass[1]	Pass[1]
+10		CC1	Pass[1]	Pass[1]
		CC2	Pass[1]	Pass[1]
-10		CC1	Pass[1]	Pass[1]
		CC2	Pass[1]	Pass[1]
+12		CC1	Pass[1]	Pass[1]
		CC2	Pass[1]	Pass[1]
-12		CC1	Pass[1]	Pass[1]
		CC2	Pass[1]	Pass[1]
+14		CC1	Pass[1]	Pass[1]
		CC2	Pass[1]	Pass[1]
-14		CC1	Pass[1]	Pass[1]
		CC2	Pass[1]	Pass[1]
+16.5		CC1	Pass[1]	Pass[1]
		CC2	Pass[1]	Pass[1]
-16.5		CC1	Pass[1]	Pass[1]
		CC2	Pass[1]	Pass[1]

[1]Power supply might initiate Auto-Restart

17 Revision History

Date	Author	Revision	Description & Changes	Reviewed
03-Nov-21	CC	1.0	Initial Release.	Apps & Mktg

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