Design Example Report

Title	***15 W Isolated Flyback Power Supply Using InnoSwitch™3-CE INN3164C- H101 with ±30 kV ESD Capability***
Specification	90 VAC – 265 VAC Input; 12 V, 1.25 A Output
Application	Adapter with ±30 kV ESD Capability
Author	Applications Engineering Department
Document Number	DER-717
Date	February 23, 2021
Revision	1.0

Summary and Features

- ±30 kV ESD Class B
- >90% average efficiency at nominal AC input
- <25 mW no-load input power
- Integrate protection and reliability features
    - Output short-circuit
    - Line and output OVP
    - Over temperature shutdown
- Synchronous rectification for higher efficiency
- Meets EN550022 and CISPR-22 Class B conducted EMI
- Meets IEC 1.0 kV differential surge
- Meets IEC 2.0 kV differential ring wave

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Important Note: Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

Demand for consumer electronics products are steadily increasing. At the same time, a more robust and reliable power supply is a must. Adapter that can withstand high ESD voltages increases power supply reliability and robustness.

This engineering report describes an isolated flyback adapter designed to provide a nominal output voltage of 12 V at 1.25 A load from a wide input voltage range of 90 VAC to 265 VAC. Design of this power supply can withstand ± 30 kV ESD. This adapter utilizes the INN3164C-H101 from the InnoSwitch3-CE family of ICs.

This document contains the complete power supply specifications, bill of materials, transformer construction, circuit schematic and printed circuit board layout, along with performance data and electrical waveforms.

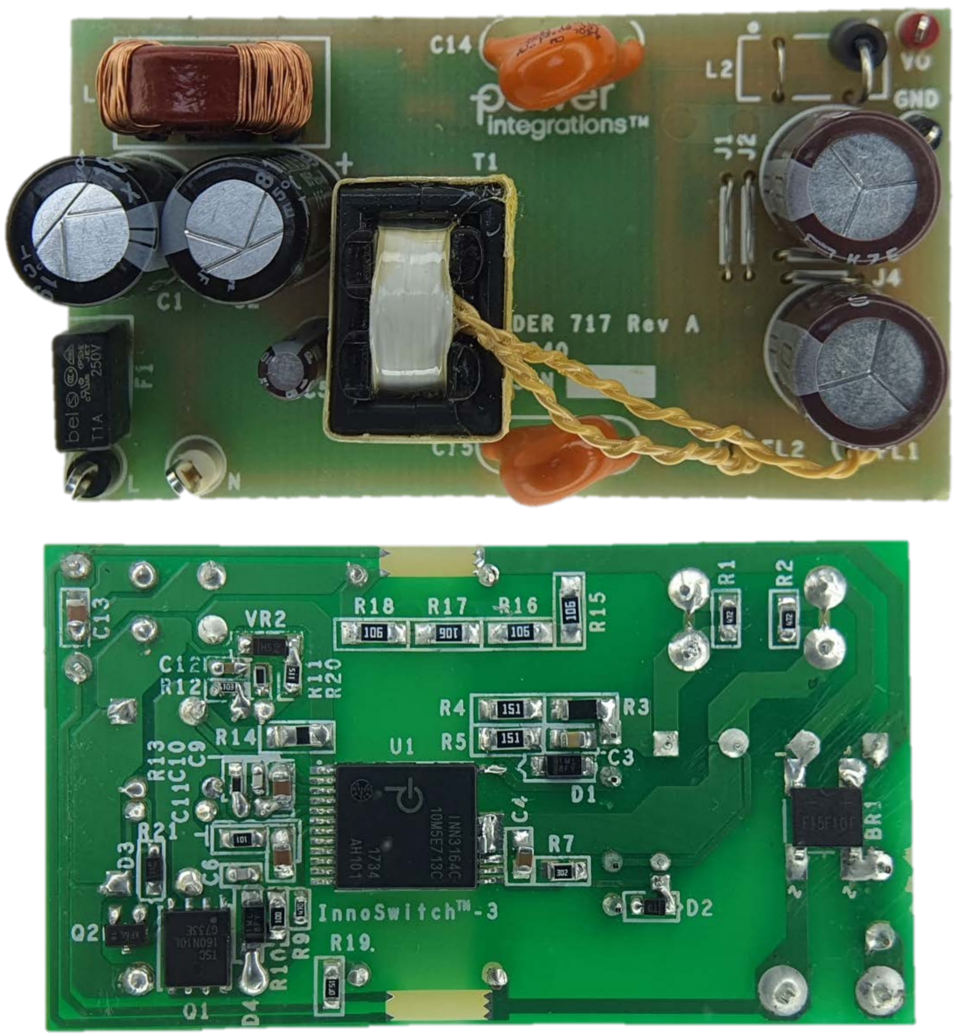

Figure 1 – Populated Circuit Board.

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2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power				0.025	W	230 VAC.
Output						
Output Voltage	V_{OUT}	11.4	12	12.6	V	± 5%
Output Ripple Voltage	V_{RIPPLE}			200	mV	20 MHz Bandwidth.
Output Current	I_{OUT}		1.25		A	
Total Output Power						
Continuous Output Power	P_{OUT}		15		W	
Efficiency						
Full Load	η		90		%	Measured at P_{OUT} 25 °C.
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				
Surge				1	kV	1.2/50 µs surge, IEC 61000-4-5, Series Impedance: Differential Mode: 2 Ω Common Mode: 12 Ω.
Ring Wave				2	kV	
ESD				±30 ±8	kV kV	Air Discharge. Contact Discharge.
Ambient Temperature	T_{AMB}	0		50	°C	Free Convection, Sea Level.

3 Schematic

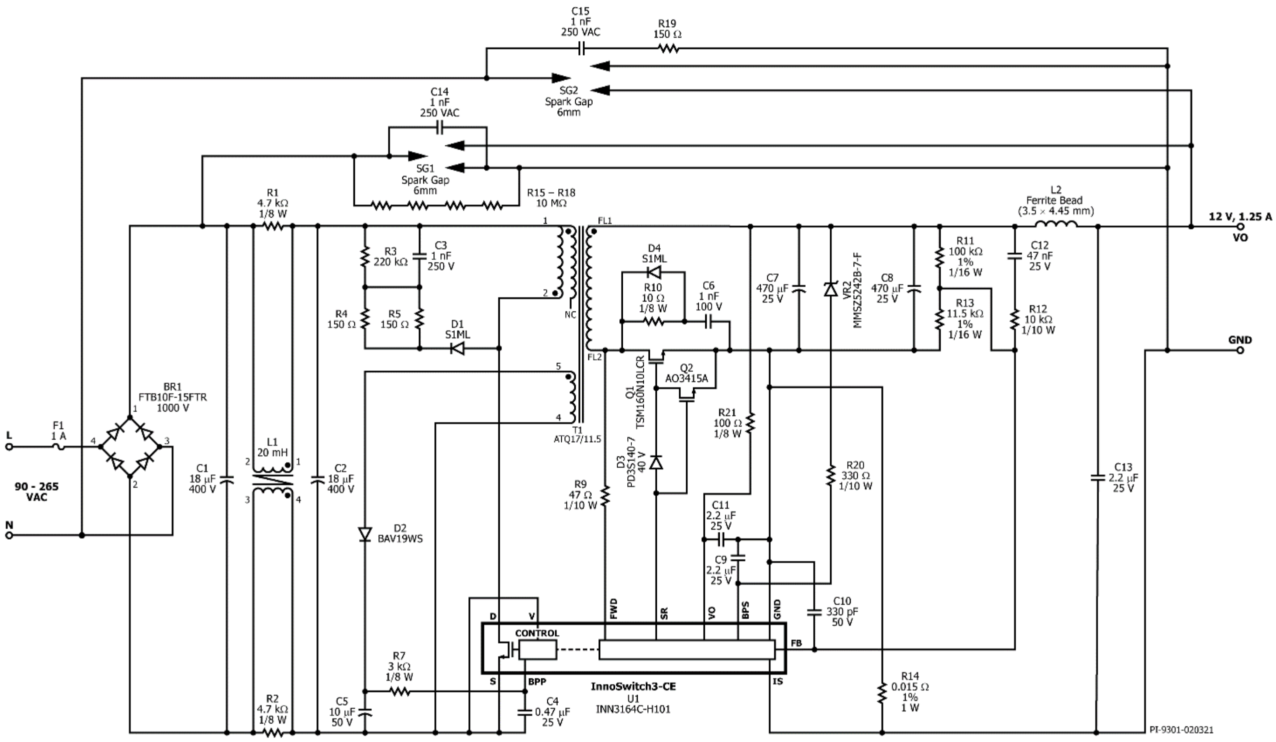

Figure 2 – Schematic.

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4 Circuit Description

The InnoSwitch3-CE IC combines primary, secondary, and feedback circuits in a single surface mounted off-line flyback switcher IC. The IC incorporates the primary MOSFET, the primary-side controller, the secondary-side controller for synchronous rectification, and the Fluxlink™ technology that eliminates the optocoupler on a secondary sensed feedback system.

4.1 *Input Rectifier and Filter*

Fuse F1 isolates the circuit and provides protection from component failure. Bridge rectifier BR1 converts the AC line voltage into the DC voltage seen across capacitors C1 and C2. Another pi-filter is formed from common mode choke L1 and bulk capacitors C1 and C2, providing filtering for both common mode and differential mode noise.

4.2 *InnoSwitch3-CE Primary-Side*

The power transformer T1 is designed for a flyback topology power supply. The start winding of the transformer is connected to the DRAIN pin of the MOSFET inside the INN3164 IC, while the end of the winding is connected to the rectified DC bus. A low cost RCD clamp (consisting of diode D1, resistors R3 R4 R5, and capacitor C3) limit the primary drain to source voltage spike caused by the transformer leakage inductance. The RCD clamp values should be tuned to achieve optimized efficiency and standby power.

At start-up, U1 initially draws current from the DRAIN pin, through an internal high-voltage current source that charges the BPP pin capacitor C4. During normal operation, U1 draws current from the bias winding of T1. The bias winding is configured as a low voltage flyback winding which is rectified by diode D2 and capacitor C5. Resistor R7 limits the current supplied to the BPP pin.

4.3 *InnosSwitch3-CE Secondary-Side*

The secondary-side of the INN3164 provides output voltage sensing, output current sensing, and internal gate driver for a synchronous rectifier (SR) MOSFET. The secondary-side is powered by an internal 4.4 V regulator which draws current from either VOUT or FWD pin via current limiting resistors R21 and R9 respectively. Its output is connected to an external decoupling capacitor C9, also referred to as BPS capacitor.

The FWD pin also provides negative edge detection by sensing the transformer's secondary pin through resistor R9. The voltage sensed by the FWD pin is used for both the primary-secondary handshake at start-up, and for timing the turn-on instant of the SR FET Q1. This ensures quasi-resonant operation when operating at discontinuous conduction mode (DCM).

The SR FET Q1 is driven by U1 SR pin, through Schottky diode D3. Diode D3 and p-channel MOSFET Q2 form a fast turn-off circuit. Secondary RCD snubber (consisting of R10 C6 D4) limits the drain to source voltage spike across the SR FET.

The feedback network comprised of resistors R11 R12 R13 and capacitors C10 C12 is connected between the output voltage and secondary ground. The sensed voltage between R11 and R13 is connected to the FB pin. External current sense resistor R14 is connected between ISENSE pin and secondary ground pin.

Output capacitors C7 and C8 are selected to be low ESR type to provide output filtering and to ensure low output voltage ripple. An external OVP circuit (consisting of resistor R20 and Zener diode VR2) is connected between the output voltage and BP pin. In the event of an output overvoltage, VR2 will conduct and current will be injected into the BPS pin causing the device to enter latch mode operation.

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5 PCB Layout

DER-717 PCB is 1.6mm thick, 2oz copper and FR-4 material.

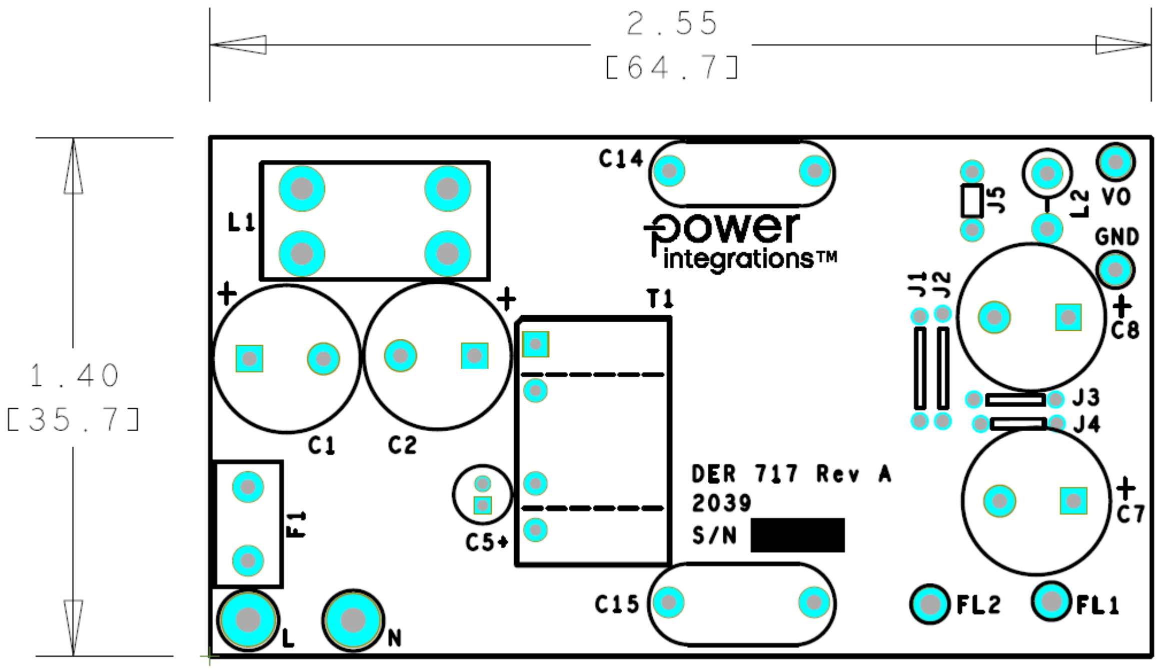

Figure 3 – Printed Circuit Board, Top View.

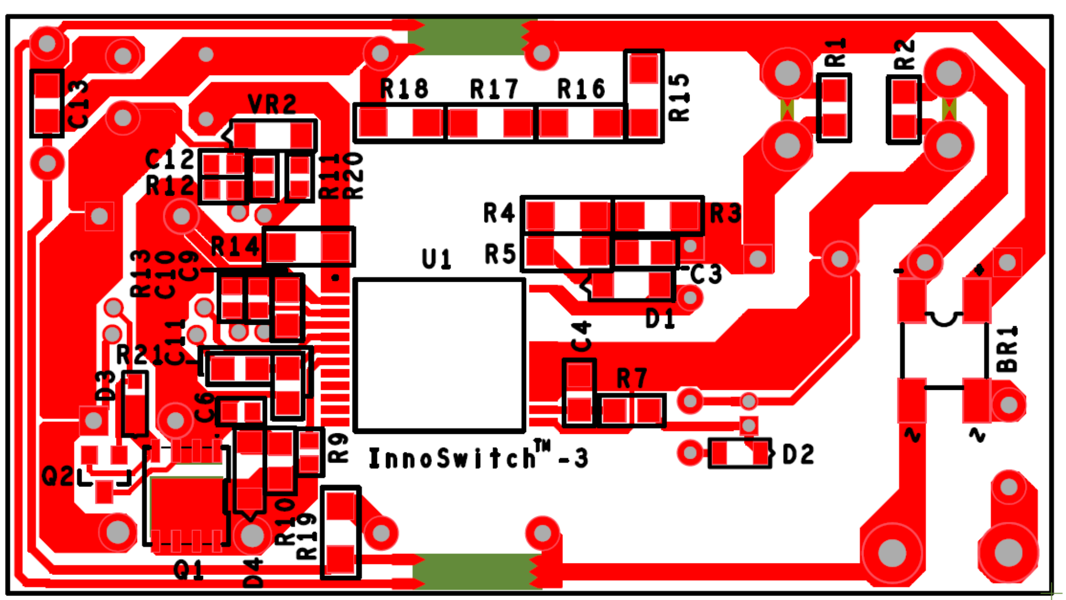

Figure 4 – Printed Circuit Board, Bottom View.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	BRIDGE RECT, 1PH, 1KV, 1.5A, 4-SMD	FTB10F-15FTR	SMC
2	1	C1	18 µF, 20%, 400 V, Electrolytic, Gen. Purpose, (10 x 16mm), 2000 Hrs @ 105°C	400AX18MEFC10X16	Rubycon
3	1	C2	18 µF, 20%, 400 V, Electrolytic, Gen. Purpose, (10 x 16mm), 2000 Hrs @ 105°C	400AX18MEFC10X16	Rubycon
4	1	C3	1 nF, 250 V, Ceramic, X7R, 0805	GRM21AR72E102KW01D	Murata
5	1	C4	0.47 µF, ±10%,25 V, Ceramic, X7R, 0805	CGA4J2X7R1E474K125AA	TDK
6	1	C5	10 µF, 20%, 50V, Aluminum, Radial, Can 2000 Hrs @ 105°C	UPW1H100MDD6	Nichicon
7	1	C6	1000 pF, 100 V, Ceramic, NP0, 0603	C1608C0G2A102J	TDK
8	1	C7	470 µF, 25 V, Electrolytic, Very Low ESR, 38 mΩ, (10 x 16)	EKZE250ELL471MJ16S	Nippon Chemi-Con
9	1	C8	470 µF, 25 V, Electrolytic, Very Low ESR, 38 mΩ, (10 x 16)	EKZE250ELL471MJ16S	Nippon Chemi-Con
10	1	C9	2.2 µF, 25 V, Ceramic, X7R, 0805	C2012X7R1E225M	TDK
11	1	C10	330 pF, ±5%, 50 V, Ceramic, C0G, NP0, 0603	C0603C331J5GACAUTO	KEMET
12	1	C11	2.2 µF, 25 V, Ceramic, X7R, 0805	C2012X7R1E225M	TDK
13	1	C12	47 nF 25 V, Ceramic, X7R, 0603	CC0603KRX7R8BB473	Yageo
14	1	C13	2.2 µF, 25 V, Ceramic, X7R, 0805	C2012X7R1E225M	TDK
15	1	C14	1 nF, Ceramic, Y1	440LD10-R	Vishay
16	1	C15	1 nF, Ceramic, Y1	440LD10-R	Vishay
17	1	D1	1 kV, 1 A, Standard Recovery, SMA	S1ML	TAIWAN SEMI
18	1	D2	100 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV19WS-7-F	Diodes, Inc.
19	1	D3	40 V, 1 A, POWERDI123	PD3S140-7	Diodes, Inc.
20	1	D4	1 kV, 1 A, Standard Recovery, SMA	S1ML	TAIWAN SEMI
21	1	F1	1 A, 250 V, Slow, Long Time Lag, RST 1	RST 1	Belfuse
22	1	L1	20 mH @ 10 kHz, 0.5 A, 500mA, DCR 1 Ω, CMC	744821120	Wurth
23	1	L2	3.5 mm x 4.45 mm, 56 Ω at 100 MHz, 22 AWG hole, Ferrite Bead	2761001112	Fair-Rite
24	1	Q1	MOSFET, N-Channel, 100 V, 46 A (Tc), 83 W (Tc), SMT, 8PDFN, 8-PDFN (5x6)	TSM160N10LCR RLG	Taiwan Semi
25	1	Q2	P-Channel 20 V 5 A (Ta) 1.5 W (Ta) Surface Mount SOT-23-3L, TO-236-3, SC-59, SOT-23-3	AO3415A	Alpha & Omega Semi
26	1	R1	RES, 4.7 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ472V	Panasonic
27	1	R2	RES, 4.7 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ472V	Panasonic
28	1	R3	RES, 220 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ224V	Panasonic
29	1	R4	RES, 150 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ151V	Panasonic
30	1	R5	RES, 150 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ151V	Panasonic
31	1	R7	RES, 3 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ302V	Panasonic
32	1	R9	RES, 47 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ470V	Panasonic
33	1	R10	RES, 10 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ100V	Panasonic
34	1	R11	RES, 100 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1003V	Panasonic
35	1	R12	RES, 10 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ103V	Panasonic
36	1	R13	RES, 11.5 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1152V	Panasonic
37	1	R14	0.015 Ω, ±1%, ±75ppm/°C, 1 W, 1206 Current Sense, -55°C ~ 155°C	ERJ-8CWFR015V	Panasonic
38	1	R15	RES, 10 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ106V	Panasonic
39	1	R16	RES, 10 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ106V	Panasonic
40	1	R17	RES, 10 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ106V	Panasonic
41	1	R18	RES, 10 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ106V	Panasonic

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42	1	R19	RES, 150 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ151V	Panasonic
43	1	R20	RES, 330 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ331V	Panasonic
44	1	R21	RES, 100 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ101V	Panasonic
45	1	T1	Bobbin, ATQ17/11.5, Horizontal, 10 pins. Mates with core 99-000xx-00.	TBI-238-26101.1206	TBI Transformer Bobbin Industrial
46	1	U1	InnoSwitch3-CE Switch Integrated Circuit, InSOP24D	INN3164C-H101	Power Integrations
47	1	VR2	Diode Zener 12 V 500 mW SOD123	MMSZ5242B-7-F	Diodes, Inc.

6.1 *Miscellaneous*

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	L	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone
2	1	N	Test Point, WHT, THRU-HOLE MOUNT	5012	Keystone
3	1	VO	Test Point, RED, Miniature THRU-HOLE MOUNT	5000	Keystone
4	1	GND	Test Point, BLK, Miniature THRU-HOLE MOUNT	5001	Keystone

7 Transformer Specification

7.1 *Electrical Diagram*

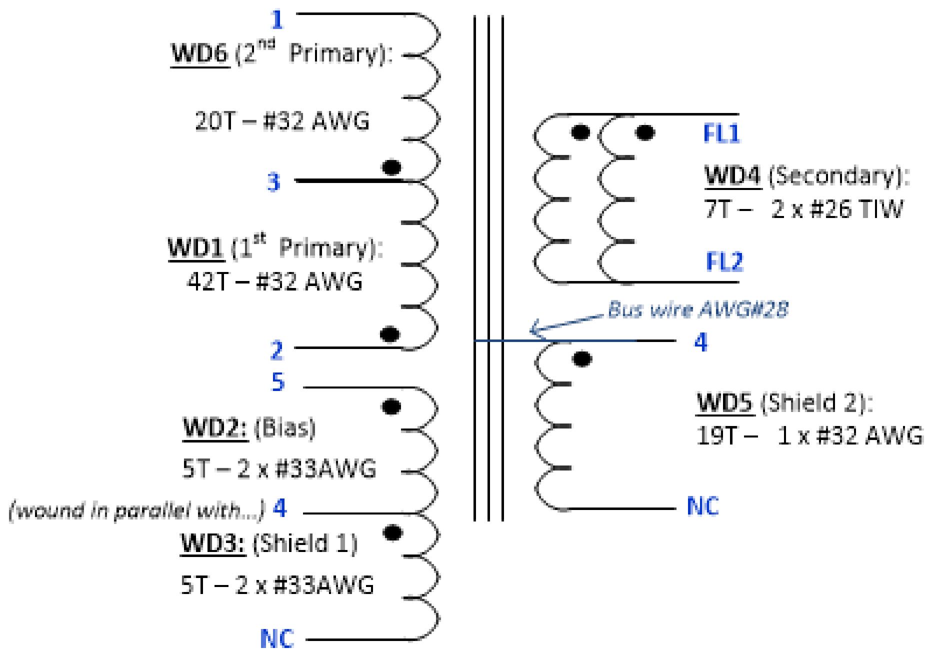

Figure 5 – Transformer Electrical Diagram.

7.2 *Electrical Specifications*

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V_{PK-PK}, 100 kHz switching frequency, between pin 4 and pin 5 with all other windings open.	1070 µH
Tolerance	Tolerance of Primary Inductance.	±5%
Leakage Inductance	Measured across primary winding with all other windings shorted.	<32 µH

7.3 *Material List*

Item	Description
[1]	Core: ATQ17.5/11.5.
[2]	Bobbin: ATQ17.5/11.5, Horizontal, 10 Pins, PI#25-01175-00.
[3]	Magnet Wire: #33 AWG.
[4]	Magnet Wire: #32 AWG.
[5]	Tripe Insulated Wire: #26 AWG.
[6]	Polyester Tape: 5.5 mm.
[7]	Polyester Tape: 9.5 mm.
[8]	Polyester Tape: 13 mm.
[9]	Varnish: Dolph BC 359 or Equivalent.
[10]	Bus Wire: #28 AWG, Alpha Wire, Tinned Copper, 40.0 mm Length.

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7.4 *Transformer Build Diagram*

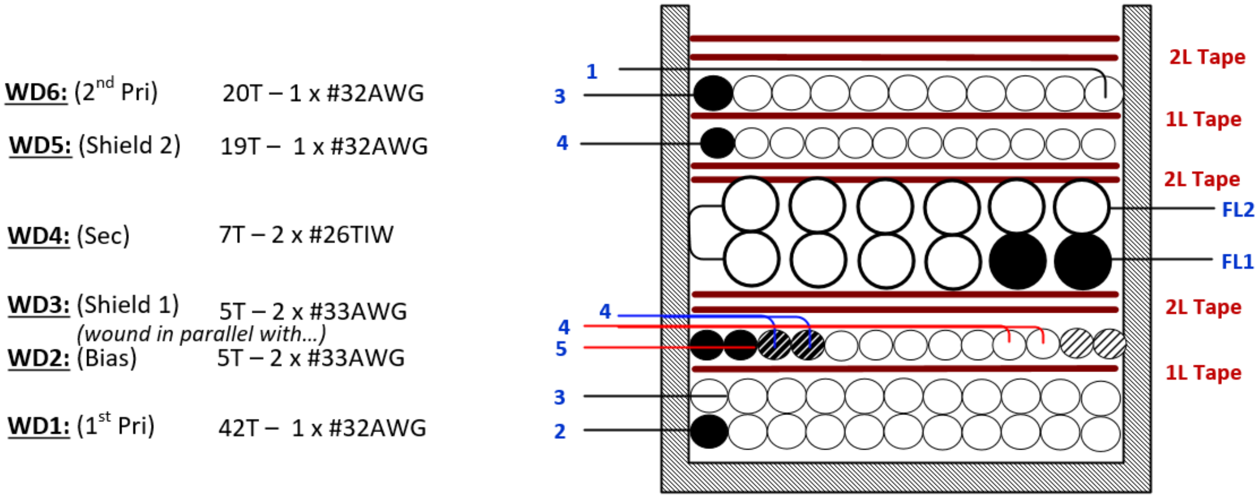
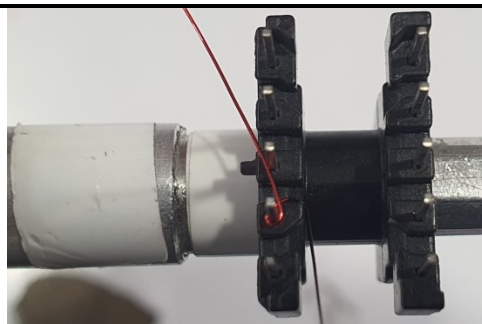
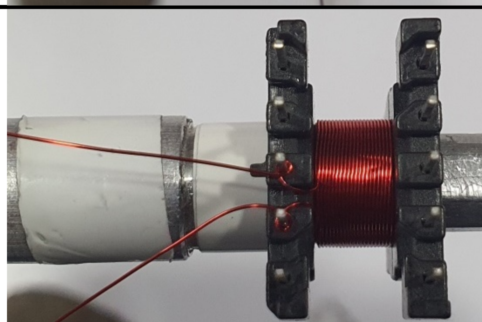
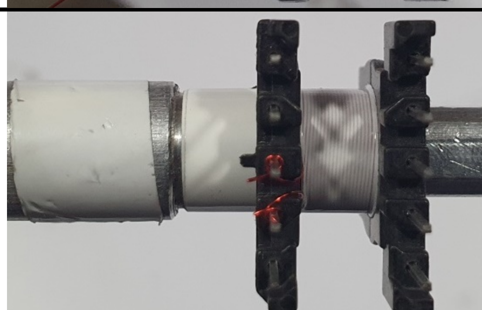
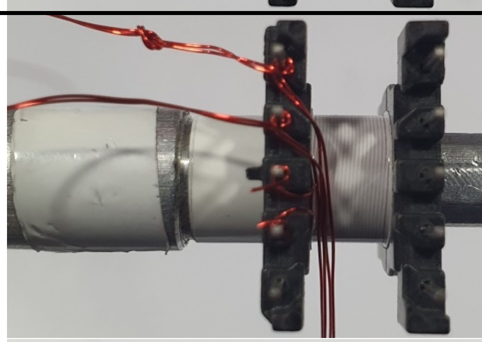
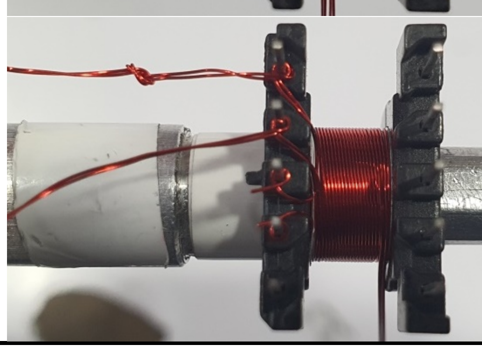


Figure 6 – Transformer Build Diagram.

7.5 *Transformer Instructions*

Bobbin Preparation	For the purposes of these instructions, bobbin is oriented on winder such that pin side is on the left side. Winding direction is clockwise.
WD1 1st Primary	Start at pin 2. Wind 42 turns of wire Item [4] in 2 layers. Finish at pin 3.
Insulation	1 layer of tape Item [6]
WD2 & WD3 Bias & Shield 1	Prepare 4 strands of wire Item [3]. For WD2, start 2 strands of wire Item [3] at pin 5. For WD3, start 2 strands of wire Item [3] at pin 4. Wind all wires 5 turns in parallel. Finish WD2 at pin 4. Cut WD3 at the end of the last turn with no connection.
Insulation	2 layers of tape Item [6]
WD4 Secondary	Start FL1 at the right side using two strands of TIW Item [5]. Wind 7 turns in 2 layers. For both FL1 and FL2, leave 50 mm length of wire.
Insulation	2 layers of tape Item [6]
WD5 Shield 2	Start at pin 4. Wind 19 turns of wire Item [4] in 1 layer. Finish the winding at the right side and cut the wire with no connection.
Insulation	1 layer of tape Item [6]
WD6 2nd Primary	Start at pin 3. Wind 20 turns of wire Item [4] in 1 layer. Finish at pin 1.
Insulation	2 layers of tape Item [6]
Bobbin Finish	Cut short pin 3. Remove pins 6-10, then trim bobbin as shown. Gap cores to get 1070 µH. Solder bus wire Item [10] to pin 4.
Tape Finish	Wrap 1 layer of tape Item [7] along the bobbin to secure the bus wire. Wrap 1 layer of tape Item [8] along the bottom side of the winding. Add another 1 layer of tape Item [8] along the bottom side of the winding. Wrap another 1 layer of tape Item [7] along the bobbin. Varnish using Item [9]. Twist FL1 and FL2 windings,

7.6 *Transformer Winding Illustrations*

Bobbin Preparation		For the purposes of these instructions, bobbin is oriented on winder such that pin side is on the left side. Winding direction is clockwise.
WD1 1st Primary		Start at pin 2. Wind 42 turns of wire Item [4] in 2 layers. Finish at pin 3.
Insulation		1 layer of tape Item [6]
WD2 & WD3 Bias & Shield 1	 	Prepare 4 strands of wire Item [3]. For WD2, start 2 strands of wire Item [3] at pin 5. For WD3, start 2 strands of wire Item [3] at pin 4. Wind all wires 5 turns in parallel. Finish WD2 at pin 4. Cut WD3 at the end of the last turn with no connection.

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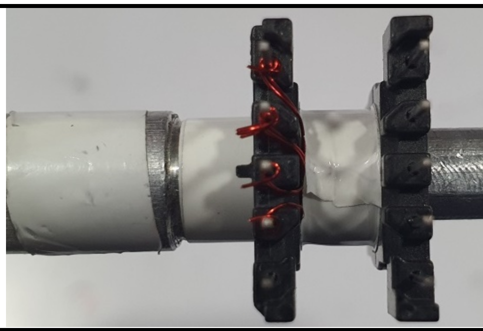
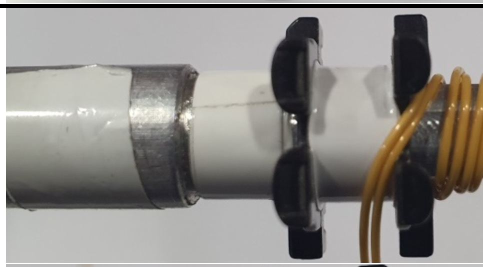
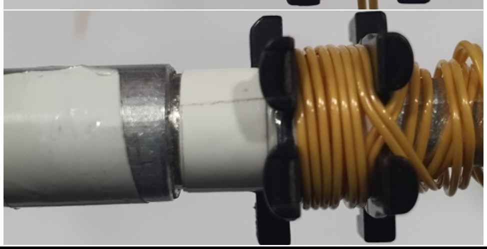
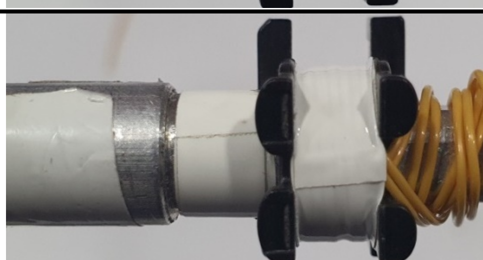
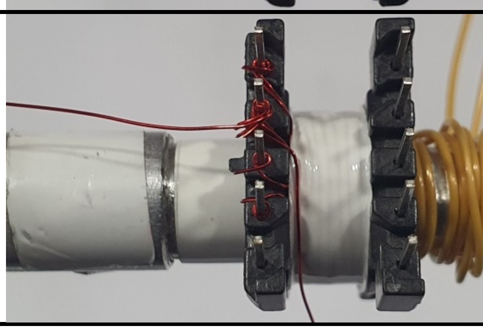
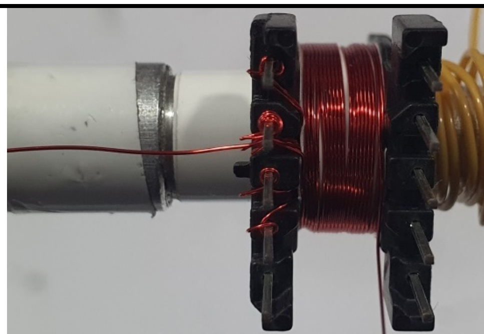
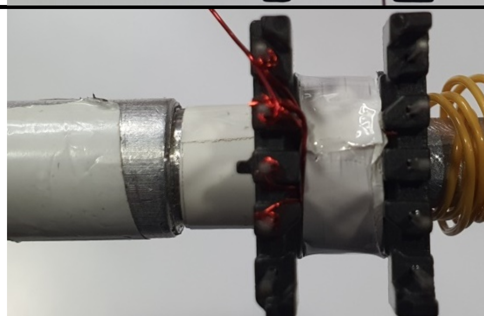
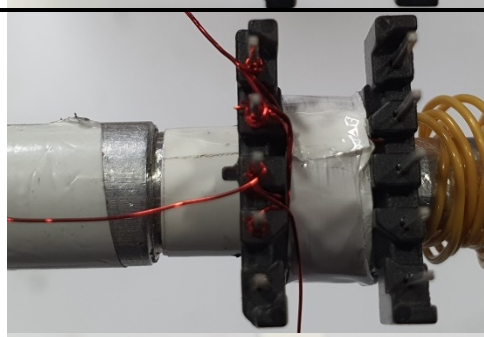
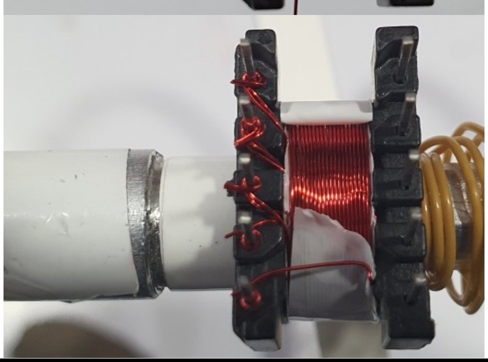
Insulation		2 layers of tape Item [6]
WD4 Secondary	 	Start FL1 at the right side using two strands of TIW Item [5]. Wind 7 turns in 2 layers. For both FL1 and FL2, leave 50 mm length of wire.
Insulation		2 layers of tape Item [6]
WD5 Shield 2		Start at pin 4. Wind 19 turns of wire Item [4] in 1 layer. Finish the winding at the right side and cut the wire with no connection.

<table>
<tr><td></td><td></td><td></td></tr>
<tr><td>Insulation</td><td></td><td>1 layer of tape Item [6]</td></tr>
<tr><td>WD6
2nd Primary</td><td>
</td><td>Start at pin 3. Wind 20 turns of wire Item [4] in 1 layer. Finish at pin 1.</td></tr>
<tr><td>Insulation</td><td></td><td>2 layers of tape Item [6]</td></tr>
</table>

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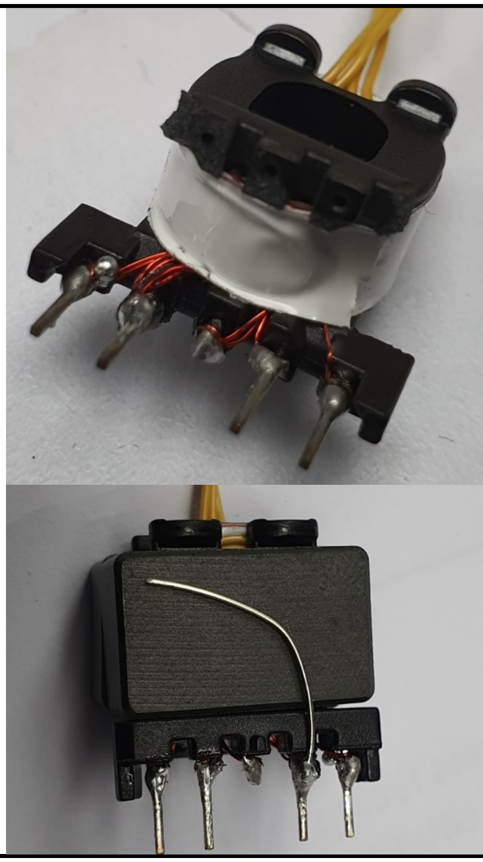
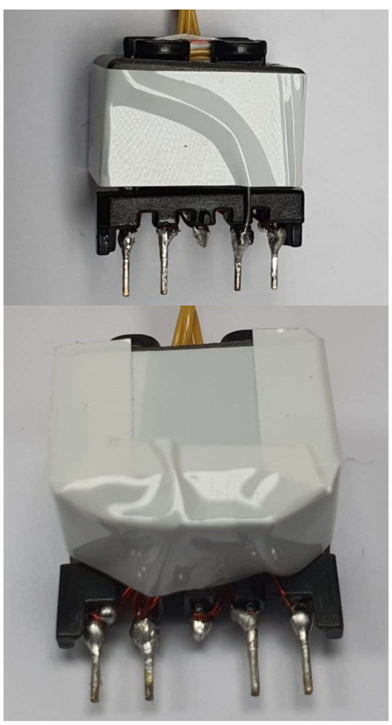
Bobbin Finish		Cut short pin 3. Remove pins 6-10, then trim bobbin as shown. Gap cores to get 1070 µH. Solder bus wire Item [10] to pin 4.
Tape Finish		Wrap 1 layer of tape Item [7] along the bobbin to secure the bus wire. Wrap 1 layer of tape Item [8] along the bottom side of the winding.

	 	Add another 1 layer of tape Item [8] along the bottom side of the winding. Wrap another 1 layer of tape Item [7] along the bobbin. Varnish using Item [9]. Twist FL1 and FL2 windings,

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8 Transformer Design Spreadsheet

ACDC_InnoSwitch3-CE_Flyback_090320; Rev.1.5; Copyright Power Integrations 2020	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3 CE Flyback Design Spreadsheet
APPLICATION VARIABLES					
VIN_MIN	90		90	V	Minimum AC input voltage
VIN_MAX	265		265	V	Maximum AC input voltage
VIN_RANGE			UNIVERSAL		Range of AC input voltage
LINEFREQ			60	Hz	AC Input voltage frequency
CAP_INPUT	36.0		36.0	uF	Input capacitor
VOUT	12.00		12.00	V	Output voltage at the board
CDC	0		0	mV	Cable drop compensation desired at full load
IOUT	1.250		1.250	A	Output current
POUT			15.00	W	Output power
EFFICIENCY			0.89		AC-DC efficiency estimate at full load given that the converter is switching at the valley of the rectified minimum input AC voltage
FACTOR_Z			0.50		Z-factor estimate
ENCLOSURE	ADAPTER		ADAPTER		Power supply enclosure
PRIMARY CONTROLLER SELECTION					
ILIMIT_MODE	STANDARD		STANDARD		Device current limit mode
DEVICE_GENERIC	INN31X4		INN31X4		Generic device code
DEVICE_CODE			INN3164C		Actual device code
POUT_MAX			15	W	Power capability of the device based on thermal performance
RDSON_100DEG			5.70		

IPEDESTAL_PRIMARY			0.000	A	Primary switch current pedestal
IAVG_PRIMARY			0.160	A	Primary switch average current
IRIPPLE_PRIMARY			0.744	A	Primary switch ripple current
IRMS_PRIMARY			0.282	A	Primary switch RMS current
SECONDARY CURRENT					
IPEAK_SECONDARY			6.591	A	Secondary winding peak current
IPEDESTAL_SECONDARY			0.000	A	Secondary winding current pedestal
IRMS_SECONDARY			2.418	A	Secondary winding RMS current
TRANSFORMER CONSTRUCTION PARAMETERS					
CORE SELECTION					
CORE	ATQ17/11.5A	Info	ATQ17/11.5A		The transformer windings may not fit: pick a bigger core or bobbin and refer to the Transformer Parameters tab for fit calculations
CORE CODE			ATQ17/11.5A		Core code
AE			40.20	mm^2	Core cross sectional area
LE			31.40	mm	Core magnetic path length
AL			3740	nH/turns^2	Ungapped core effective inductance
VE			1262.0	mm^3	Core volume
BOBBIN			TBI-238-26101.1206		Bobbin
AW			13.26	mm^2	Window area of the bobbin
BW			5.10	mm	Bobbin width
MARGIN			0.0	mm	Safety margin width (Half the primary to secondary creepage distance)
PRIMARY WINDING					
NPRIMARY			62		Primary turns
BPEAK			3710	Gauss	Peak flux density
BMAX			3313	Gauss	Maximum flux density
BAC			1656	Gauss	AC flux density (0.5 x Peak to Peak)
ALG			279	nH/turns^2	Typical gapped core effective inductance
LG			0.168	mm	Core gap length
LAYERS_PRIMARY			3		Number of primary layers
AWG_PRIMARY			32	AWG	Primary winding wire AWG
OD_PRIMARY_INSULATED			0.244	mm	Primary winding wire outer diameter with insulation
OD_PRIMARY_BARE			0.202	mm	Primary winding wire outer diameter without insulation
CMA_PRIMARY			224	Cmil/A	Primary winding wire CMA
SECONDARY WINDING					
NSECONDARY	7		7		Secondary turns
AWG_SECONDARY			23	AWG	Secondary winding wire AWG
OD_SECONDARY_INSULATED			0.879	mm	Secondary winding wire outer diameter with insulation
OD_SECONDARY_BARE			0.573	mm	Secondary winding wire outer diameter without insulation
CMA_SECONDARY			211	Cmil/A	Secondary winding wire CMA
BIAS WINDING					
NBIAS			8		Bias turns
PRIMARY COMPONENTS SELECTION					
LINE UNDERVOLTAGE					
BROWN-IN REQURED			72.0	V	Required AC RMS line voltage brown-in threshold
RLS			3.64		Connect two 1.82 MOhm resistors to the V-pin for the required UV/OV threshold
BROWN-IN ACTUAL			73.0	V	Actual AC RMS brown-in threshold
BROWN-OUT ACTUAL			66.0	V	Actual AC RMS brown-out threshold
LINE OVERVOLTAGE					
OVERVOLTAGE_LINE			304.2	V	The device voltage stress will be higher

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					than 585V when overvoltage is trigerred
BIAS DIODE					
VBIAS			12.0	V	Rectified bias voltage
VF_BIAS			0.70	V	Bias winding diode forward drop
VREVERSE_BIASDIODE			60.18	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
CBIAS			22	uF	Bias winding rectification capacitor
CBPP			0.47	uF	BPP pin capacitor
SECONDARY COMPONENTS					
RFB_UPPER			100.00		Upper feedback resistor (connected to the first output voltage)
RFB_LOWER			11.80		Lower feedback resistor
CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor
MULTIPLE OUTPUT PARAMETERS					
OUTPUT 1					
VOUT1			12.00	V	Output 1 voltage
IOUT1			1.25	A	Output 1 current
POUT1			15.00	W	Output 1 power
IRMS_SECONDARY1			2.418	A	Root mean squared value of the secondary current for output 1
IRIPPLE_CAP_OUTPUT1			2.070	A	Current ripple on the secondary waveform for output 1
AWG_SECONDARY1			23	AWG	Wire size for output 1
OD_SECONDARY1_INSULATED			0.879	mm	Secondary winding wire outer diameter with insulation for output 1
OD_SECONDARY1_BARE			0.573	mm	Secondary winding wire outer diameter without insulation for output 1
CM_SECONDARY1			484	Cmils	Bare conductor effective area in circular mils for output 1
NSECONDARY1			7		Number of turns for output 1
VREVERSE_RECTIFIER1			54.15	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 1
SRFET1	Auto		AOD2816		Secondary rectifier (Logic MOSFET) for output 1
VF_SRFET1			0.036	V	SRFET on-time drain voltage for output 1
VBREAKDOWN_SRFET1			80	V	SRFET breakdown voltage for output 1
RDSON_SRFET1			29.0		SRFET on-time drain resistance at 25degC and VGS=4.4V for output 1
PO_TOTAL			15.00	W	Total power of all outputs
NEGATIVE OUTPUT	N/A		N/A		If negative output exists, enter the output number; e.g. If VO2 is negative output, select 2
TOLERANCE ANALYSIS					
USER_VAC	115		115	V	Input AC RMS voltage corner to be evaluated
USER_ILIMIT	TYP		0.750	A	Current limit corner to be evaluated
USER_LPRIMARY	TYP		1071.4	uH	Primary inductance corner to be evaluated
MODE_OPERATION			DCM		Mode of operation
KP			1.586		Measure of continuous/discontinuous mode of operation
FSWITCHING			60195	Hz	Switching frequency at full load and valley of the rectified minimum AC input voltage
VMIN			141.55	V	Valley of the minimum input AC voltage at full load
DUTYCYCLE			0.322		Steady state duty cycle
TIME_ON			5.34	us	Primary switch on-time
TIME_OFF			11.27	us	Primary switch off-time

IPEAK_PRIMARY			0.703	A	Primary switch peak current
IPEDESTAL_PRIMARY			0.000	A	Primary switch current pedestal
IAVERAGE_PRIMARY			0.113	A	Primary switch average current
IRIPPLE_PRIMARY			0.703	A	Primary switch ripple current
IRMS_PRIMARY			0.230	A	Primary switch RMS current
BPEAK			3300	Gauss	Peak flux density
BMAX			3021	Gauss	Maximum flux density
BAC			1511	Gauss	AC flux density (0.5 x Peak to Peak)

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9 Performance Data

9.1 *Efficiency*

9.1.1 Active Mode Measurement Data

Measured Performance				Standards		
		V_{IN} (VAC)		DOE6	EC CoC (v5)	
		115	230		2014 Tier 1	2016 Tier 2
		Efficiency (%)				
Load (%)	**10**	87.00	85.25		71.55	74.5
	25	90.04	89.54			
	50	90.98	91.14			
	75	91.05	91.53			
	100	90.98	91.78			
	Ave	**90.76**	**91.00**	84.13	81.55	84.5
No-Load Input Power (mW)		**15**	**15**	100	150	75
			Compliant	Y	Y	Y

9.1.2 Full Load Efficiency vs. Line

Test Condition: Soak for 15 minutes for each line.

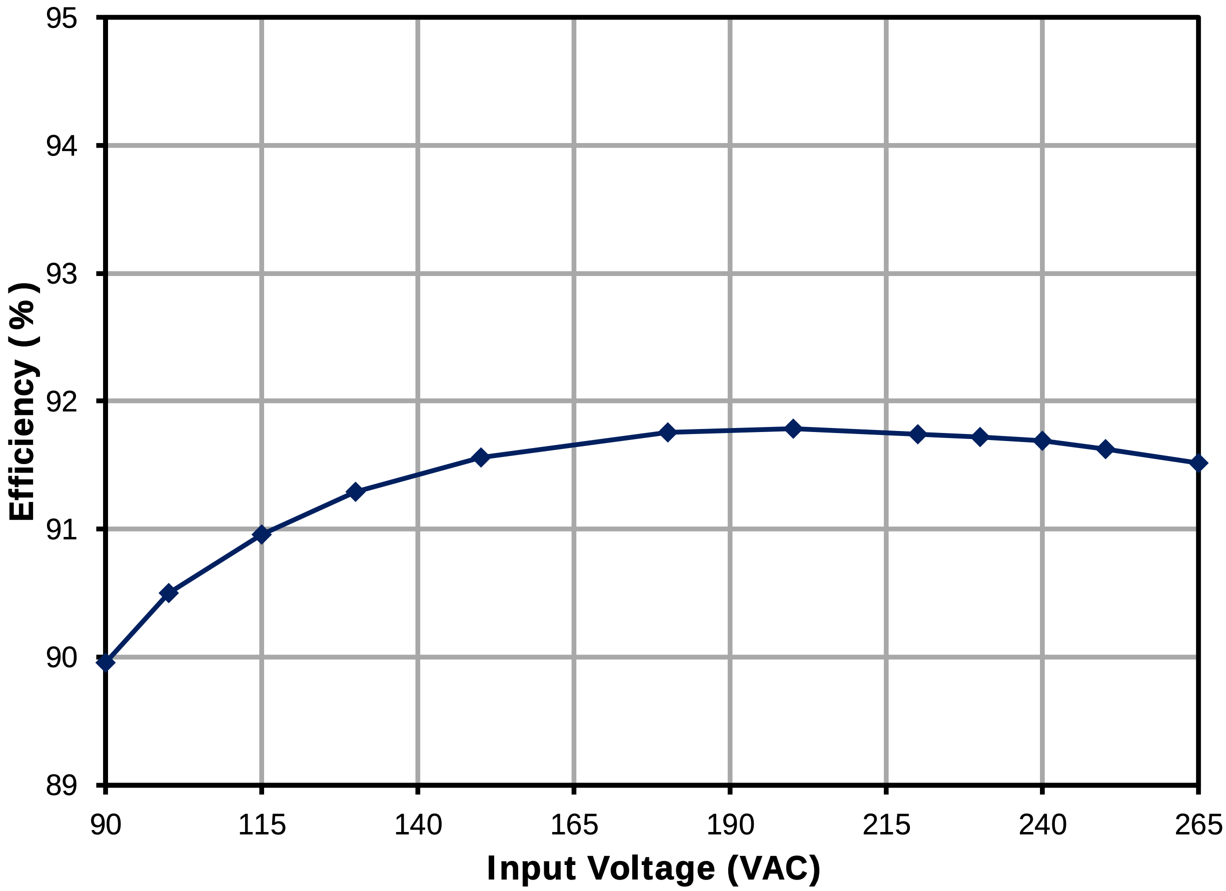

Figure 7 – Full Load Efficiency vs. Line.

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9.1.3 Efficiency vs. Load

Test Condition: Soak for 15 minutes each line, and 5 minutes for each load.

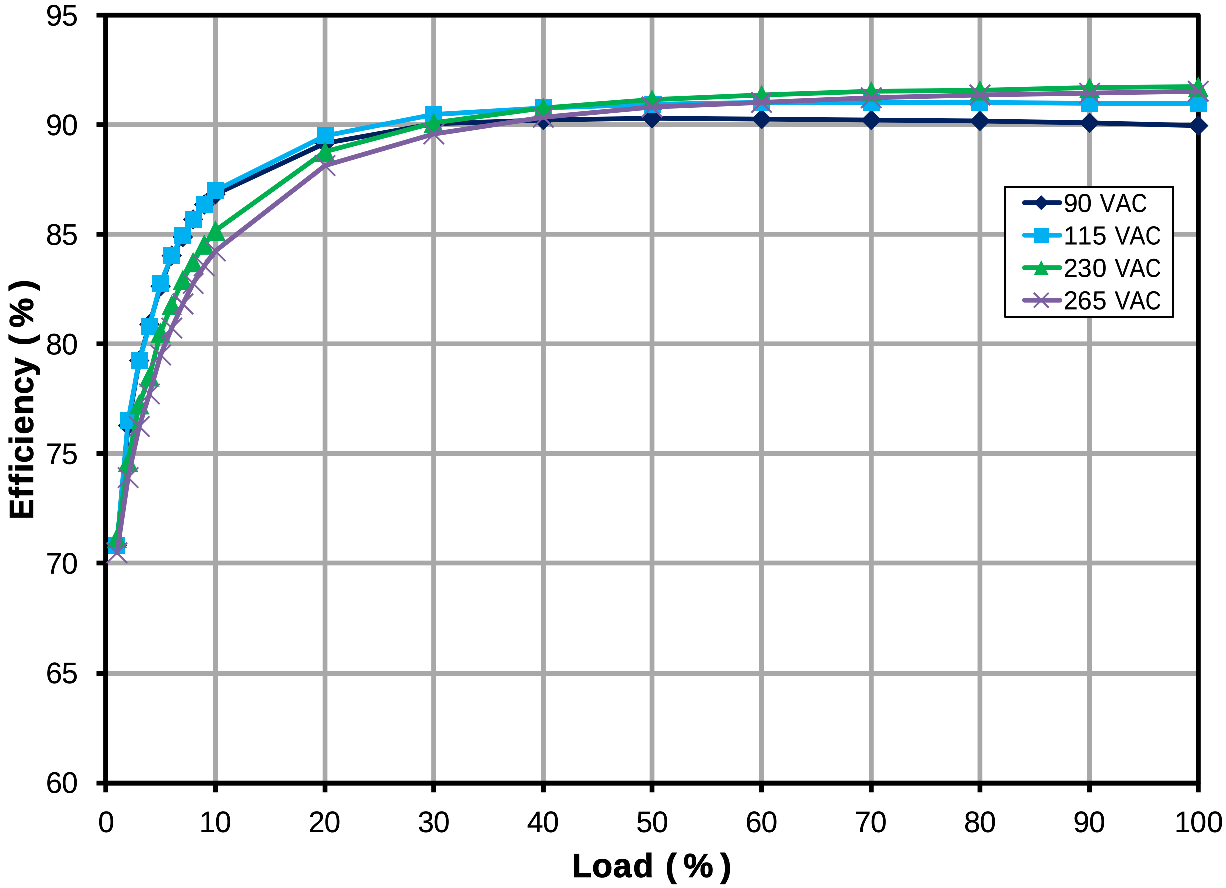

Figure 8 – Efficiency vs. Percentage Load.

9.2 *Available Standby Output Power*

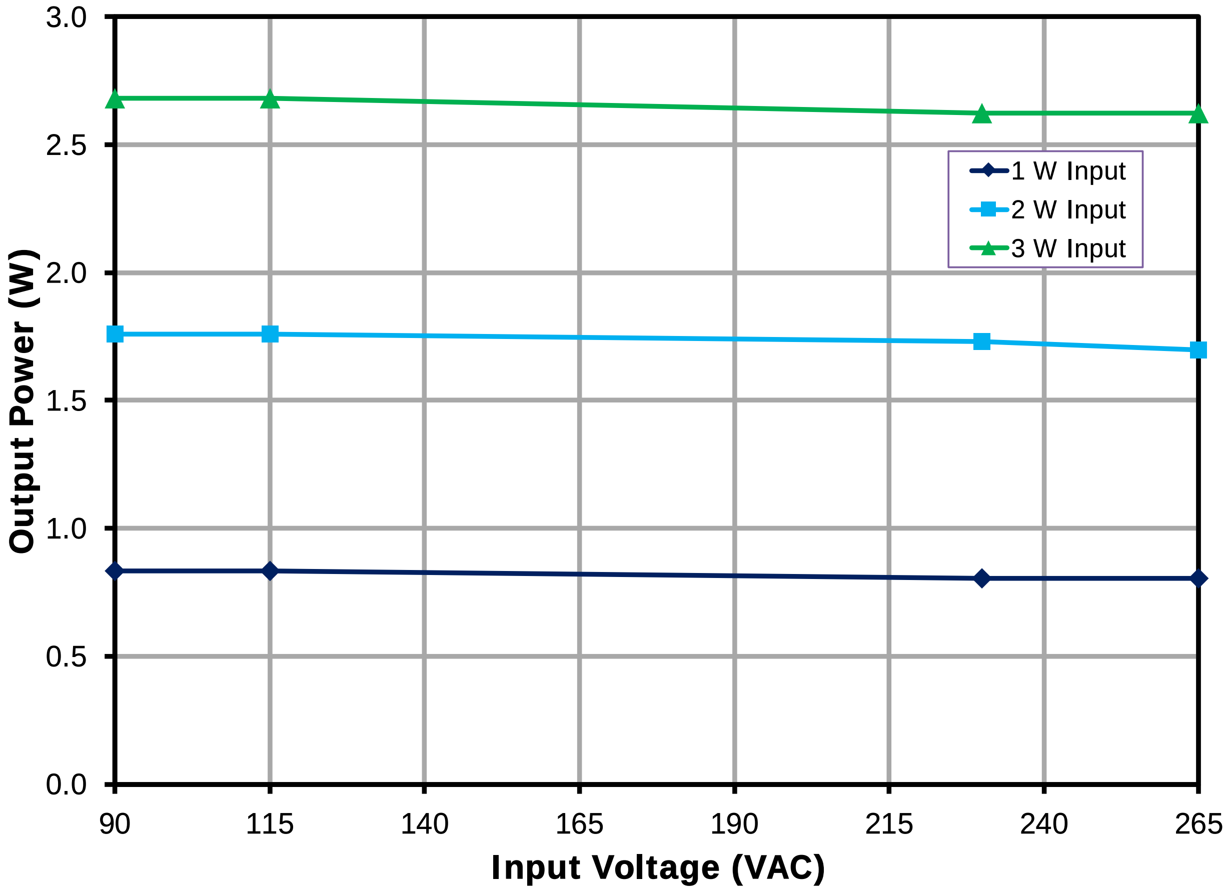

Figure 9 – Available Standby Output Power for 1 W, 2 W and 3 W Input Power.

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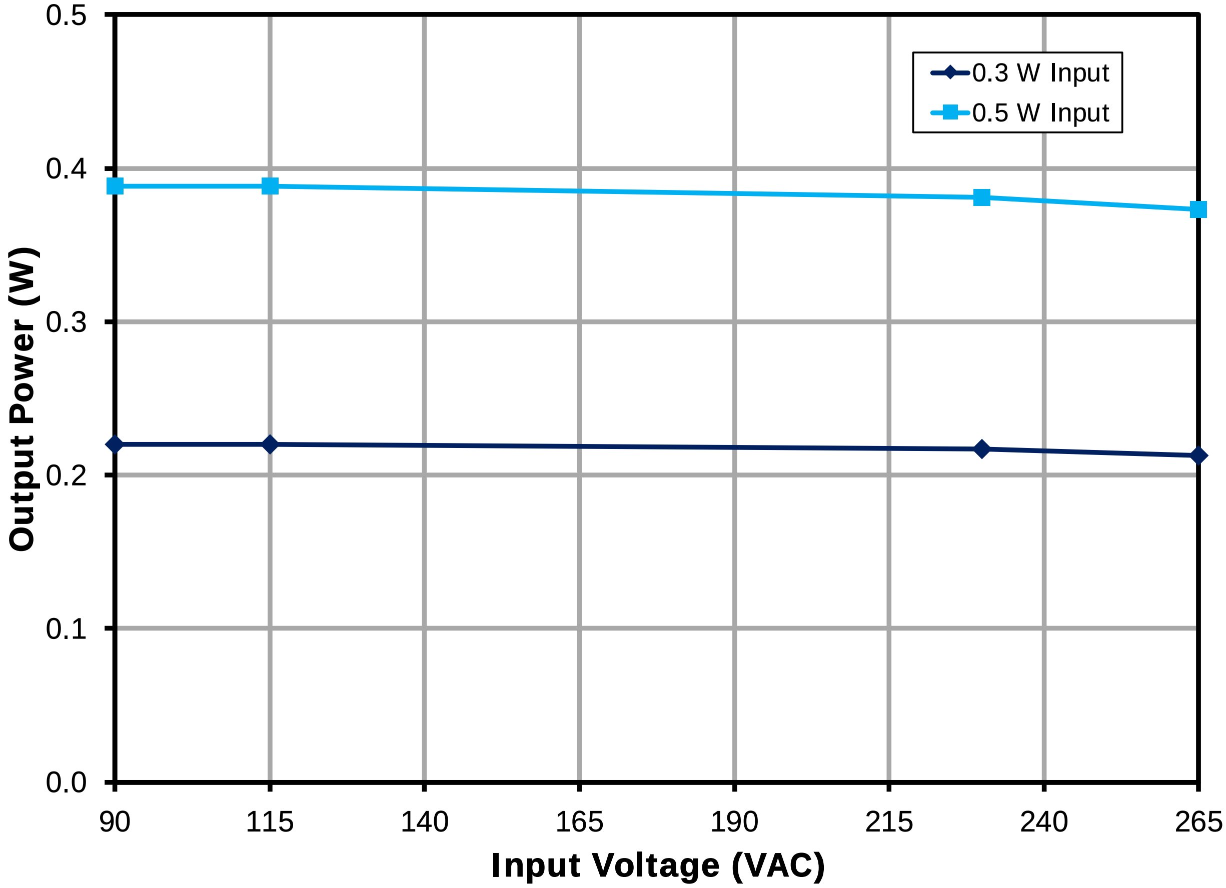

Figure 10 – Available Standby Output Power for 0.3 W and 0.5 W Input Power.

9.3 *No-Load Input Power*

Test Condition: Soak for 15 minutes each line and 1 minute integration time.

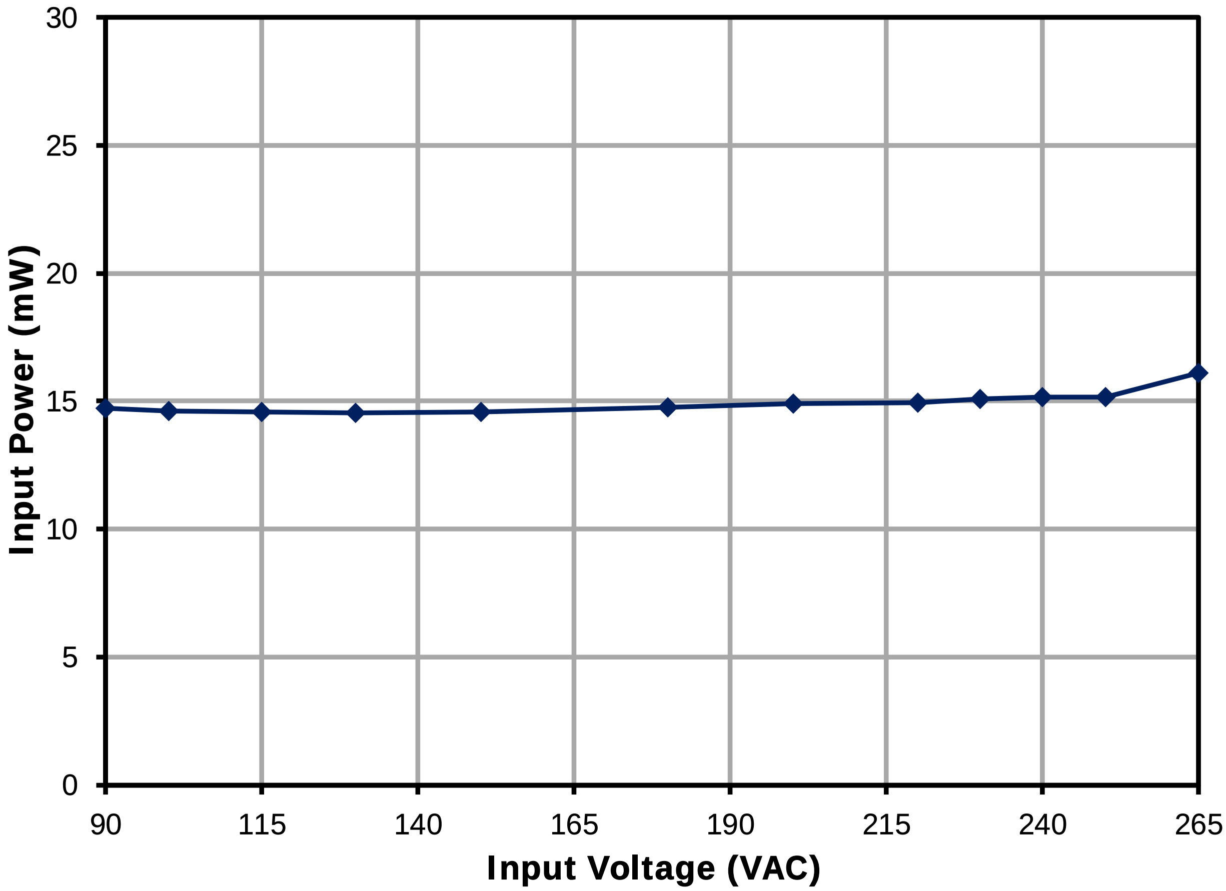

Figure 11 – No-Load Input Power vs. Line at Room Temperature.

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9.4 *Line Regulation*

Test Condition: Soak for 15 minutes for each line.

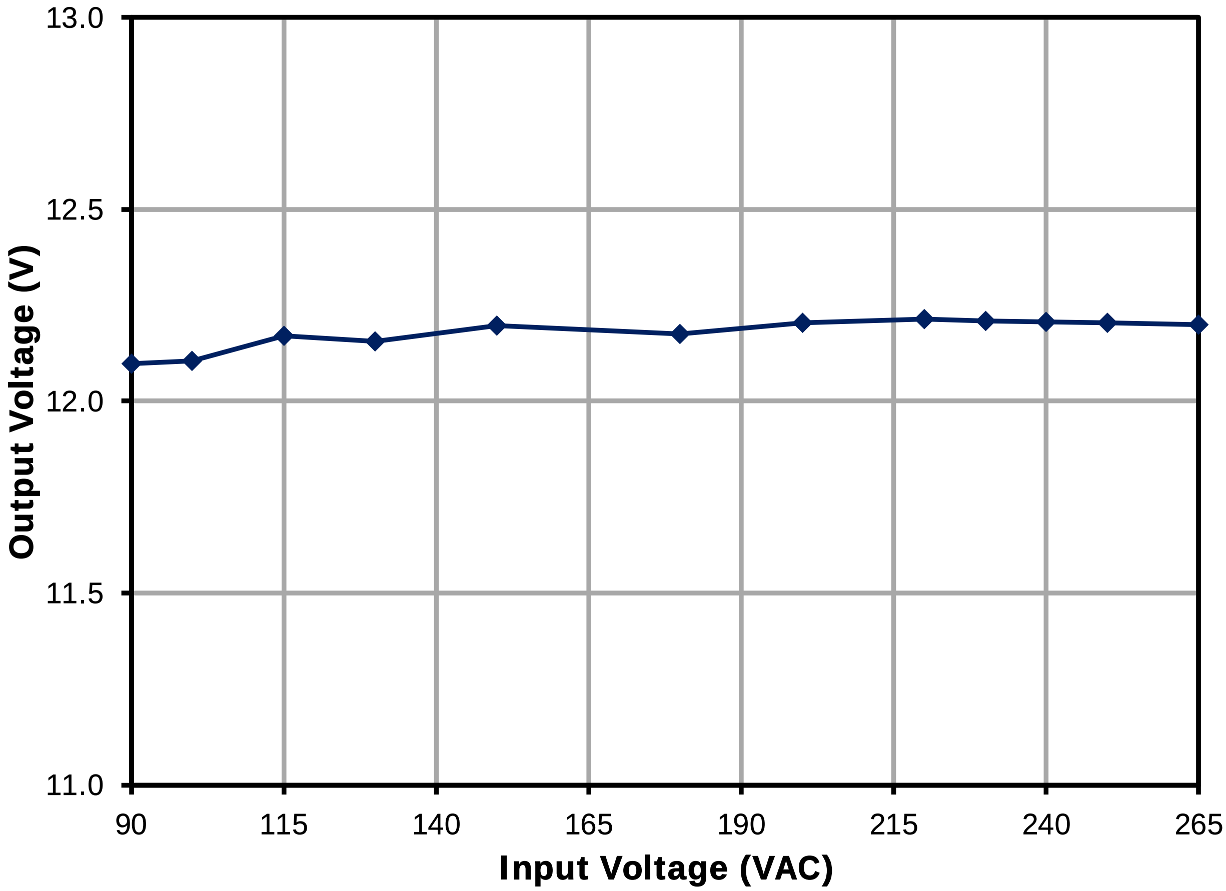

Figure 12 – Output Voltage vs. Line Voltage.

9.5 *Load Regulation*

Test Condition: Soak for 15 minutes each line, and 5 minutes for each load.

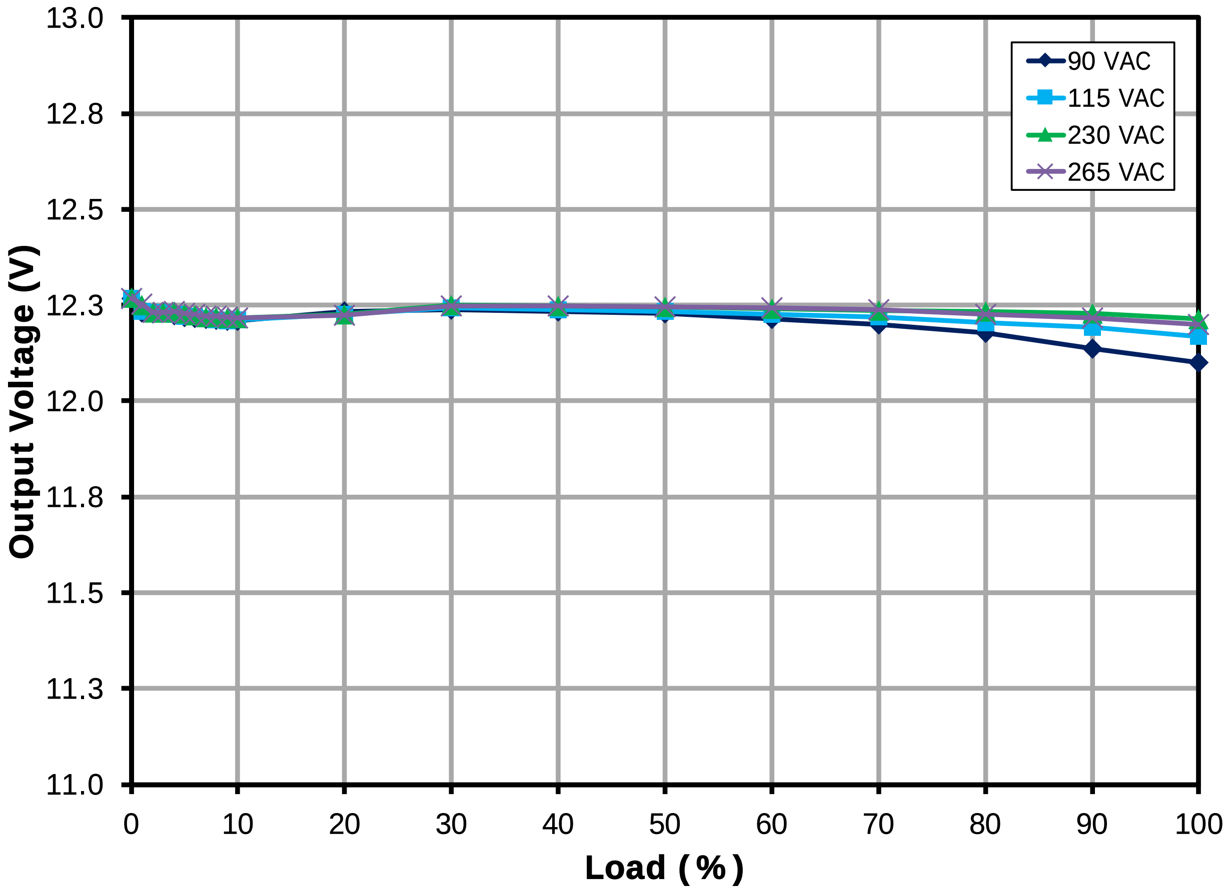

Figure 13 – Output Voltage vs. Percent Load.

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10 Waveforms

10.1 *Load Transient Response*

Test Condition: Dynamic load frequency = 1 kHz, duty cycle = 50 %

10.1.1 0% - 100% Load Change

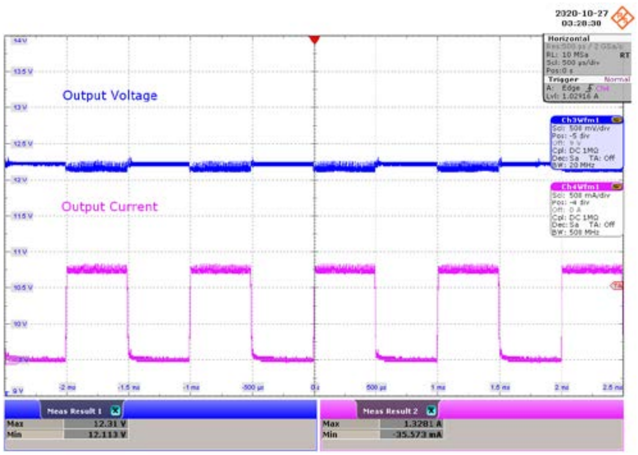

Figure 14 – 90 VAC 60 Hz.
CH3: V_{OUT}, 500 mV / div., 500 µs / div.
CH4: I_{OUT}, 500 mA / div., 500 µs / div.
V_{MAX}: 12.31 V, V_{MIN}: 12.113 V.

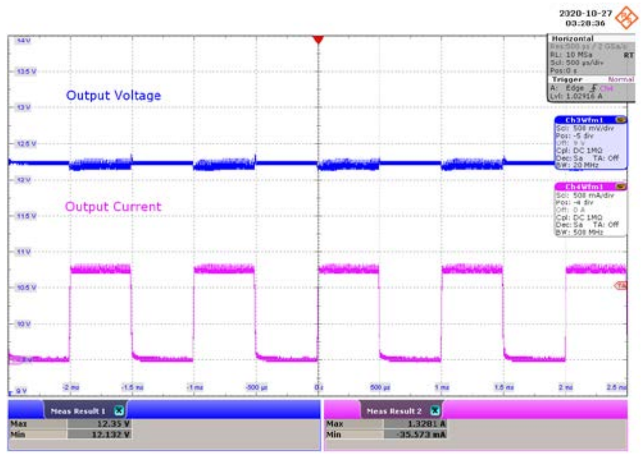

Figure 15 – 115 VAC 60 Hz.
CH3: V_{OUT}, 500 mV / div., 500 µs / div.
CH4: I_{OUT}, 500 mA / div., 500 µs / div.
V_{MAX}: 12.35 V, V_{MIN}: 12.132 V.

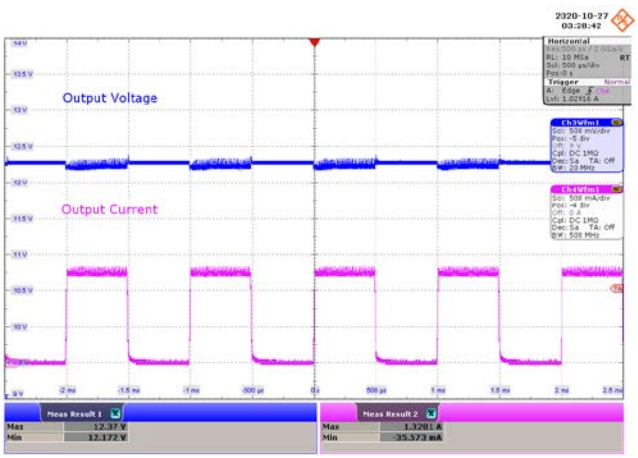

Figure 16 – 230 VAC 50 Hz.
CH3: V_{OUT}, 500 mV / div., 500 µs / div.
CH4: I_{OUT}, 500 mA / div., 500 µs / div.
V_{MAX}: 12.37 V, V_{MIN}: 12.172 V.

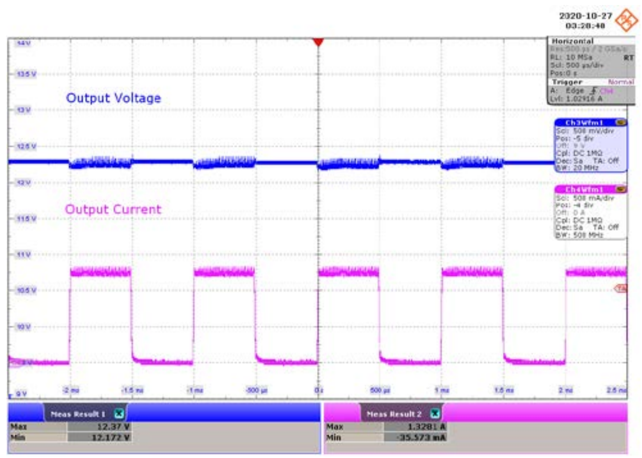

Figure 17 – 265 VAC 50 Hz.
CH3: V_{OUT}, 500 mV / div., 500 µs / div.
CH4: I_{OUT}, 500 mA / div., 500 µs / div.
V_{MAX}: 12.37 V, V_{MIN}: 12.172 V.

10.1.2 50% - 100% Load Change

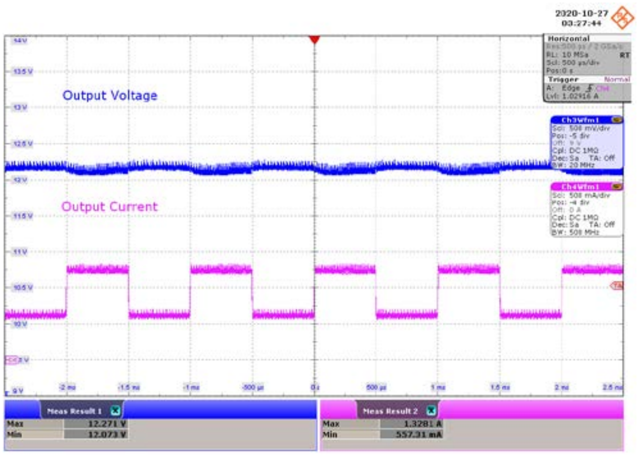

Figure 18 – 90 VAC 60 Hz.
CH3: V_{OUT}, 500 mV / div., 500 µs / div.
CH4: I_{OUT}, 500 mA / div., 500 µs / div.
V_{MAX}: 12.271 V, V_{MIN}: 12.073 V.

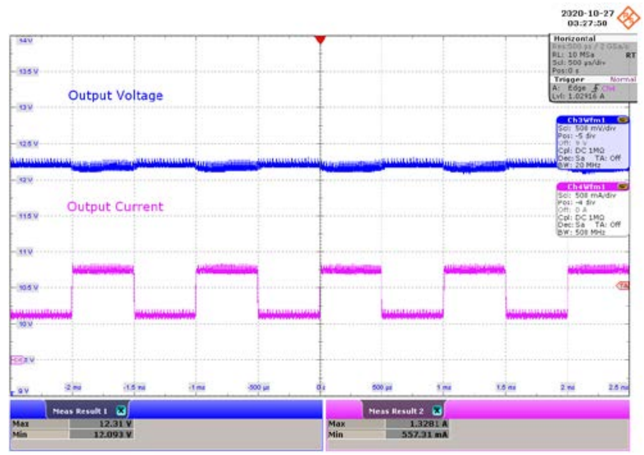

Figure 19 – 115 VAC 60 Hz.
CH3: V_{OUT}, 500 mV / div., 500 µs / div.
CH4: I_{OUT}, 500 mA / div., 500 µs / div.
V_{MAX}: 12.31 V, V_{MIN}: 12.093 V.

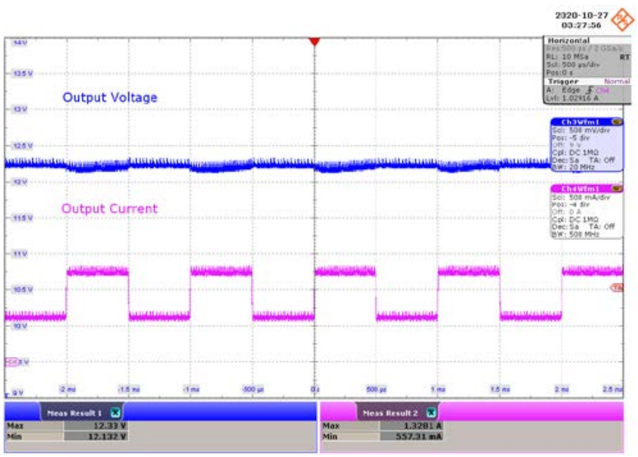

Figure 20 – 230 VAC 50 Hz.
CH3: V_{OUT}, 500 mV / div., 500 µs / div.
CH4: I_{OUT}, 500 mA / div., 500 µs / div.
V_{MAX}: 12.33 V, V_{MIN}: 12.132 V.

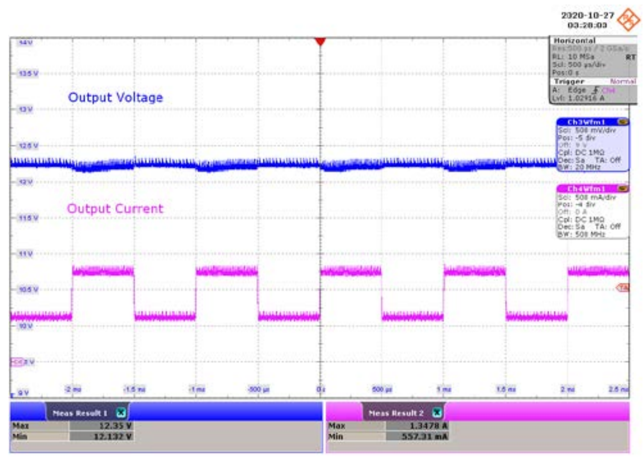

Figure 21 – 265 VAC 50 Hz.
CH3: V_{OUT}, 500 mV / div., 500 µs / div.
CH4: I_{OUT}, 500 mA / div., 500 µs / div.
V_{MAX}: 12.35 V, V_{MIN}: 12.132 V.

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10.2 *Output Voltage at Start-up*

10.2.1 CC Mode

10.2.1.1 100% Load

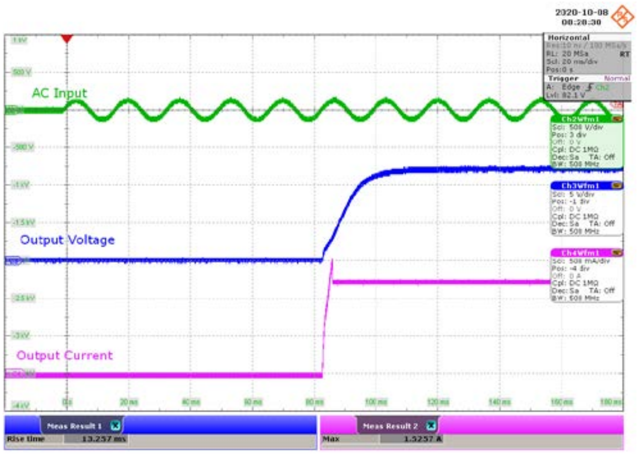

Figure 22 – 90 VAC 60 Hz.
CH2: $V_{IN,}$ 500 V / div., 20 ms / div.
CH3: $V_{OUT,}$ 5 V / div., 20 ms / div.
CH4: I_{OUT}, 500 mA / div., 20 ms / div.
Rise Time = 13.257 ms.

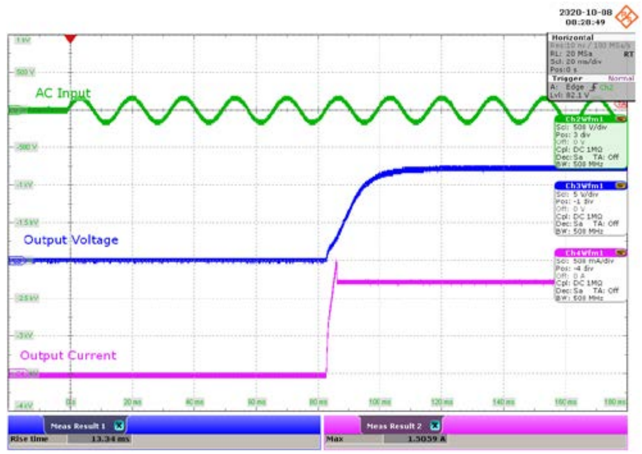

Figure 23 – 115 VAC 60 Hz.
CH2: $V_{IN,}$ 500 V / div., 20 ms / div.
CH3: $V_{OUT,}$ 5 V / div., 20 ms / div.
CH4: I_{OUT}, 500 mA / div., 20 ms / div.
Rise Time = 13.34 ms.

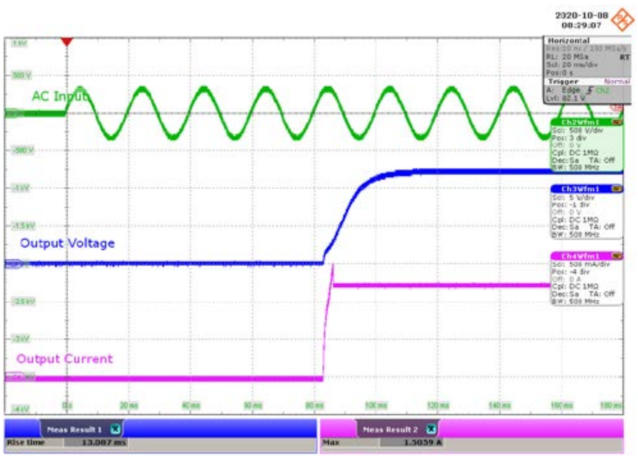

Figure 24 – 230 VAC 50 Hz.
CH2: $V_{IN,}$ 500 V / div., 20 ms / div.
CH3: $V_{OUT,}$ 5 V / div., 20 ms / div.
CH4: I_{OUT}, 500 mA / div., 20 ms / div.
Rise Time = 13.087 ms.

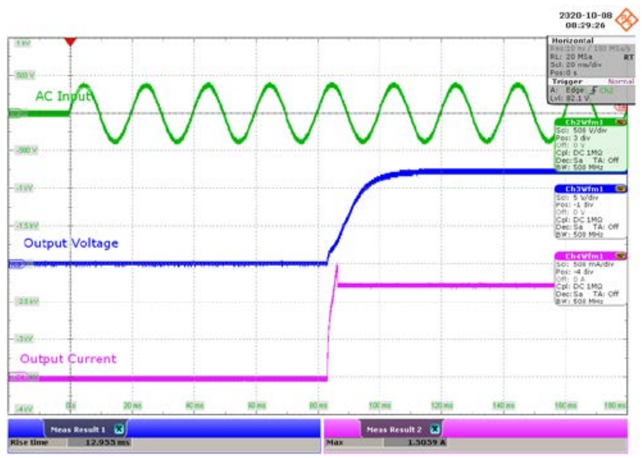

Figure 25 – 265 VAC 50 Hz.
CH2: $V_{IN,}$ 500 V / div., 20 ms / div.
CH3: $V_{OUT,}$ 5 V / div., 20 ms / div.
CH4: I_{OUT}, 500 mA / div., 20 ms / div.
Rise Time = 12.955 ms.

10.2.1.2 0% Load

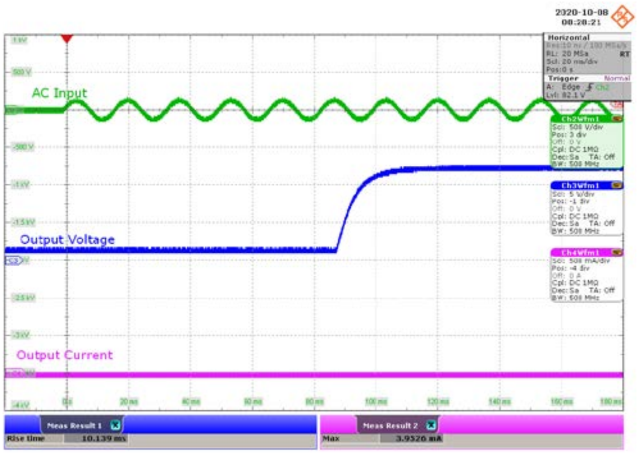

Figure 26 – 90 VAC 60 Hz.
CH2: V_{IN}, 500 V / div., 20 ms / div.
CH3: V_{OUT}, 5 V / div., 20 ms / div.
CH4: I_{OUT}, 500 mA / div., 20 ms / div.
Rise Time = 10.139 ms.

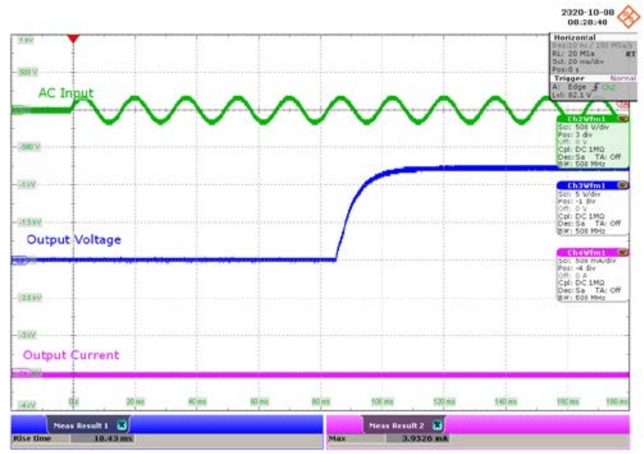

Figure 27 – 115 VAC 60 Hz.
CH2: V_{IN}, 500 V / div., 20 ms / div.
CH3: V_{OUT}, 5 V / div., 20 ms / div.
CH4: I_{OUT}, 500 mA / div., 20 ms / div.
Rise Time = 10.43 ms.

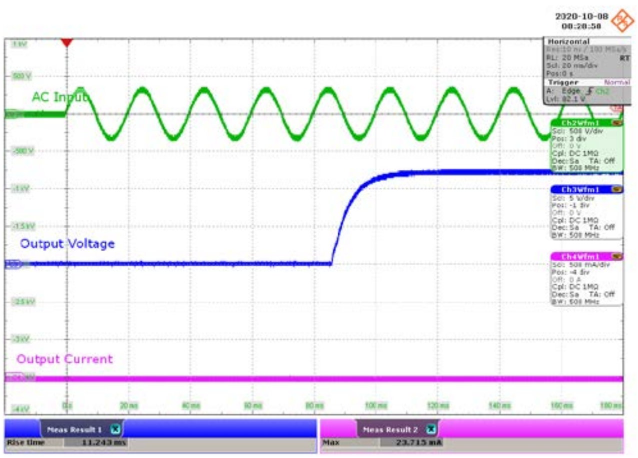

Figure 28 – 230 VAC 50 Hz.
CH2: V_{IN}, 500 V / div., 20 ms / div.
CH3: V_{OUT}, 5 V / div., 20 ms / div.
CH4: I_{OUT}, 500 mA / div., 20 ms / div.
Rise Time = 11.243 ms.

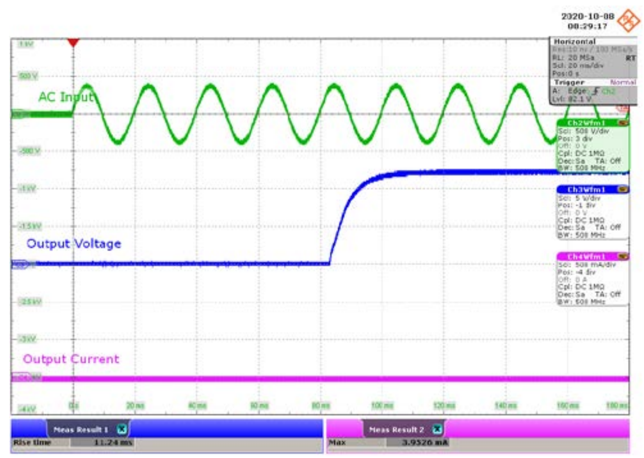

Figure 29 – 265 VAC 50 Hz.
CH2: V_{IN}, 500 V / div., 20 ms / div.
CH3: V_{OUT}, 5 V / div., 20 ms / div.
CH4: I_{OUT}, 500 mA / div., 20 ms / div.
Rise Time = 11.24 ms.

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10.2.2 CR Mode

10.2.2.1 100% Load

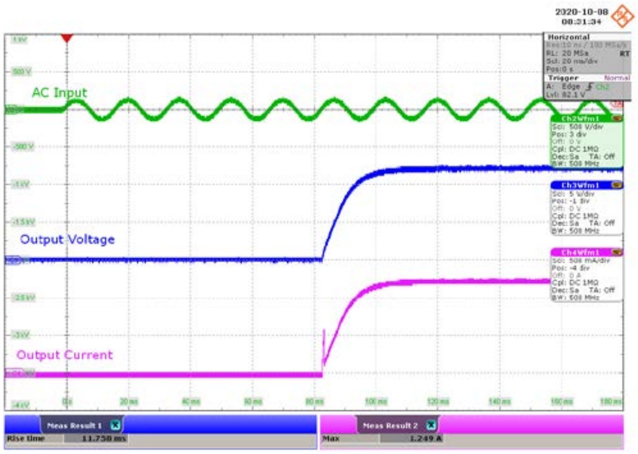

Figure 30 – 90 VAC 60 Hz.
CH2: V_{IN}, 500 V / div., 20 ms / div.
CH3: V_{OUT}, 5 V / div., 20 ms / div.
CH4: I_{OUT}, 500 mA / div., 20 ms / div.
Rise Time = 11.758 ms.

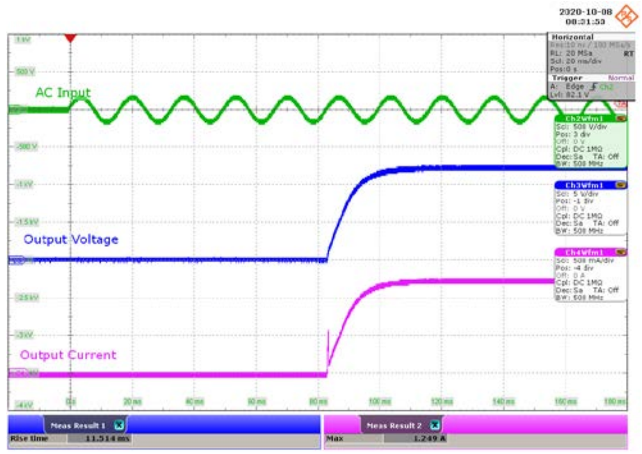

Figure 31 – 115 VAC 60 Hz.
CH2: V_{IN}, 500 V / div., 20 ms / div.
CH3: V_{OUT}, 5 V / div., 20 ms / div.
CH4: I_{OUT}, 500 mA / div., 20 ms / div.
Rise Time = 11.514 ms.

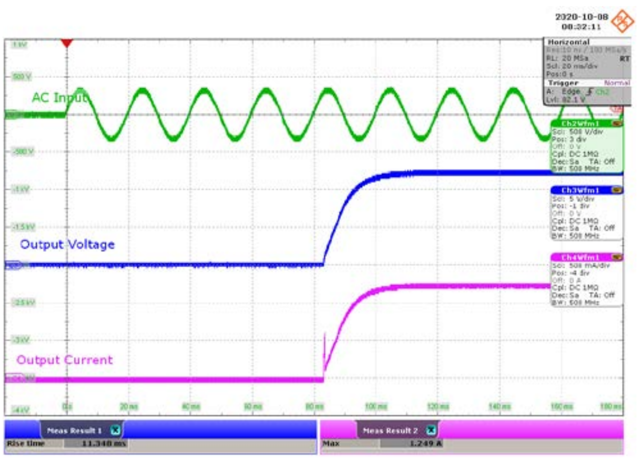

Figure 32 – 230 VAC 50 Hz.
CH2: V_{IN}, 500 V / div., 20 ms / div.
CH3: V_{OUT}, 5 V / div., 20 ms / div.
CH4: I_{OUT}, 500 mA / div., 20 ms / div.
Rise Time = 11.348 ms.

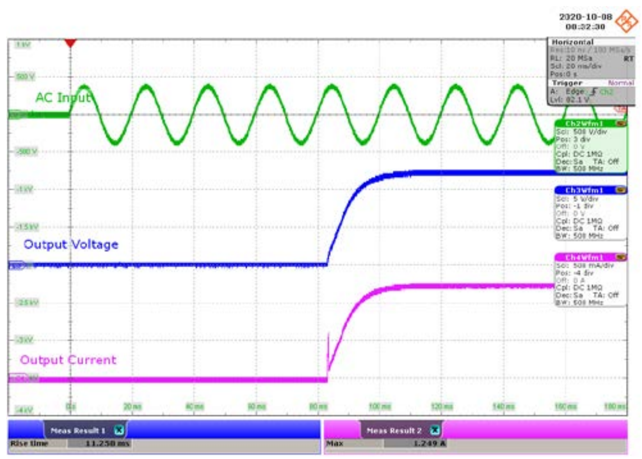

Figure 33 – 265 VAC 50 Hz.
CH2: V_{IN}, 500 V / div., 20 ms / div.
CH3: V_{OUT}, 5 V / div., 20 ms / div.
CH4: I_{OUT}, 500 mA / div., 20 ms / div.
Rise Time = 11.258 ms.

10.2.2.2 0% Load

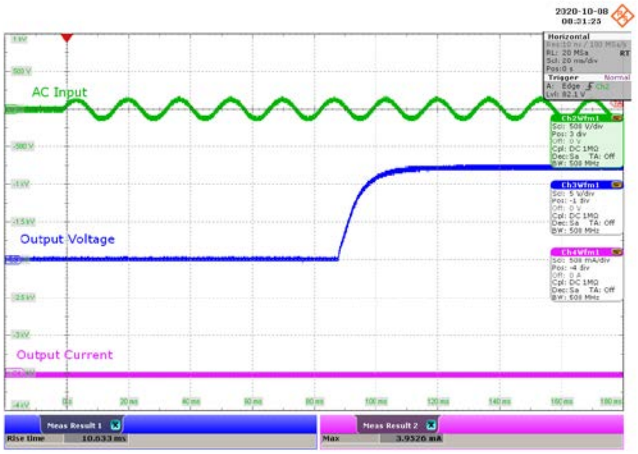

Figure 34 – 85 VAC 60 Hz.
CH2: V_{IN}, 500 V / div., 20 ms / div.
CH3: V_{OUT}, 5 V / div., 20 ms / div.
CH4: I_{OUT}, 500 mA / div., 20 ms / div.
Rise Time = 10.633 ms.

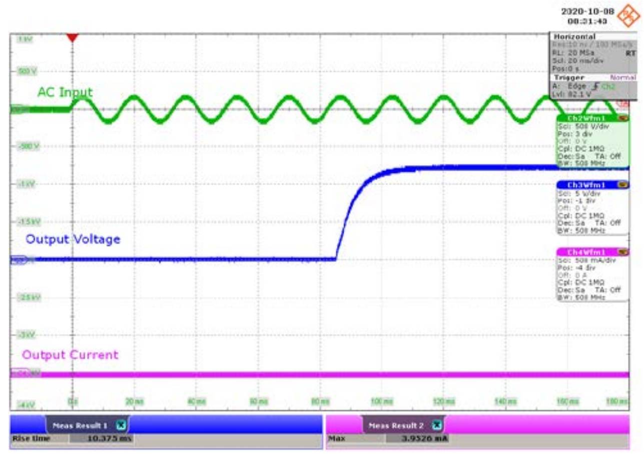

Figure 35 – 115 VAC 60 Hz.
CH2: V_{IN}, 500 V / div., 20 ms / div.
CH3: V_{OUT}, 5 V / div., 20 ms / div.
CH4: I_{OUT}, 500 mA / div., 20 ms / div.
Rise Time = 10.375 ms.

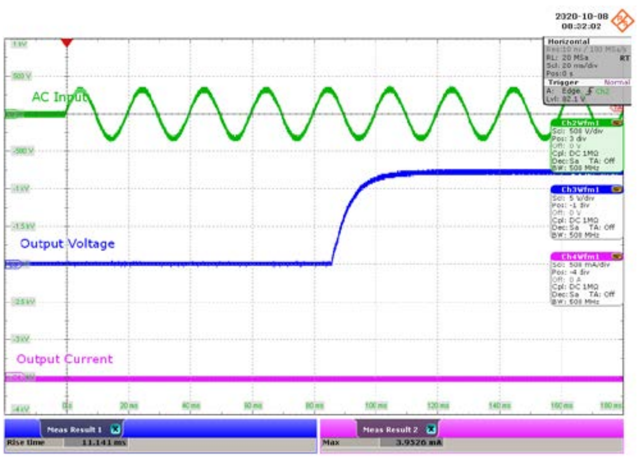

Figure 36 – 230 VAC 50 Hz.
CH2: V_{IN}, 500 V / div., 20 ms / div.
CH3: V_{OUT}, 5 V / div., 20 ms / div.
CH4: I_{OUT}, 500 mA / div., 20 ms / div.
Rise Time = 11.141 ms.

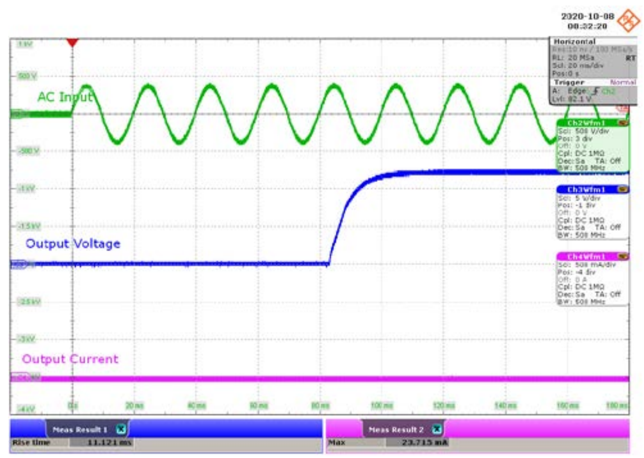

Figure 37 – 265 VAC 50 Hz.
CH2: V_{IN}, 500 V / div., 20 ms / div.
CH3: V_{OUT}, 5 V / div., 20 ms / div.
CH4: I_{OUT}, 500 mA / div., 20 ms / div.
Rise Time = 11.121 ms.

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10.3 *Switching Waveforms*

10.3.1 Primary MOSFET Drain-Source Voltage and Current at Normal Operation

10.3.1.1 100% Load

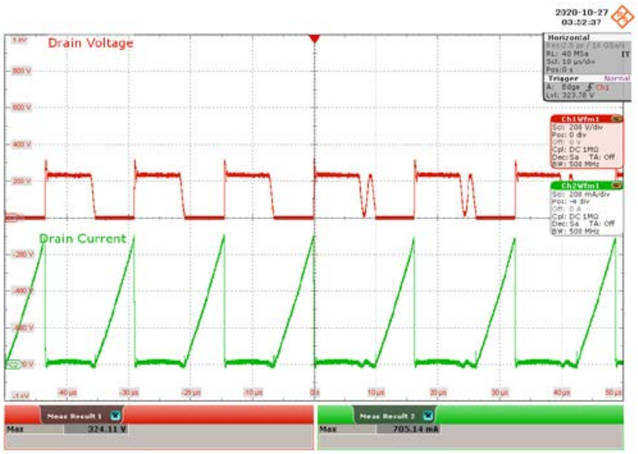

Figure 38 – 90 VAC 60 Hz.
CH1: $V_{DS,}$ 200 V / div., 10 µs / div.
CH2: $I_{DS,}$ 200 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 324.11 V.
$I_{DS(MAX)}$ = 705.14 mA.

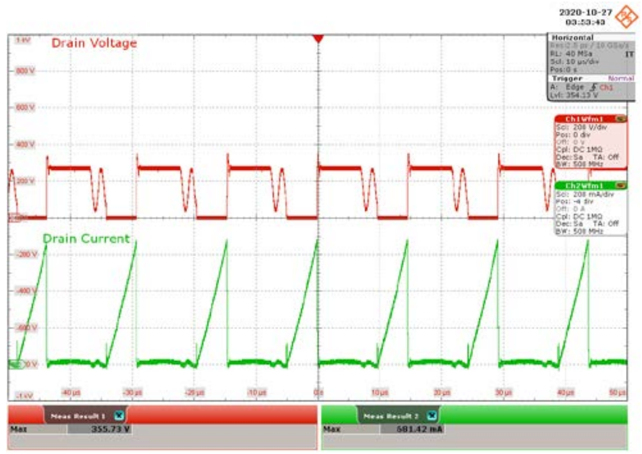

Figure 39 – 115 VAC 60 Hz.
CH1: $V_{DS,}$ 200 V / div., 10 µs / div.
CH2: $I_{DS,}$ 200 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 355.73 V.
$I_{DS(MAX)}$ = 681.42 mA.

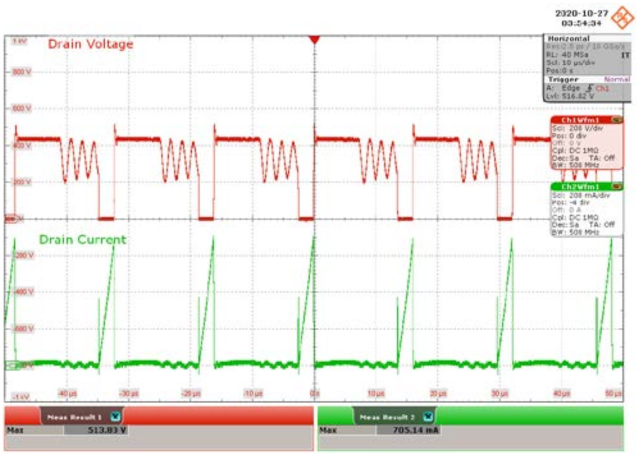

Figure 40 – 230 VAC 50 Hz.
CH1: $V_{DS,}$ 200 V / div., 10 µs / div.
CH2: $I_{DS,}$ 200 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 513.83 V.
$I_{DS(MAX)}$ = 705.14 mA.

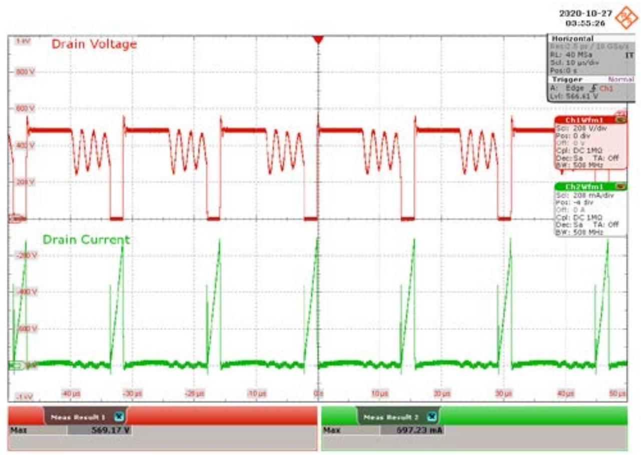

Figure 41 – 265 VAC 50 Hz.
CH1: $V_{DS,}$ 200 V / div., 10 µs / div.
CH2: $I_{DS,}$ 200 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 569.17 V.
$I_{DS(MAX)}$ = 697.23 mA.

10.3.1.2 0% Load

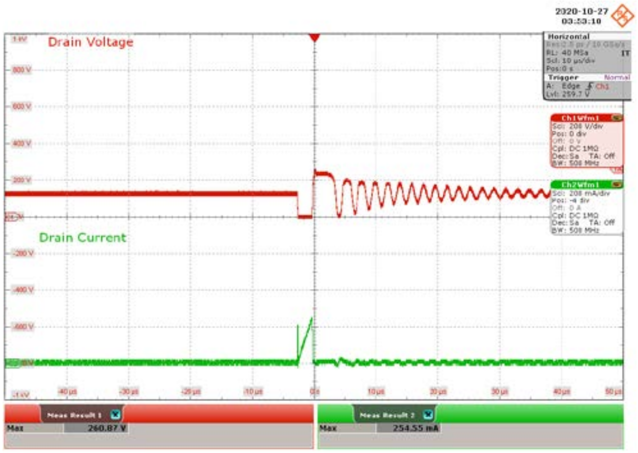

Figure 42 – 90 VAC 60 Hz.
CH1: $V_{DS,}$ 200 V / div., 10 µs / div.
CH2: $I_{DS,}$ 200 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 260.87 V.
$I_{DS(MAX)}$ = 254.55 mA.

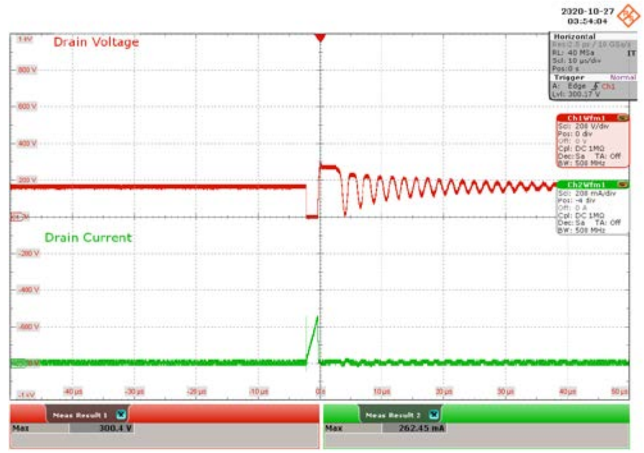

Figure 43 – 115 VAC 60 Hz.
CH1: $V_{DS,}$ 200 V / div., 10 µs / div.
CH2: $I_{DS,}$ 200 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 300.4 V.
$I_{DS(MAX)}$ = 262.45 mA.

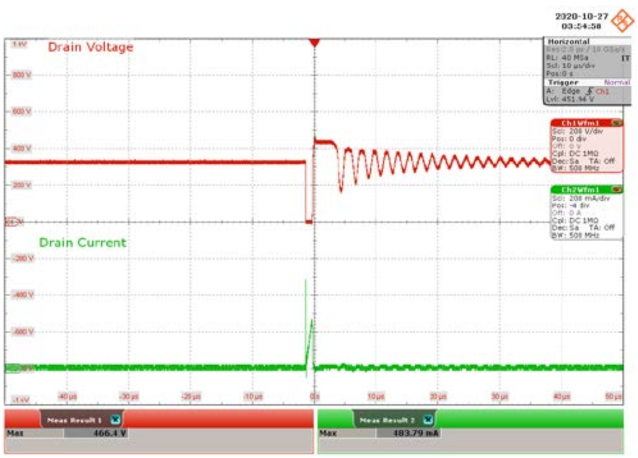

Figure 44 – 230 VAC 50 Hz.
CH1: $V_{DS,}$ 200 V / div., 10 µs / div.
CH2: $I_{DS,}$ 200 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 466.4 V.
$I_{DS(MAX)}$ = 483.79 mA.

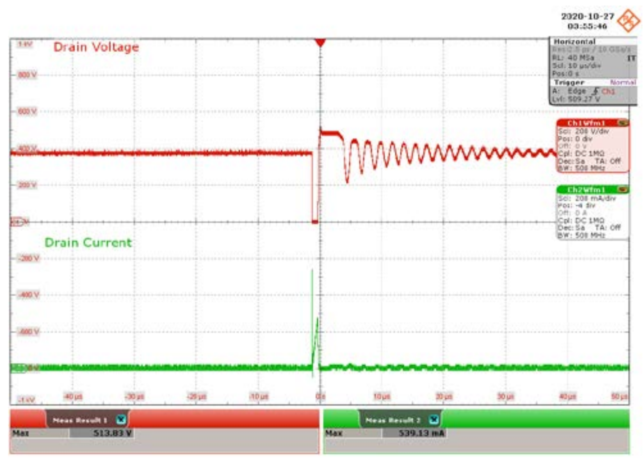

Figure 45 – 265 VAC 50 Hz.
CH1: $V_{DS,}$ 200 V / div., 10 µs / div.
CH2: $I_{DS,}$ 200 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 513.83 V.
$I_{DS(MAX)}$ = 539.13 mA.

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10.3.2 Primary MOSFET Drain-Source Voltage and Current at Start-up Operation

10.3.2.1 100% Load

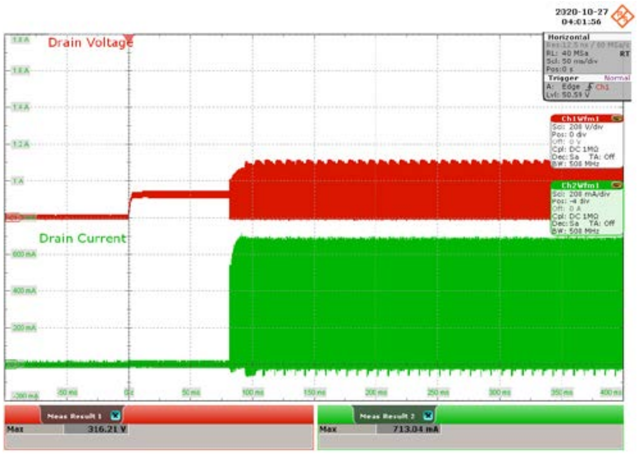

Figure 46 – 90 VAC 60 Hz.
CH1: V_{DS}, 200 V / div., 50 ms / div.
CH2: I_{DS}, 200 mA / div., 50 ms / div.
$V_{DS(MAX)}$ = 316.21 V.
$I_{DS(MAX)}$ = 713.04 mA.

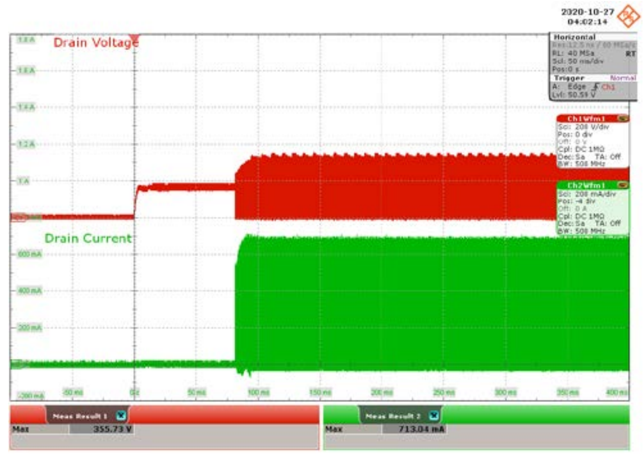

Figure 47 – 115 VAC 60 Hz.
CH1: V_{DS}, 200 V / div., 50 ms / div.
CH2: I_{DS}, 200 mA / div., 50 ms / div.
$V_{DS(MAX)}$ = 355.73 V.
$I_{DS(MAX)}$ = 713.04 mA.

Figure 48 – 230 VAC 50 Hz.
CH1: V_{DS}, 200 V / div., 50 ms / div.
CH2: I_{DS}, 200 mA / div., 50 ms / div.
$V_{DS(MAX)}$ = 513.83 V.
$I_{DS(MAX)}$ = 728.85 mA.

Figure 49 – 265 VAC 50 Hz.
CH1: V_{DS}, 200 V / div., 50 ms / div.
CH2: I_{DS}, 200 mA / div., 50 ms / div.
$V_{DS(MAX)}$ = 569.17 V.
$I_{DS(MAX)}$ = 728.85 mA.

10.3.2.2 0% Load

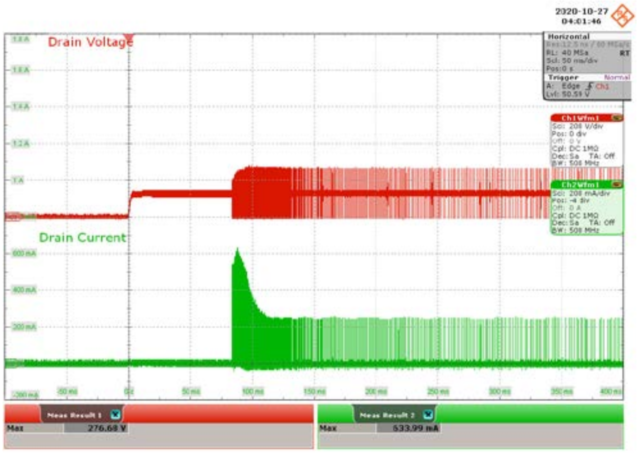

Figure 50 – 90 VAC 60 Hz.
CH1: V_{DS}, 200 V / div., 50 ms / div.
CH2: I_{DS}, 200 mA / div., 50 ms / div.
$V_{DS(MAX)}$ = 276.68 V.
$I_{DS(MAX)}$ = 633.99 mA.

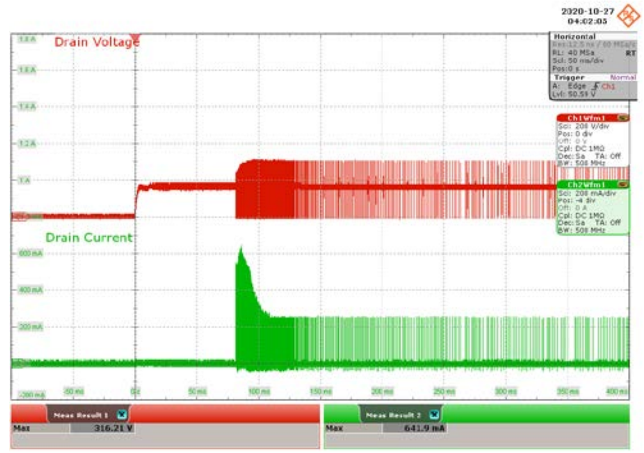

Figure 51 – 115 VAC 60 Hz.
CH1: V_{DS}, 200 V / div., 50 ms / div.
CH2: I_{DS}, 200 mA / div., 50 ms / div.
$V_{DS(MAX)}$ = 316.21 V.
$I_{DS(MAX)}$ = 641.9 mA.

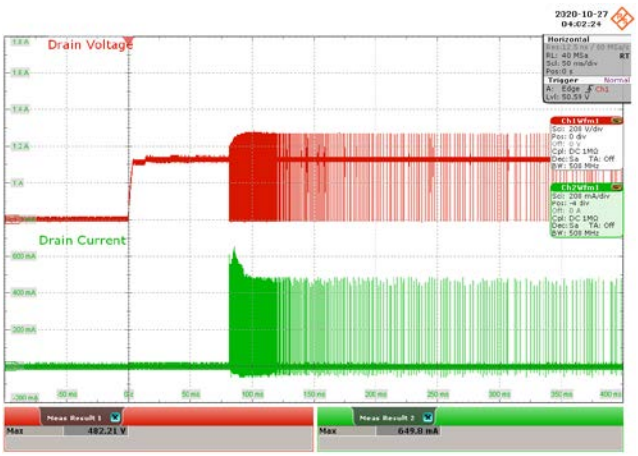

Figure 52 – 230 VAC 50 Hz.
CH1: V_{DS}, 200 V / div., 50 ms / div.
CH2: I_{DS}, 200 mA / div., 50 ms / div.
$V_{DS(MAX)}$ = 482.21 V.
$I_{DS(MAX)}$ = 649.8 mA.

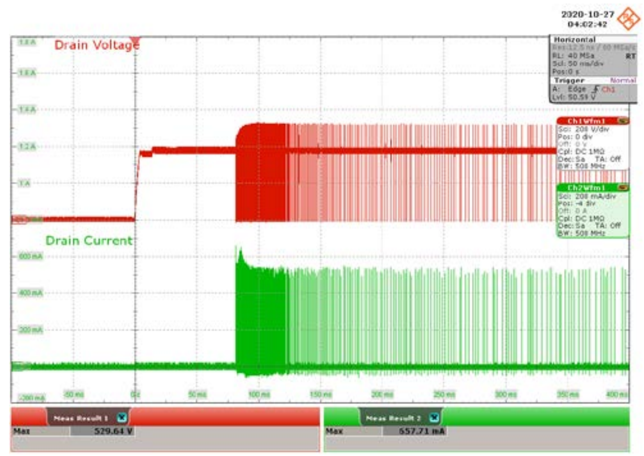

Figure 53 – 265 VAC 50 Hz.
CH1: V_{DS}, 200 V / div., 50 ms / div.
CH2: I_{DS}, 200 mA / div., 50 ms / div.
$V_{DS(MAX)}$ = 529.64 V.
$I_{DS(MAX)}$ = 657.71 mA.

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10.3.3 SR FET Voltage and Current at Normal Operation

10.3.3.1 100% Load

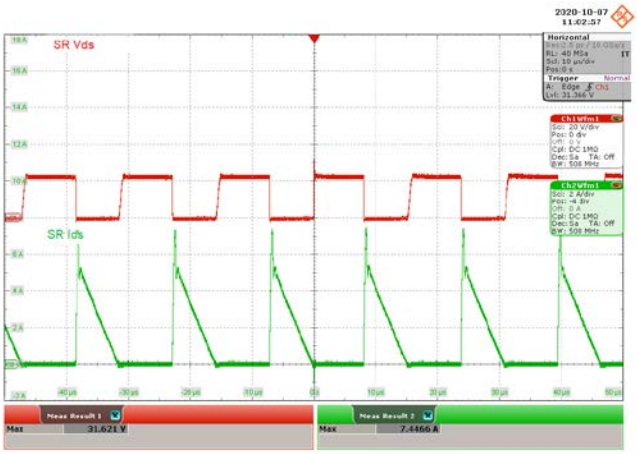

Figure 54 – 90 VAC 60 Hz.
CH1: V_D, 20 V / div., 10 µs / div.
CH2: I_D, 2 A / div., 10 µs / div.
PIV = 31.621 V.
$I_{D(MAX)}$ = 7.4466 A.

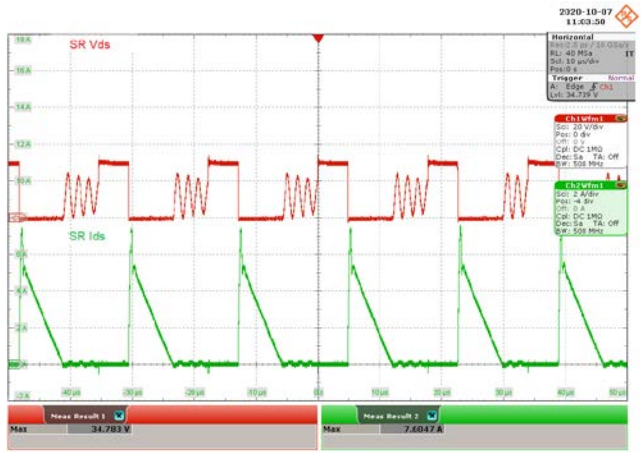

Figure 55 – 115 VAC 60 Hz.
CH1: V_D, 20 V / div., 10 µs / div.
CH2: I_D, 2 A / div., 10 µs / div.
PIV = 34.783 V.
$I_{D(MAX)}$ = 7.6047 A.

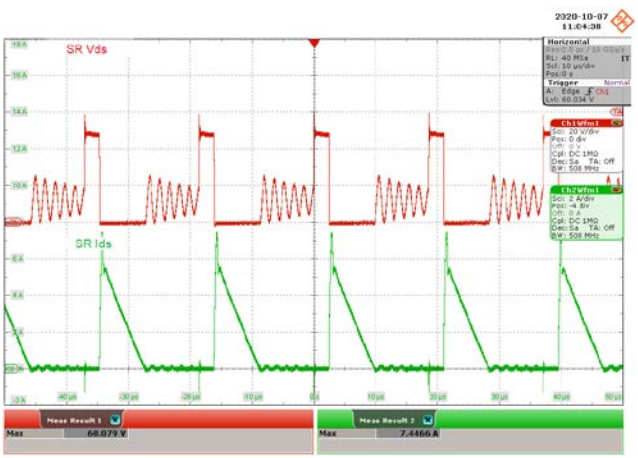

Figure 56 – 230 VAC 50 Hz.
CH1: V_D, 20 V / div., 10 µs / div.
CH2: I_D, 2 A / div., 10 µs / div.
PIV = 60.079 V.
$I_{D(MAX)}$ = 7.4466 A.

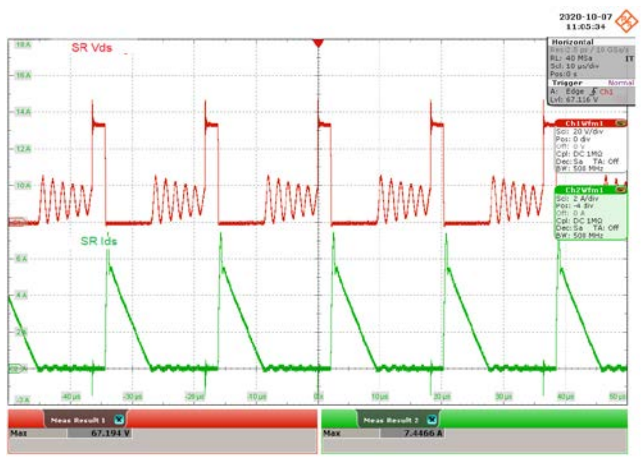

Figure 57 – 265 VAC 50 Hz.
CH1: V_D, 20 V / div., 10 µs / div.
CH2: I_D, 2 A / div., 10 µs / div.
PIV = 67.194 V.
$I_{D(MAX)}$ = 7.4466 A.

10.3.3.2 0% Load

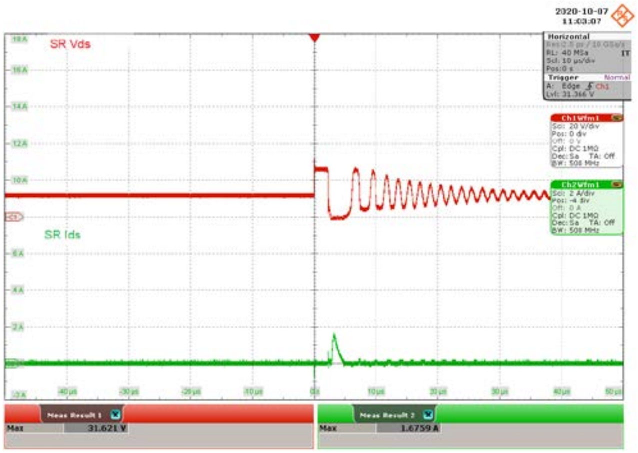

Figure 58 – 90 VAC 60 Hz.
CH1: $V_{D,}$ 20 V / div., 10 µs / div.
CH2: $I_{D,}$ 2 A / div., 10 µs / div.
PIV = 31.621 V.
$I_{D(MAX)}$ = 1.6759 A.

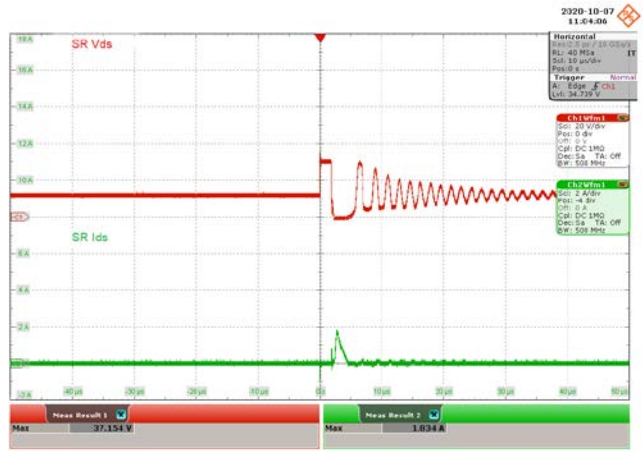

Figure 59 – 115 VAC 60 Hz.
CH1: $V_{D,}$ 20 V / div., 10 µs / div.
CH2: $I_{D,}$ 2 A / div., 10 µs / div.
PIV = 37.154 V.
$I_{D(MAX)}$ = 1.834 A.

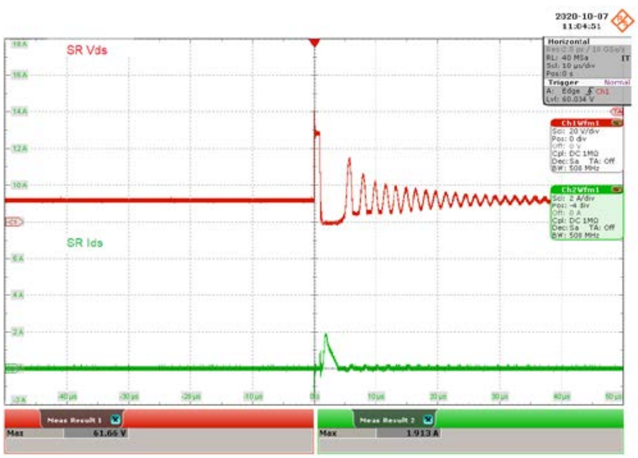

Figure 60 – 230 VAC 50 Hz.
CH1: $V_{D,}$ 20 V / div., 10 µs / div.
CH2: $I_{D,}$ 2 A / div., 10 µs / div.
PIV = 61.66 V.
$I_{D(MAX)}$ = 1.913 A.

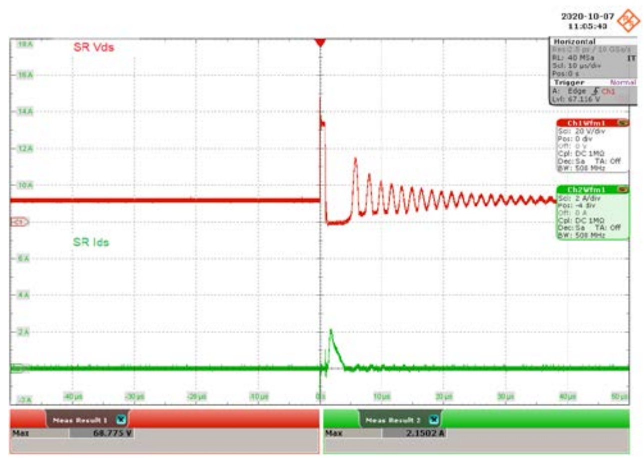

Figure 61 – 265 VAC 50 Hz.
CH1: $V_{D,}$ 20 V / div., 10 µs / div.
CH2: $I_{D,}$ 2 A / div., 10 µs / div.
PIV = 68.775 V.
$I_{D(MAX)}$ = 2.1502 A.

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10.3.4 SR FET Voltage and Current at Start-up Operation

10.3.4.1 100% Load

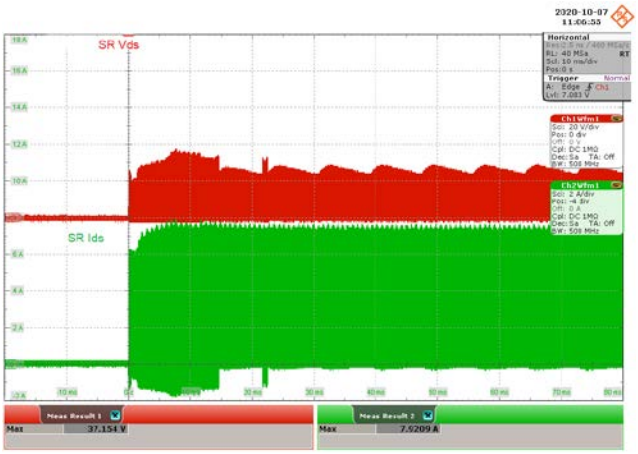

Figure 62 – 90 VAC 60 Hz.
CH1: $V_{DS,}$ 200 V / div., 10 µs / div.
CH2: $I_{DS,}$ 200 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 37.154 V.
$I_{DS(MAX)}$ = 7.9209 A.

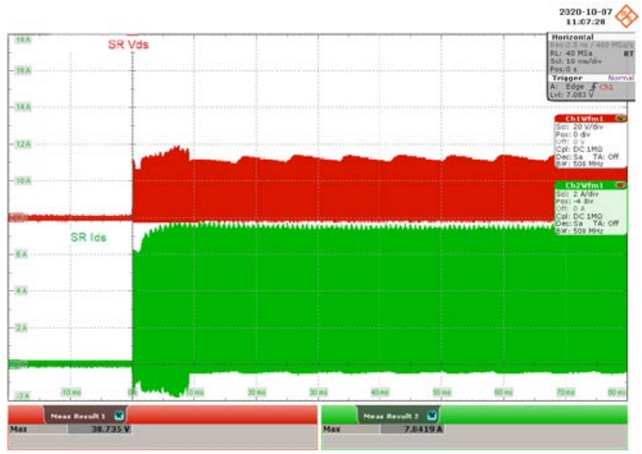

Figure 63 – 115 VAC 60 Hz.
CH1: $V_{DS,}$ 200 V / div., 10 µs / div.
CH2: $I_{DS,}$ 200 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 38.735 V.
$I_{DS(MAX)}$ = 7.8419 A.

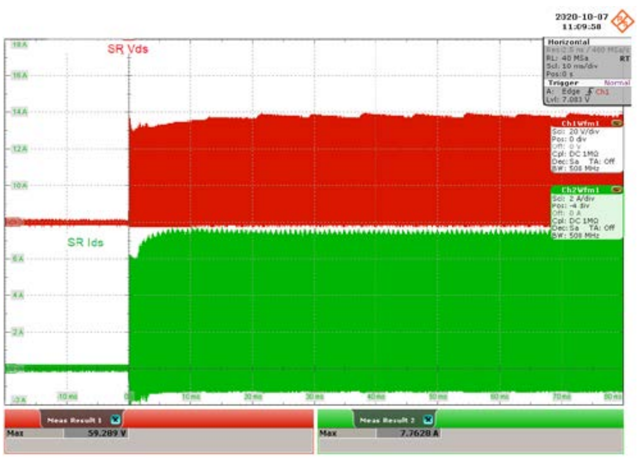

Figure 64 – 230 VAC 50 Hz.
CH1: $V_{DS,}$ 200 V / div., 10 µs / div.
CH2: $I_{DS,}$ 200 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 59.289 V.
$I_{DS(MAX)}$ = 7.7628 A.

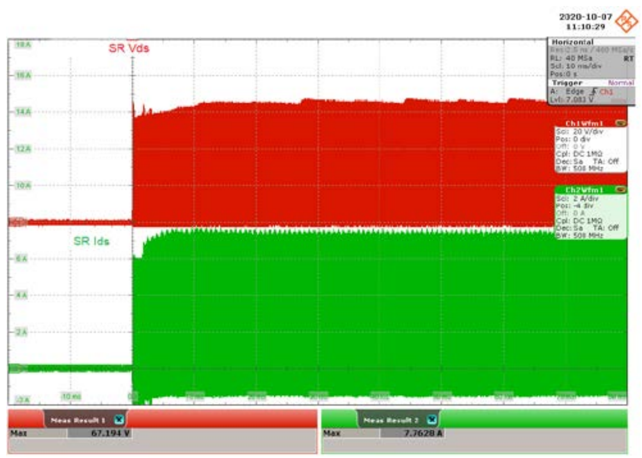

Figure 65 – 265 VAC 50 Hz.
CH1: $V_{DS,}$ 200 V / div., 10 µs / div.
CH2: $I_{DS,}$ 200 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 67.194 V.
$I_{DS(MAX)}$ = 7.7628 A.

10.3.4.2 0% Load

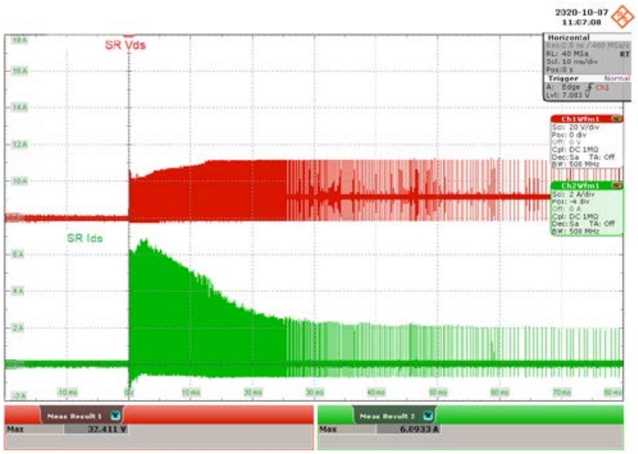

Figure 66 – 90 VAC 60 Hz.
CH1: $V_{DS,}$ 200 V / div., 10 µs / div.
CH2: $I_{DS,}$ 200 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 32.411 V.
$I_{DS(MAX)}$ = 6.8933 A.

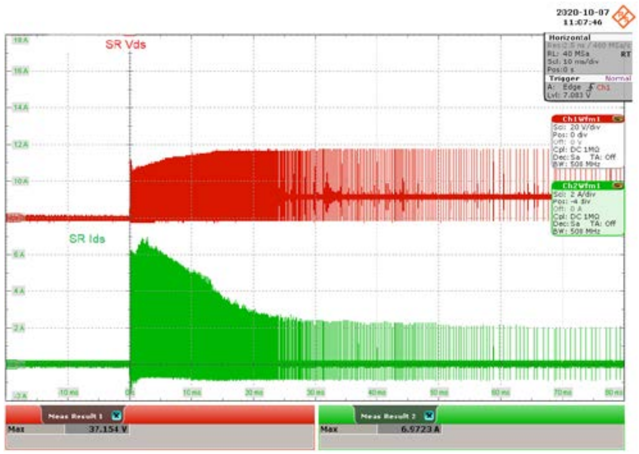

Figure 67 – 115 VAC 60 Hz.
CH1: $V_{DS,}$ 200 V / div., 10 µs / div.
CH2: $I_{DS,}$ 200 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 37.154 V.
$I_{DS(MAX)}$ = 6.9723 A.

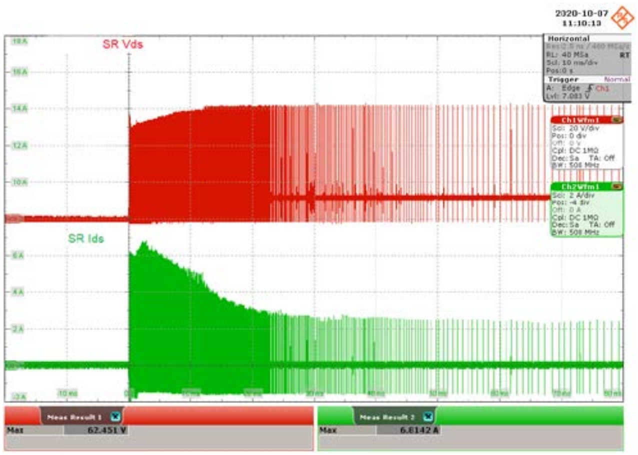

Figure 68 – 230 VAC 50 Hz.
CH1: $V_{DS,}$ 200 V / div., 10 µs / div.
CH2: $I_{DS,}$ 200 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 62.451 V.
$I_{DS(MAX)}$ = 6.8142 A.

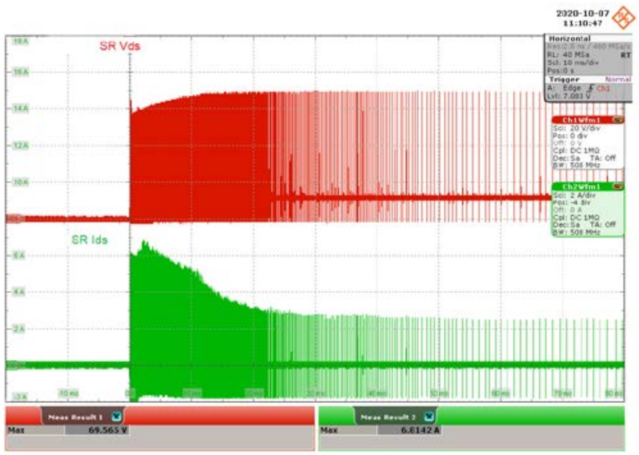

Figure 69 – 265 VAC 50 Hz.
CH1: $V_{DS,}$ 200 V / div., 10 µs / div.
CH2: $I_{DS,}$ 200 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 69.565 V.
$I_{DS(MAX)}$ = 6.8142 A.

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10.4 *Brown-In and Brown-Out*

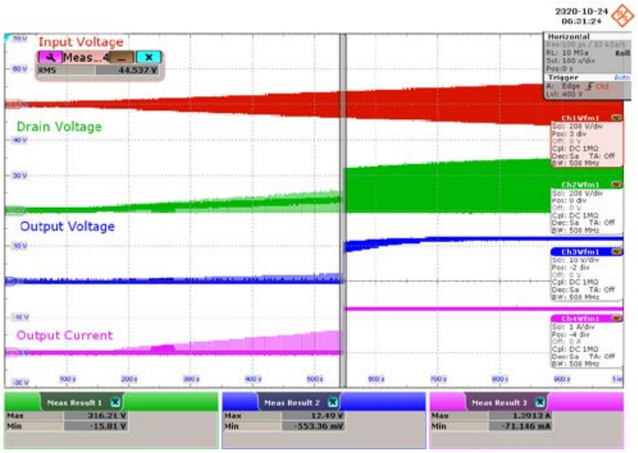

Figure 70 – Brown-In, Full Load.
CH1: $V_{IN,}$ 200 V / div., 100 s / div.
CH2: $V_{DS,}$ 200 V / div., 100 s / div.
CH3: $V_{OUT,}$ 10 V / div., 100 s / div.
CH4: I_{OUT}, 1 A / div., 100 s / div.
$V_{IN(UV)}$ = 44.537 V_{RMS}.

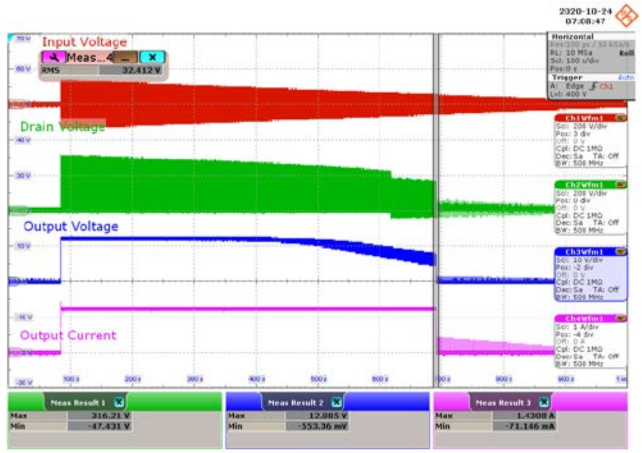

Figure 71 – Brown-Out, Full Load.
CH1: $V_{IN,}$ 200 V / div., 100 s / div.
CH2: $V_{DS,}$ 200 V / div., 100 s / div.
CH3: $V_{OUT,}$ 10 V / div., 100 s / div.
CH4: I_{OUT}, 1 A / div., 100 s / div.
$V_{IN(UV)}$ = 32.412 V_{RMS}.

10.5 *Fault Conditions*

10.5.1 Output Overvoltage

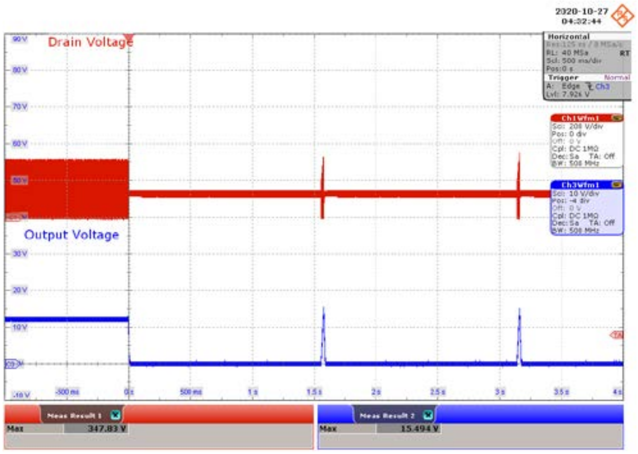

Figure 72 – 90 VAC 60 Hz, Full Load.
CH1: $V_{DS,}$ 200 V / div., 500 ms / div.
CH3: $V_{OUT,}$ 10 V / div., 500 ms / div.
$V_{DS(MAX)}$ = 347.83 V.
$V_{O(MAX)}$ = 15.494 V.

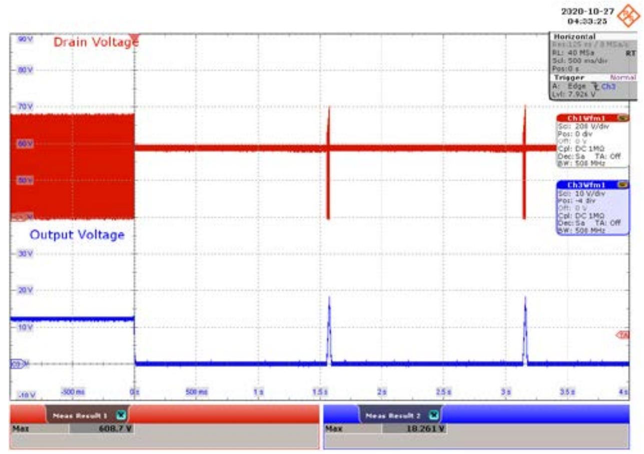

Figure 73 – 265 VAC 60 Hz, Full Load.
CH1: $V_{DS,}$ 200 V / div., 500 ms / div.
CH3: $V_{OUT,}$ 10 V / div., 500 ms / div.
$V_{DS(MAX)}$ = 608.7 V.
$V_{O(MAX)}$ = 18.261 V.

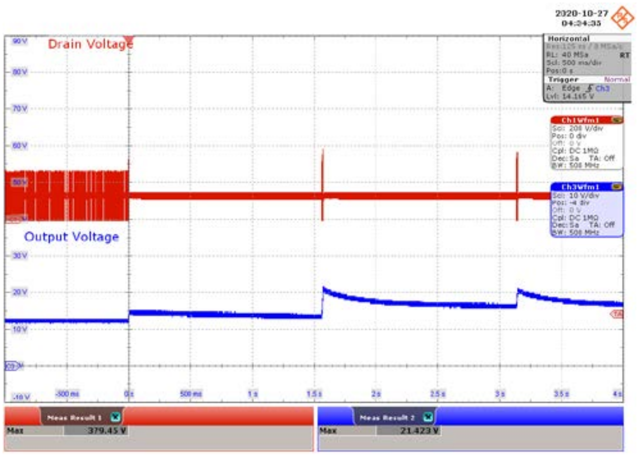

Figure 74 – 90 VAC 60 Hz, No-load.
CH1: $V_{DS,}$ 200 V / div., 500 ms / div.
CH3: $V_{OUT,}$ 10 V / div., 500 ms / div.
$V_{DS(MAX)}$ = 379.45 V.
$V_{O(MAX)}$ = 21.423 V.

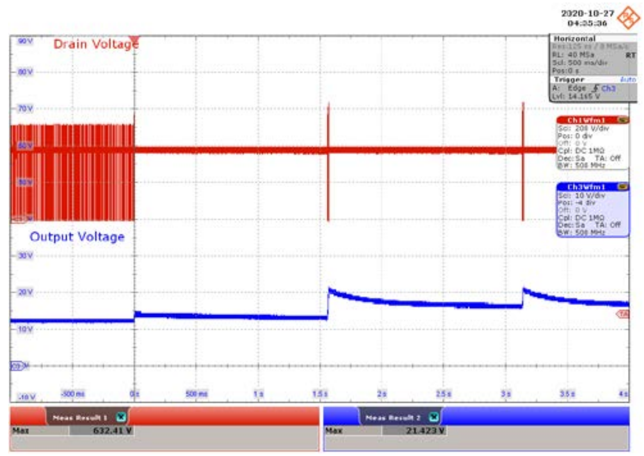

Figure 75 – 265 VAC 60 Hz, No-load.
CH1: $V_{DS,}$ 200 V / div., 500 ms / div.
CH3: $V_{OUT,}$ 10 V / div., 500 ms / div.
$V_{DS(MAX)}$ = 632.41 V.
$V_{O(MAX)}$ = 21.423 V.

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10.5.2 Output Short Circuit

Test Condition: Short circuit applied at startup

Figure 76 – 90 VAC 60 Hz.
CH1: $V_{DS,}$ 200 V / div., 1 s / div.
CH2: $I_{DS,}$ 200 mA / div., 1 s / div.
$V_{DS(MAX)}$ = 205.53 V.
$I_{DS(MAX)}$ = 539.13 mA.

Figure 77 – 265 VAC 60 Hz.
CH1: $V_{DS,}$ 200 V / div., 1 s / div.
CH2: $I_{DS,}$ 200 mA / div., 1 s / div.
$V_{DS(MAX)}$ = 442.69 V.
$I_{DS(MAX)}$ = 785.14 mA.

10.6 *Output Voltage Ripple*

10.6.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF / 50 V ceramic type and one (1) 47 μF / 50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

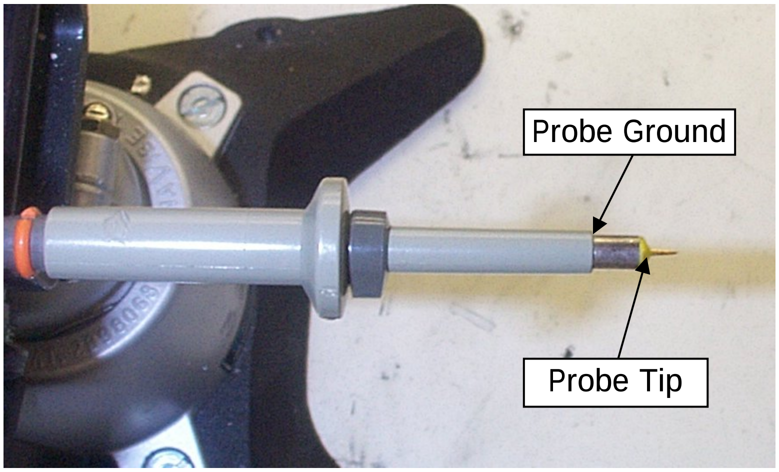

Figure 78 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed.)

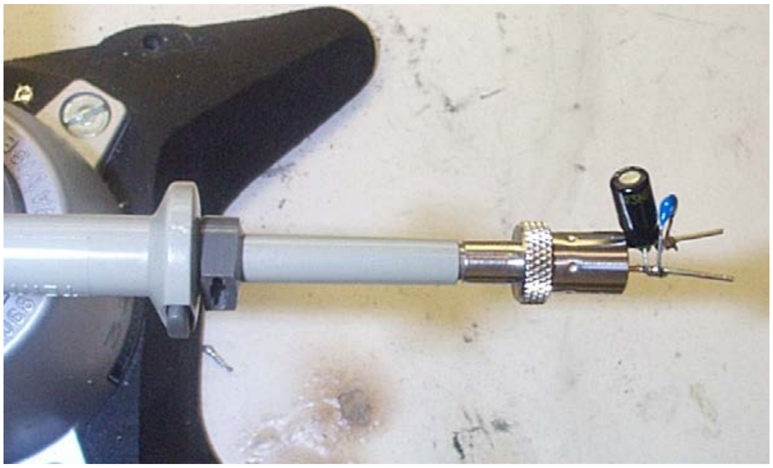

Figure 79 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added.)

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10.6.2 Measurement Results

Note: All ripple measurements were taken at the PCB terminals.

10.6.2.1 100% Load Condition

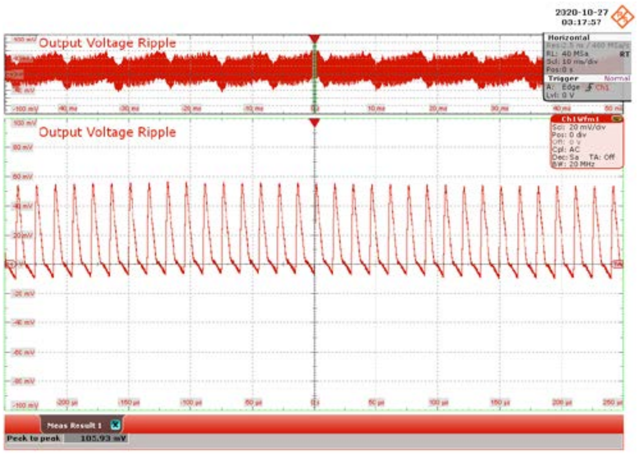

Figure 80 – 90 VAC 60 Hz.
CH1: $V_{OUT,}$ 20 mV / div., 10 ms / div.
Zoom: 50 µs / div.
Output Ripple = 105.93 mV.

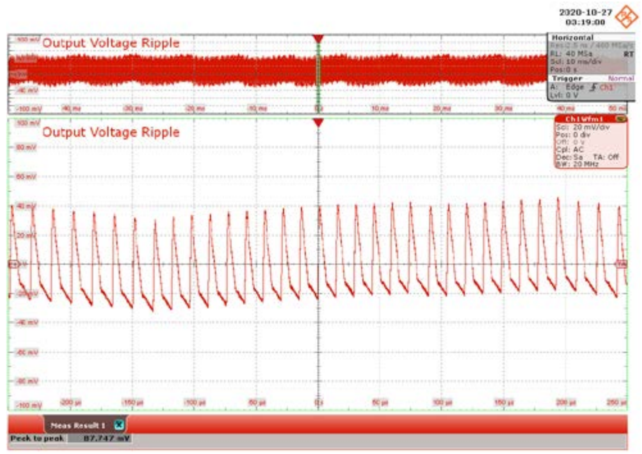

Figure 81 – 115 VAC 60 Hz.
CH1: $V_{OUT,}$ 20 mV / div., 10 ms / div.
Zoom: 50 µs / div.
Output Ripple = 87.747 mV.

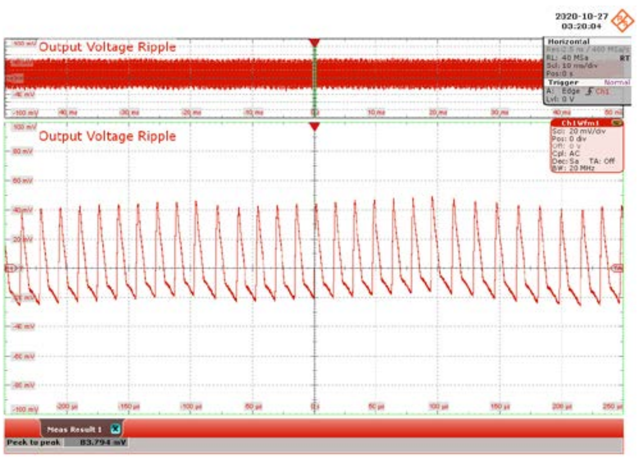

Figure 82 – 230 VAC 50 Hz.
CH1: $V_{OUT,}$ 20 mV / div., 10 ms / div.
Zoom: 50 µs / div.
Output Ripple = 83.794 mV.

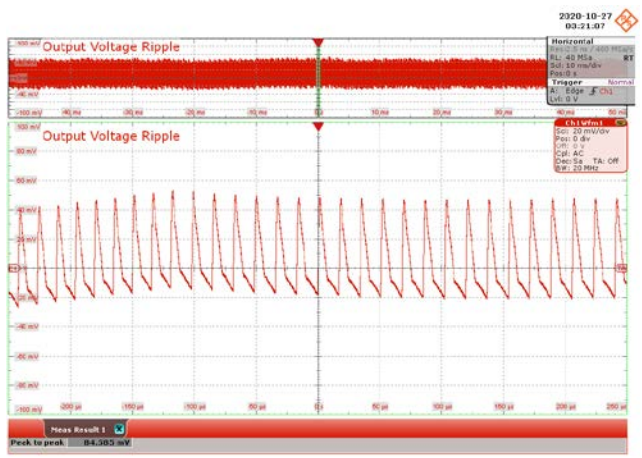

Figure 83 – 265 VAC 50 Hz.
CH1: $V_{OUT,}$ 20 mV / div., 10 ms / div.
Zoom: 50 µs / div.
Output Ripple = 84.585 mV.

10.6.2.2 75% Load Condition

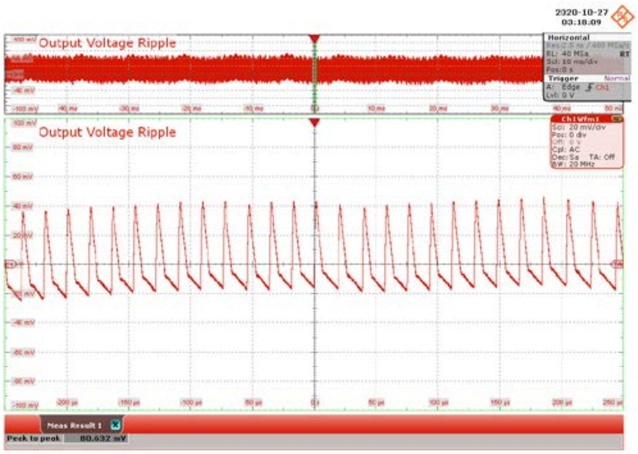

Figure 84 – 90 VAC 60 Hz.
CH1: $V_{OUT,}$ 20 mV / div., 10 ms / div.
Zoom: 50 µs / div.
Output Ripple = 80.632 mV.

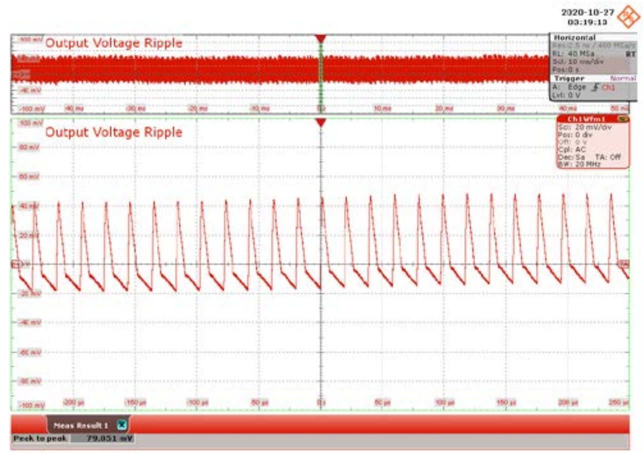

Figure 85 – 115 VAC 60 Hz.
CH1: $V_{OUT,}$ 20 mV / div., 10 ms / div.
Zoom: 50 µs / div.
Output Ripple = 79.051 mV.

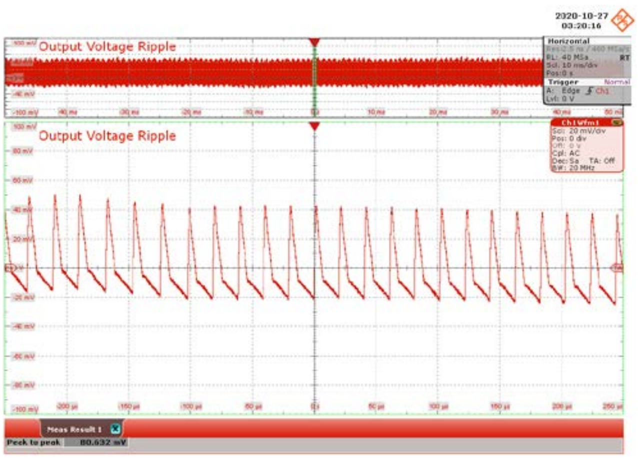

Figure 86 – 230 VAC 50 Hz.
CH1: $V_{OUT,}$ 20 mV / div., 10 ms / div.
Zoom: 50 µs / div.
Output Ripple = 80.632 mV.

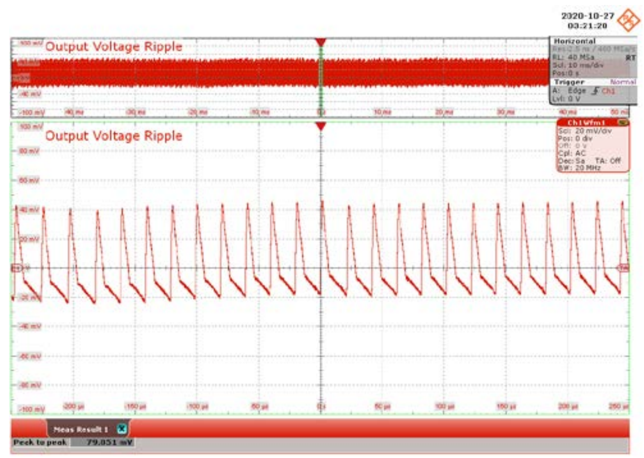

Figure 87 – 265 VAC 50 Hz.
CH1: $V_{OUT,}$ 20 mV / div., 10 ms / div.
Zoom: 50 µs / div.
Output Ripple = 79.051 mV.

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10.6.2.3 50% Load Condition

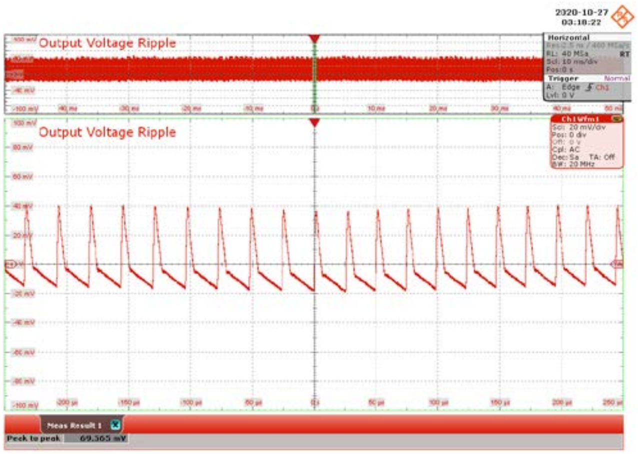

Figure 88 – 90 VAC 60 Hz.
CH1: V_{OUT}, 20 mV / div., 10 ms / div.
Zoom: 50 µs / div.
Output Ripple = 69.565 mV.

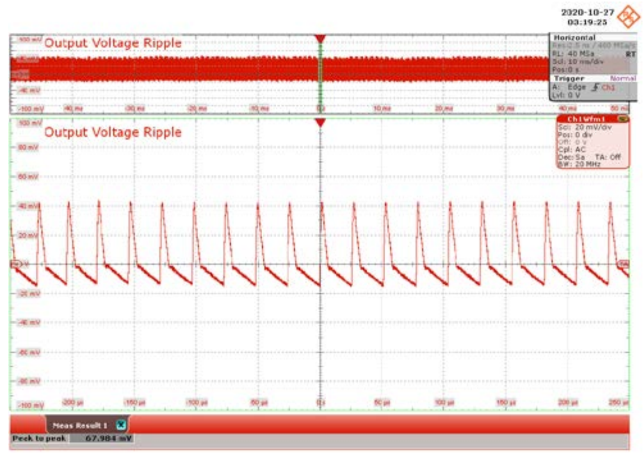

Figure 89 – 115 VAC 60 Hz.
CH1: V_{OUT}, 20 mV / div., 10 ms / div.
Zoom: 50 µs / div.
Output Ripple = 67.984 mV.

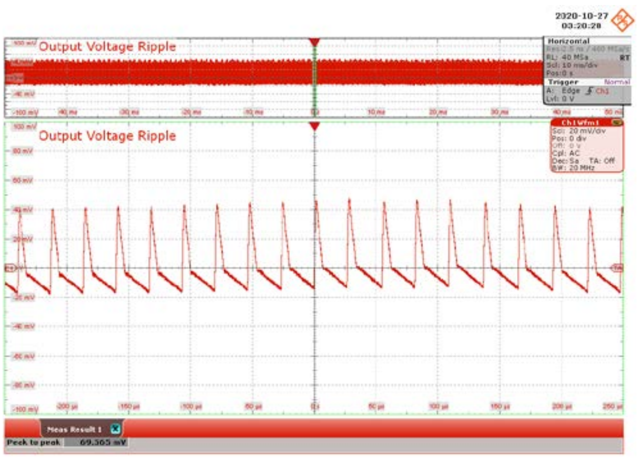

Figure 90 – 230 VAC 50 Hz.
CH1: V_{OUT}, 20 mV / div., 10 ms / div.
Zoom: 50 µs / div.
Output Ripple = 69.565 mV.

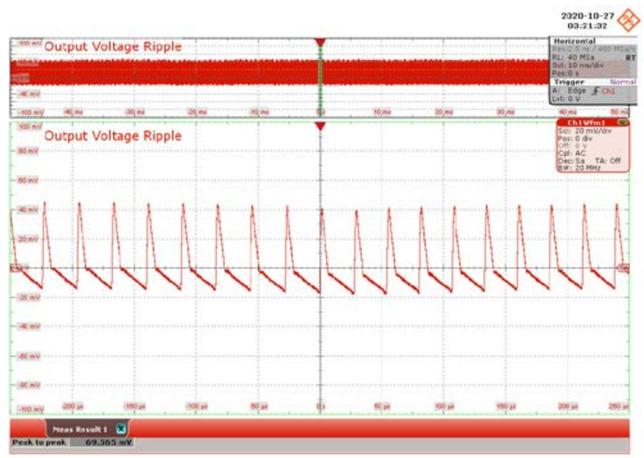

Figure 91 – 265 VAC 50 Hz.
CH1: V_{OUT}, 20 mV / div., 10 ms / div.
Zoom: 50 µs / div.
Output Ripple = 69.565 mV.

10.6.2.4 25% Load Condition

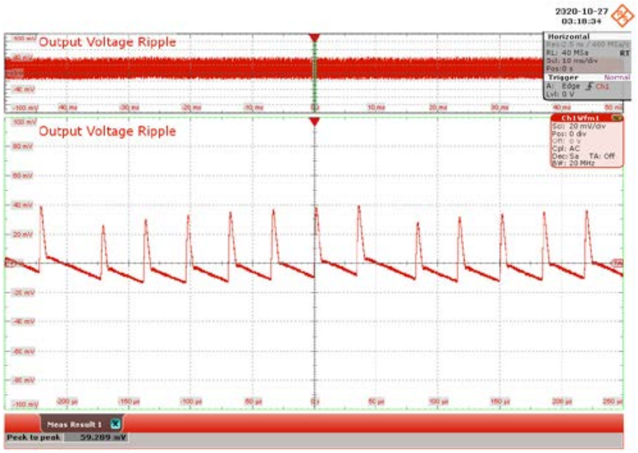

Figure 92 – 90 VAC 60 Hz.
CH1: $V_{OUT,}$ 20 mV / div., 10 ms / div.
Zoom: 50 µs / div.
Output Ripple = 59.289 mV.

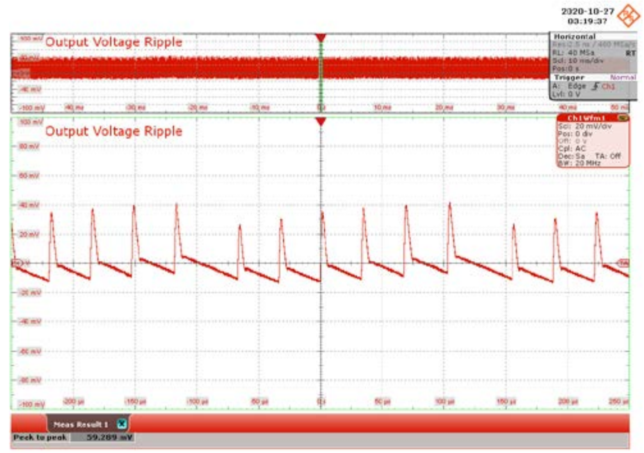

Figure 93 – 115 VAC 60 Hz.
CH1: $V_{OUT,}$ 20 mV / div., 10 ms / div.
Zoom: 50 µs / div.
Output Ripple = 59.289 mV.

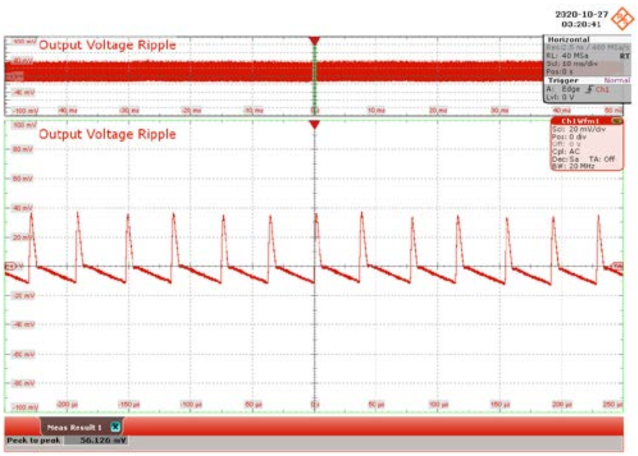

Figure 94 – 230 VAC 50 Hz.
CH1: $V_{OUT,}$ 20 mV / div., 10 ms / div.
Zoom: 50 µs / div.
Output Ripple = 56.126 mV.

Figure 95 – 265 VAC 50 Hz.
CH1: $V_{OUT,}$ 20 mV / div., 10 ms / div.
Zoom: 50 µs / div.
Output Ripple = 56.126 mV.

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10.6.3 Output Ripple Voltage Graph from 0% - 100%

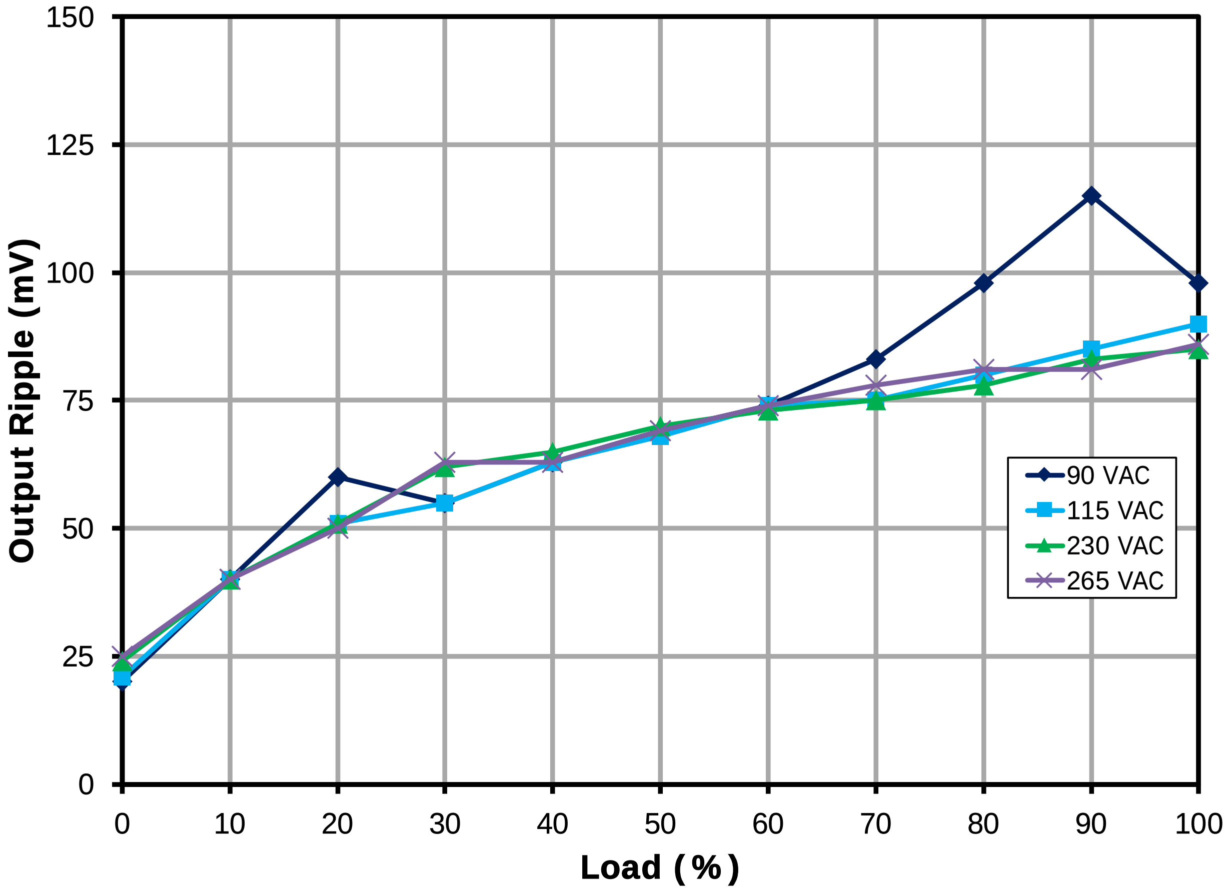

Figure 96 – Measured at the PCB Terminal, at Room Temperature.

11 Thermal Performance

11.1 *Test Set-Up*

Thermal evaluation was performed under two conditions: (1) room temperature with the circuit board enclosed inside an acrylic box and (2), 50 ºC ambient inside a thermal chamber. In both conditions, the circuit is soaked for one hour under full load conditions.

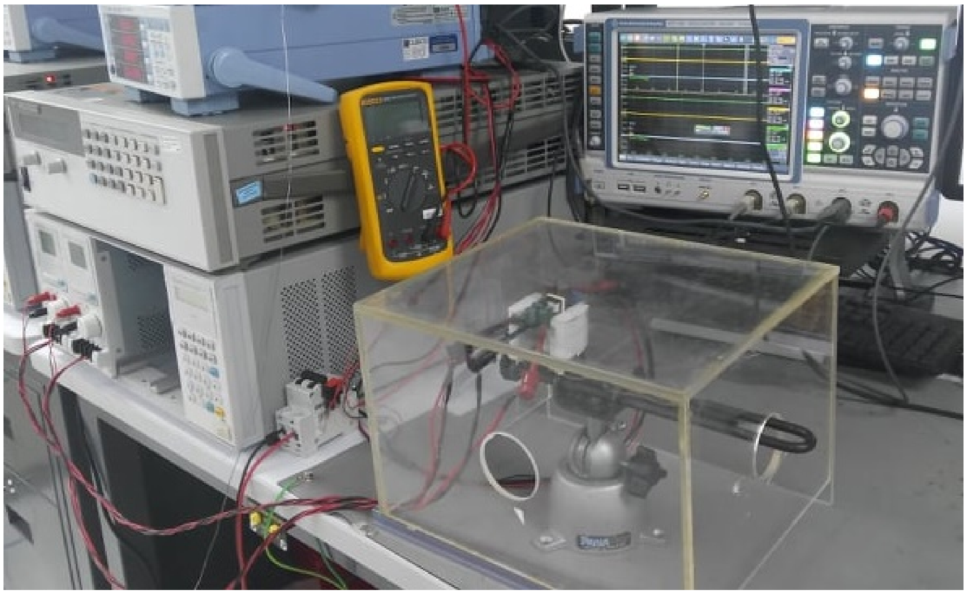

Figure 97 – Thermal Performance Set-up Using an Acrylic Box.

Figure 98 – Thermal Performance Set-up Using Thermal Chamber.

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11.2 *Thermal Performance at Room Temperature*

11.2.1 90 VAC at Room Temperature

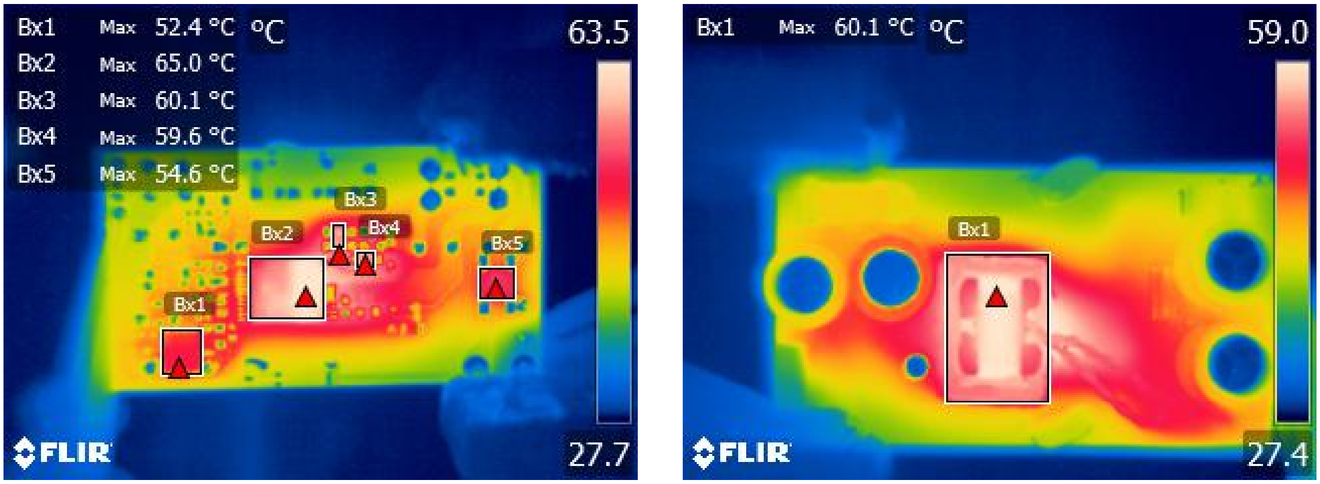

Figure 99 – Thermal Performance at 90 VAC.

Component	Temperature (°C)
Ambient	28.0
SR FET	52.4
INN3164	65.0
Snubber R4	60.1
Snubber D1	59.6
Bridge Rectifier	54.6
Transformer	60.1

11.2.2 265 VAC at Room Temperature

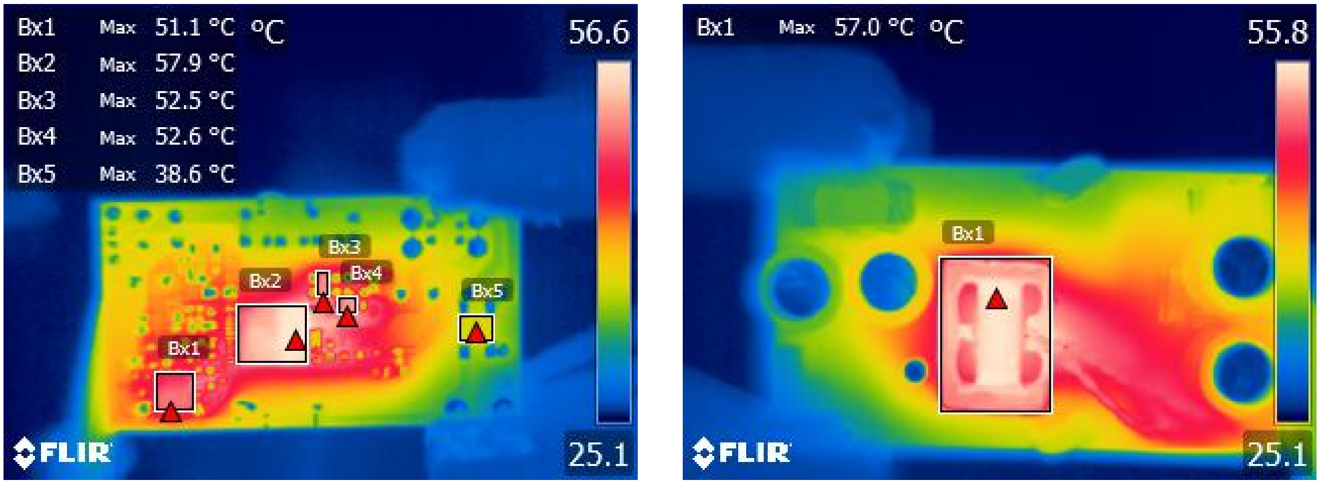

Figure 100 – Thermal Performance at 265 VAC.

Component	**Temperature (°C)**
Ambient	26.5
SR FET	51.1
INN3164	57.9
Snubber R4	52.5
Snubber D1	52.6
Bridge Rectifier	38.6
Transformer	57.0

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11.3 *Thermal Performance at 50 °C*

11.3.1 90 VAC at 50 °C

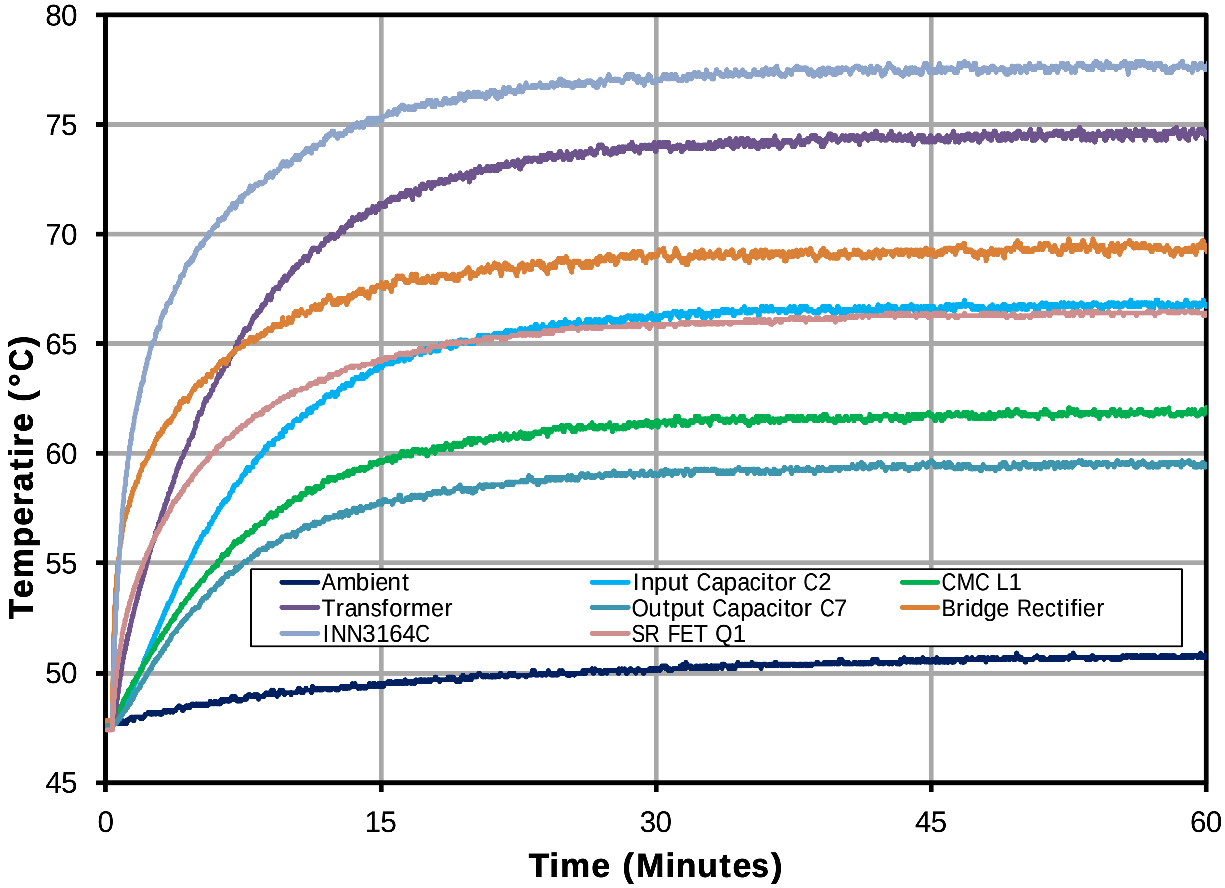

Figure 101 – Thermal Performance at 90 VAC, Full Load.

Component	Temperature (°C)
Ambient	50.8
Input Capacitor C2	66.6
CMC L1	61.9
Transformer	74.6
Output Capacitor C7	59.6
Bridge Rectifier	69.2
INN3164	77.5
SR FET Q1	66.5

11.3.2 265 VAC at 50 °C

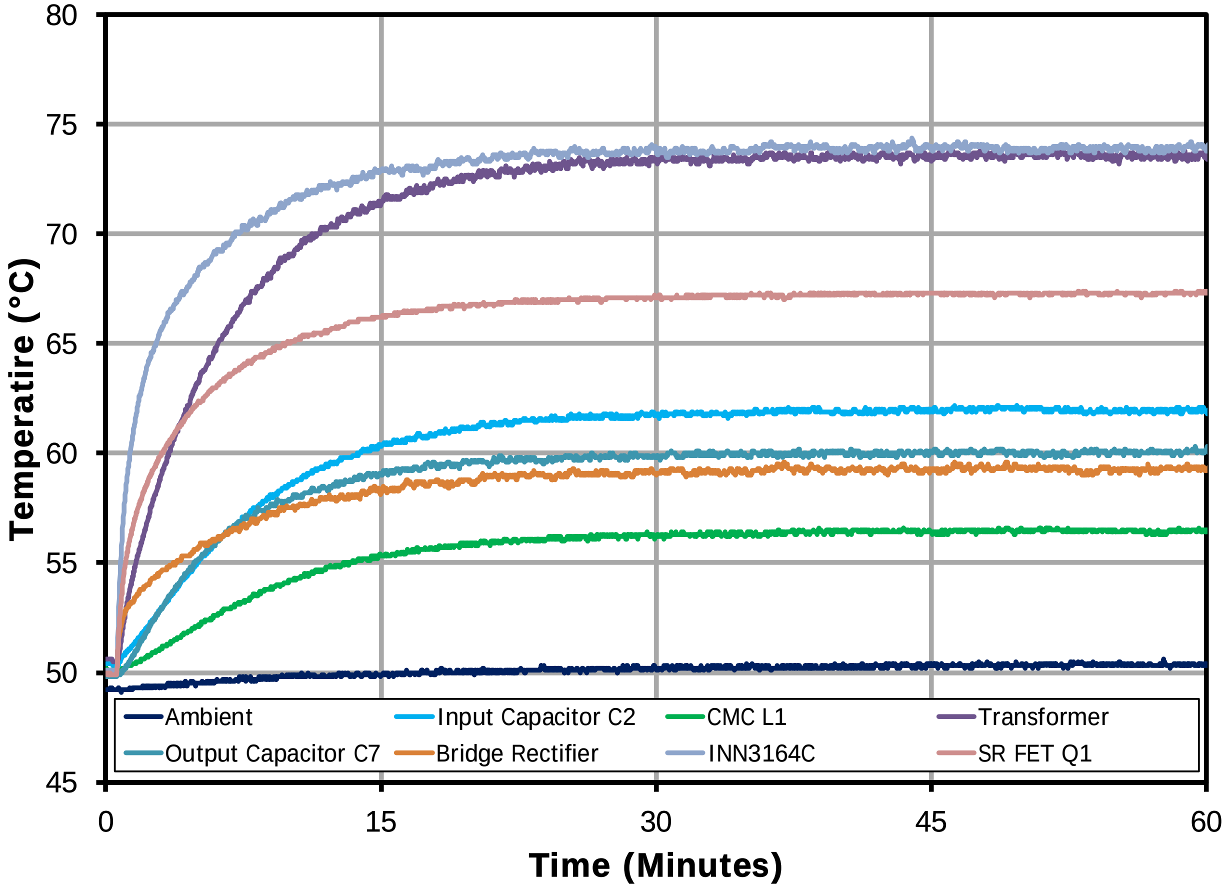

Figure 102 – Thermal Performance at 265 VAC, Full Load.

Component	Temperature (°C)
Ambient	50.4
Input Capacitor C2	61.9
CMC L1	56.5
Transformer	73.7
Output Capacitor C7	60.1
Bridge Rectifier	59.2
INN3164	74
SR FET Q1	67.4

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11.4 *Over Temperature Protection*

11.4.1 OTP at 90 VAC

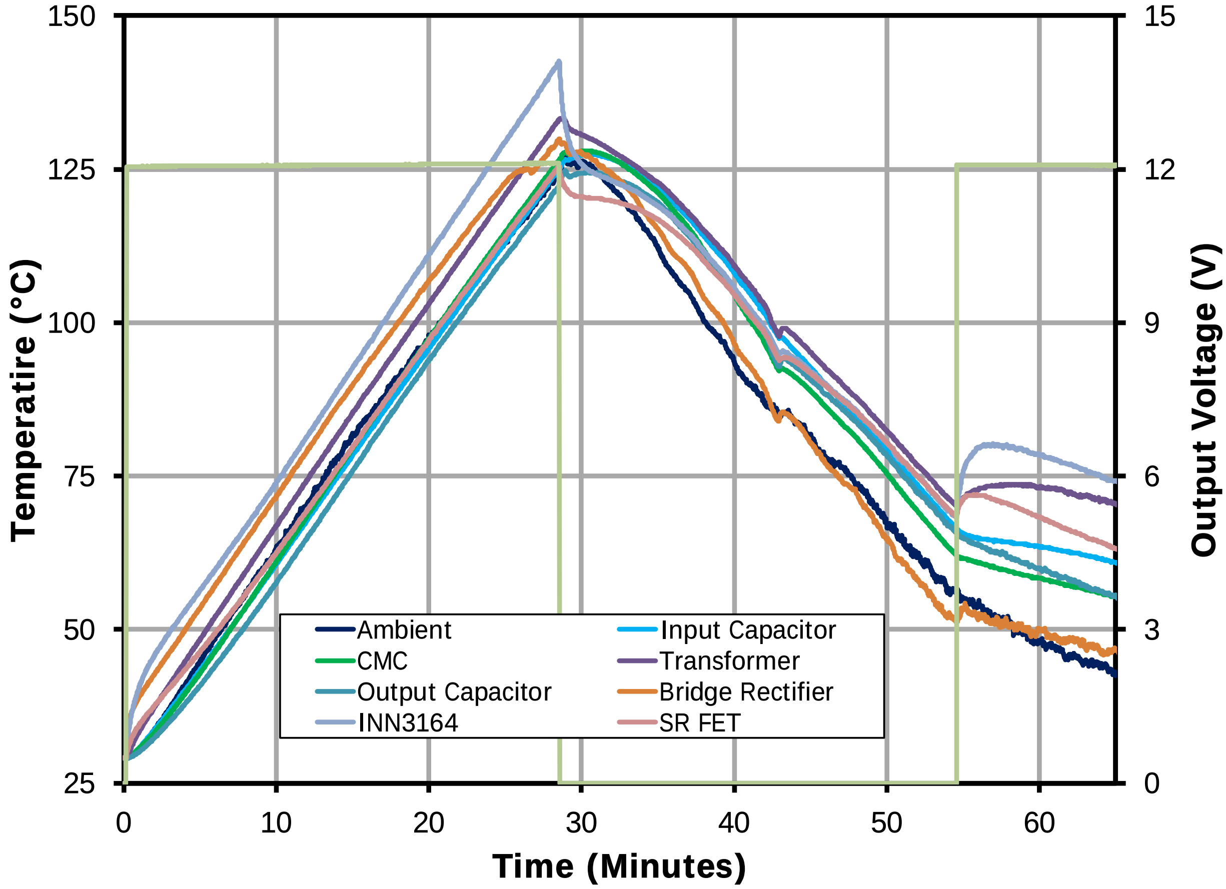

Figure 103 – Over Temperature Protection at 90 VAC.

Component	At OTP Trigger Temperature (°C)	At Recovery Temperature (°C)
Ambient	124.6	56.2
Input Capacitor C2	125.1	66.4
CMC L1	126.5	62.1
Transformer	133.1	70.1
Output Capacitor C7	122.3	65.6
Bridge Rectifier	129.9	51.3
INN3164	142.6	68.2
SR FET Q1	125.5	68.4

11.4.2 OTP at 265 VAC

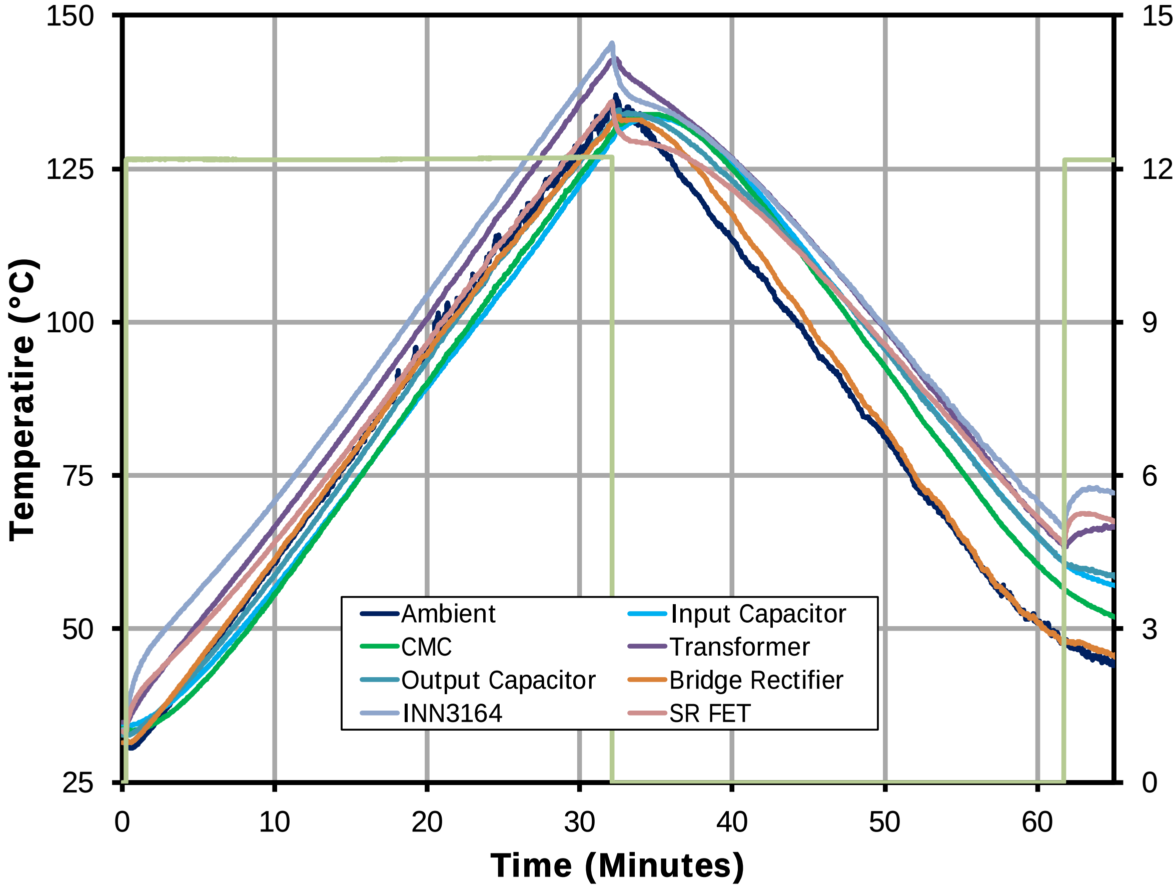

Figure 104 – Over Temperature Protection at 265 VAC.

Component	At OTP Trigger Temperature (°C)	At Recovery Temperature (°C)
Ambient	134.6	47.3
Input Capacitor C2	129.7	60.7
CMC L1	130.7	56.4
Transformer	142.7	63.2
Output Capacitor C7	132.7	60.8
Bridge Rectifier	132.4	47.7
INN3164	145.5	66.5
SR FET Q1	136	63.9

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12 Conducted EMI

Conducted emissions tests were performed at 115 VAC and 230 VAC at full load (12 V, 1.25 A). Measurements were taken with an Artificial Hand connected and a floating DC output load resistor.

12.1 *Test Set-up Equipment*

12.1.1 Equipment and Load Used

1. Rohde and Schwarz ENV216 two line V-network.
2. Rohde and Schwarz ESRP EMI test receiver.
3. Yokogawa WT310E Digital Power Meter
4. Chroma measurement test fixture.
5. Input voltage set at 115 VAC and 230 VAC.

12.2 *Test Set-up*

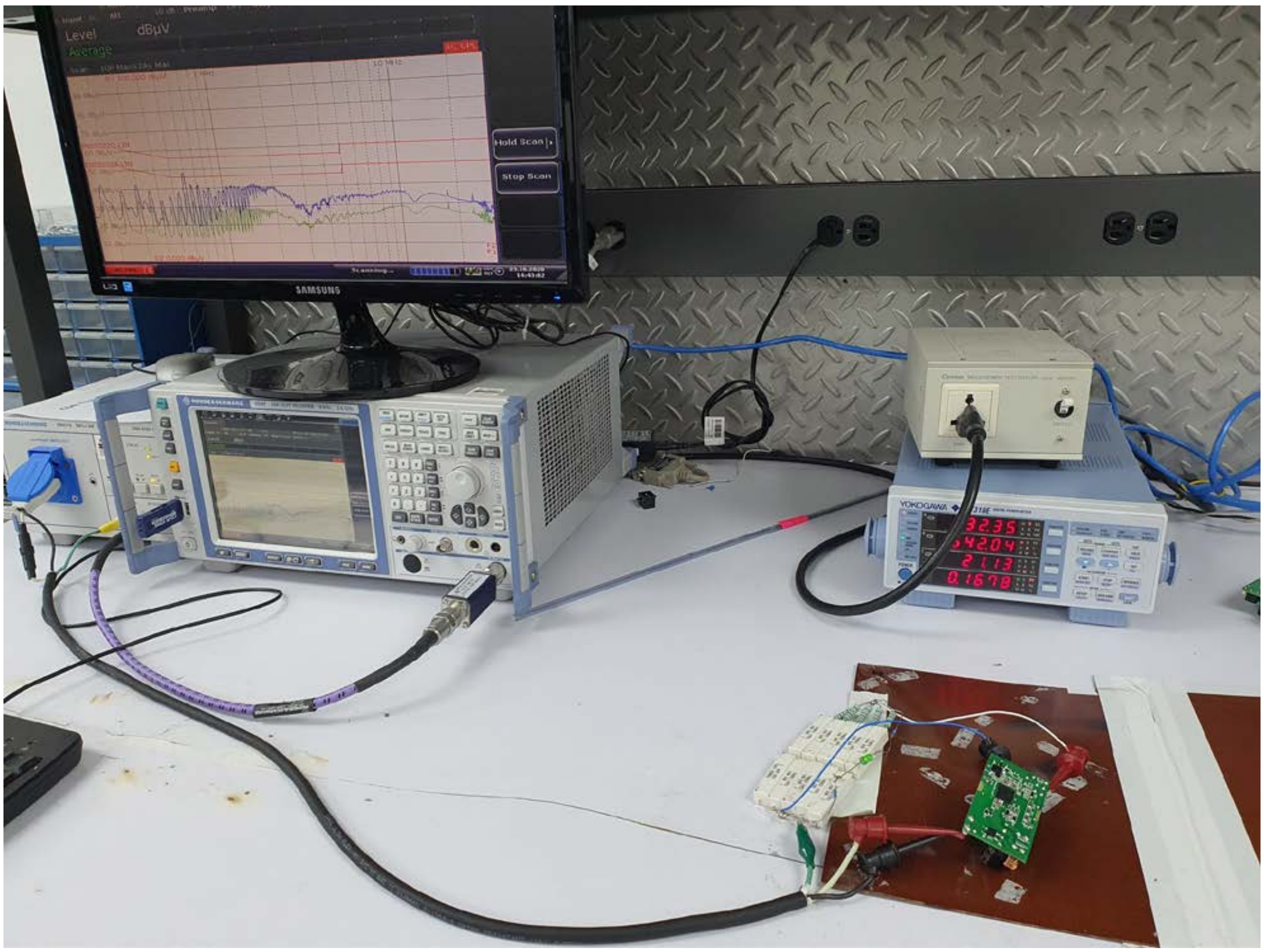

Figure 105 – EMI Test Set-up.

12.3 *Test Results*

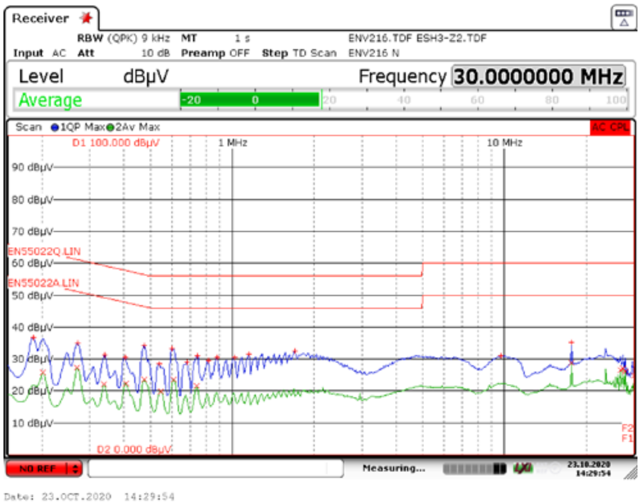

Figure 106 – 115 VAC 60 Hz, Artificial Hand.

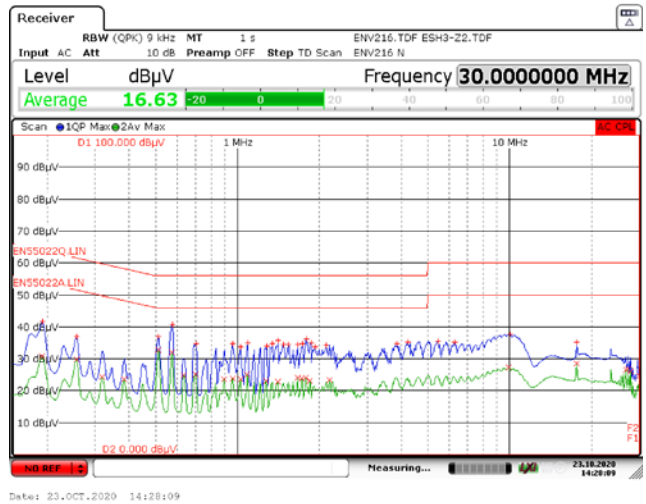

Figure 107 – 230 VAC 60 Hz, Artificial Hand.

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13 Line Surge

Differential and common mode input line surge testing was completed on a single test unit to IEC61000-4-5. Input voltage was set at 230 VAC / 60 Hz. Output was loaded at full load and operation was verified following each surge event.

13.1 *Surge*

DM Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+1000	230	L to N	0	Pass
-1000	230	L to N	0	Pass
+1000	230	L to N	90	Pass
-1000	230	L to N	90	Pass
+1000	230	L to N	180	Pass
-1000	230	L to N	180	Pass
+1000	230	L to N	270	Pass
-1000	230	L to N	270	Pass

Note: In all PASS results, no damage and no auto-restart was observed.

13.2 *Ring Wave*

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+2000	230	L to N	0	Pass
-2000	230	L to N	0	Pass
+2000	230	L to N	90	Pass
-2000	230	L to N	90	Pass
+2000	230	L to N	180	Pass
-2000	230	L to N	180	Pass
+2000	230	L to N	270	Pass
-2000	230	L to N	270	Pass

Note: In all PASS results, no damage and no auto-restart was observed.

14 ESD

Unit was subjected to up to ±8 kV contact discharge and up to ±30 kV air discharge ESD. An LED indicator connected across the resistor load was used to observe the output behavior after each ESD strike. A test failure was defined as a non-recoverable interruption of output.

Note: Output load set to full load (12 V / 1.25 A) using a 9.6 resistor.

14.1 *Contact Discharge*

Contact Voltage (kV)	Applied To	Number of Strikes	Test Result		Contact Voltage (kV)	Applied To	Number of Strikes	Test Result
+1	12 V	10	PASS		+5	12 V	10	PASS
	GND	10	PASS			GND	10	PASS
-1	12 V	10	PASS		-5	12 V	10	PASS
	GND	10	PASS			GND	10	PASS
+2	12 V	10	PASS		+6	12 V	10	PASS
	GND	10	PASS			GND	10	PASS
-2	12 V	10	PASS		-6	12 V	10	PASS
	GND	10	PASS			GND	10	PASS
+3	12 V	10	PASS		+7	12 V	10	PASS
	GND	10	PASS			GND	10	PASS
-3	12 V	10	PASS		-7	12 V	10	PASS
	GND	10	PASS			GND	10	PASS
+4	12 V	10	PASS		+8	12 V	10	PASS
	GND	10	PASS			GND	10	PASS
-4	12 V	10	PASS		-8	12 V	10	PASS
	GND	10	PASS			GND	10	PASS

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14.2 *Air Discharge*

Air Discharge Voltage (kV)	Applied To	Number of Strikes	Test Result		Air Discharge Voltage (kV)	Applied To	Number of Strikes	Test Result
+8	12 V	10	PASS		+24	12 V	10	PASS
	GND	10	PASS			GND	10	PASS
-8	12 V	10	PASS		-24	12 V	10	PASS
	GND	10	PASS			GND	10	PASS
+12	12 V	10	PASS		+26	12 V	10	PASS
	GND	10	PASS			GND	10	PASS
-12	12 V	10	PASS		-26	12 V	10	PASS
	GND	10	PASS			GND	10	PASS
+16	12 V	10	PASS		+28	12 V	10	PASS
	GND	10	PASS			GND	10	PASS
-16	12 V	10	PASS		-28	12 V	10	PASS
	GND	10	PASS			GND	10	PASS
+20	12 V	10	PASS		+30	12 V	10	PASS
	GND	10	PASS			GND	10	PASS
-20	12 V	10	PASS		-30	12 V	10	PASS
	GND	10	PASS			GND	10	PASS

15 Revision History

Date	Author	Revision	Description and Changes	Reviewed
23-Feb-21	JPB	1.0	Initial Release.	Apps & Mktg

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