Design Example Report

Title	***125 W LLC DC-DC Resonant Converter Using HiperLCS™ LCS701HG***
Specification	380 VDC Input; 24 V, 4 A and 12 V, 2.4 A Outputs
Application	LCD TV
Author	Applications Engineering Department
Document Number	DER-270
Date	September 13, 2011
Revision	1.0

Summary and Features

- Low Profile Design
  - 11 mm height idea for low profile LCD TV designs
- Low part count solution
  - Integration of controller, drivers and MOSFET half bridge in a single HiperLCS IC dramatically reduces component count and complexity
- High Operating Frequency (190 kHz)
  - Enabled use of ceramic output capacitors
  - Enabled use of low profile EFD35 core size
- High Performance
  - >94% full load efficiency
  - Excellent output cross regulation
  - Lossless capacitive current sense for reduced losses
  - Burst mode ensures regulation under no-load condition

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Table of Contents

Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved.

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1 Introduction

This document is an engineering report describing a 12 V and 24 V, 125 W LLC DC-DC converter utilizing a LCS701HG integrated LLC power stage IC. This power supply is intended as for use in an LCD TV with LED back lighting. The board requires 12 VDC and 380 VDC inputs.

The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

1.1 Important Notes

For proper operation, the RD-270 must be used with a bulk capacitor of at least 10 μF between the +380 V input and the input return placed directly across the terminals.

Note: This power supply has short-circuit protection, but no provisions for overvoltage protection. Performing an overvoltage test by disabling the TL431 (U3) or optocoupler (U2) will cause the output voltage to rise sufficiently to break down the output Schottky rectifiers (D2-D4) and destroy them.

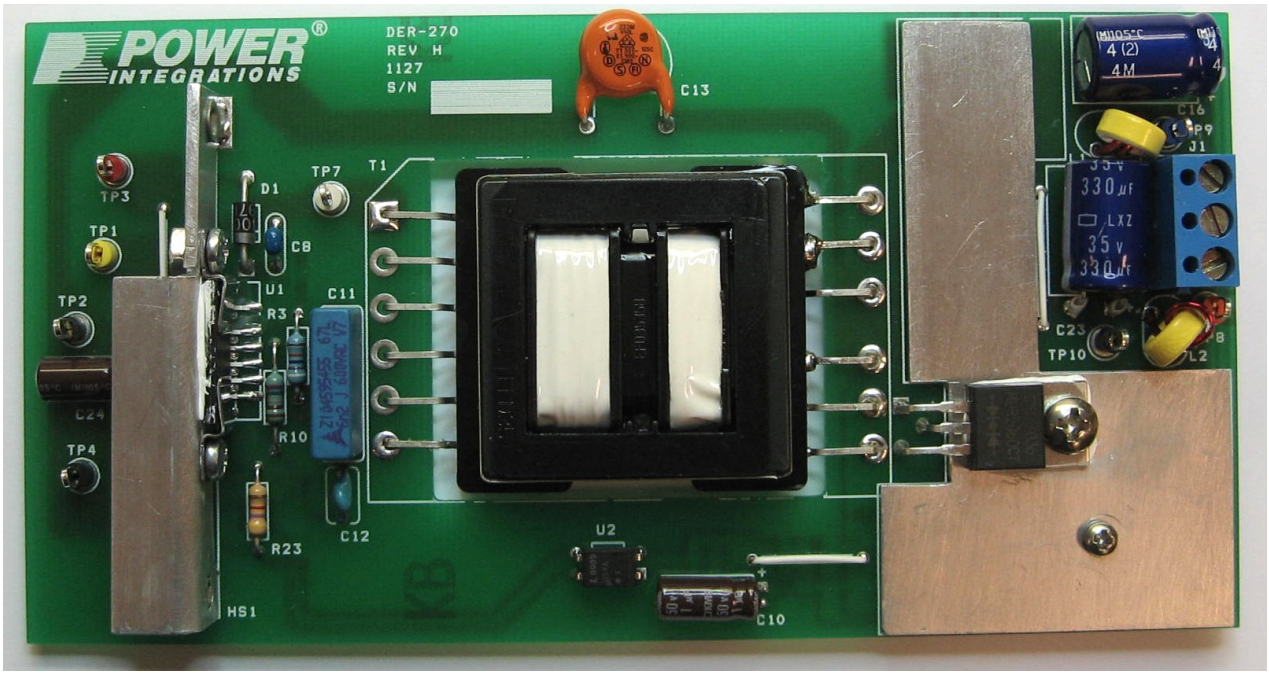

Figure 1 – Populated Circuit Board Photograph, Top View. 2.97” x 5.8” (75.44 mm x 147.32 mm).

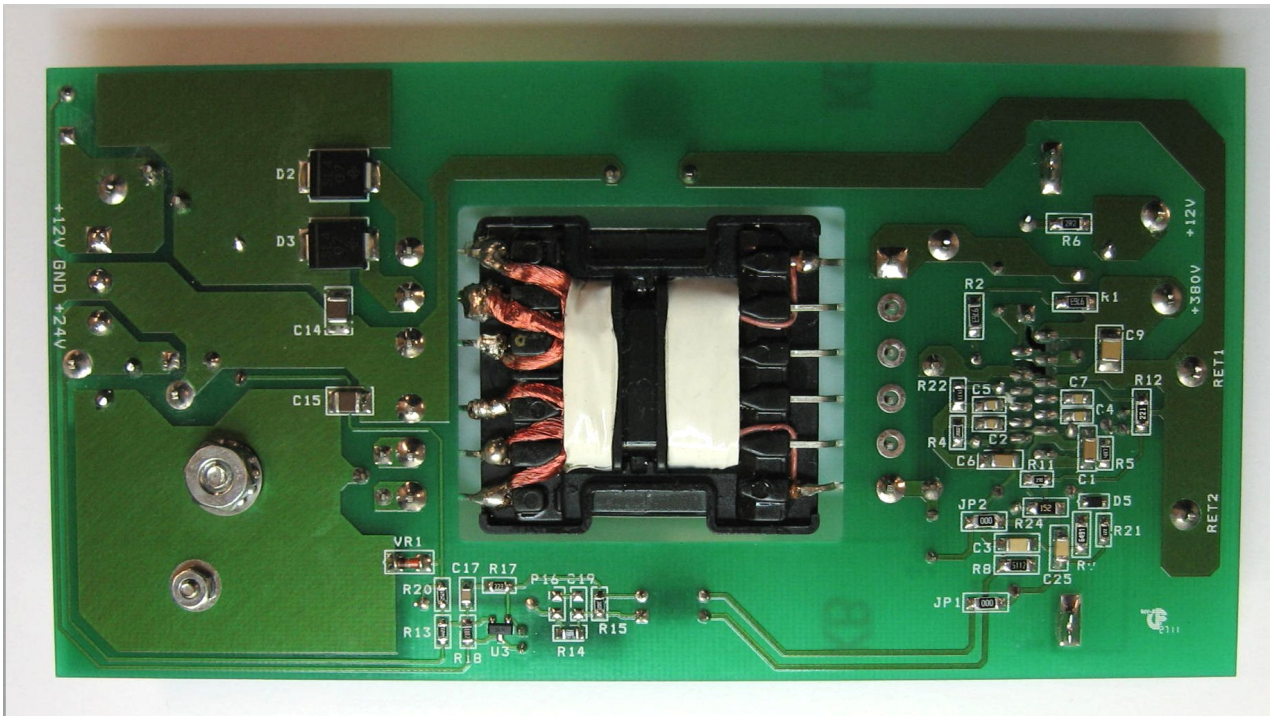

Figure 2 – Populated Circuit Board Photograph, Bottom View.

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2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	300	380	420	VDC	DC Input Only.
Frequency	f_{LINE}				Hz	N/A
No-load Input Power (230 VAC)			N/A		W	
Output						
Output Voltage 1	V_{OUT1}	11.4	12	12.6	V	± 5%
Output P-P Ripple Voltage 1	$V_{RIPPLE1}$			120	mV	20 MHz bandwidth
Output Current 1	I_{OUT1}	0.02	2.4	2.4	A	Total Load on Both outputs ≤ 125 W
Output Voltage 2	V_{OUT2}	22.8	24	25.2	V	± 5%
Output P-P Ripple Voltage 2	$V_{RIPPLE2}$			240	mV	20 MHz bandwidth
Output Current 2	I_{OUT2}	0.00	4	4	A	Total Load on Both outputs ≤ 100 W
Total Output Power						
Continuous Output Power	P_{OUT}			125	W	
Peak Output Power	P_{OUT_PEAK}			125	W	
Efficiency						
20% Load	η	87.5	88		%	DC-DC Converter Target Efficiency, Measured at 25 °C, 380 VDC Input
50% Load	η	93.5	94.0		%	DC-DC Converter Target Efficiency, Measured at 25 °C, 380 VDC Input
100% Load	η	94.0	94.2		%	DC-DC Converter Target Efficiency, Measured at 25 °C, 380 VDC Input
No-Load Input Power			0.350			Burst mode operation designated to maintain output regulation under output no-load.

3 Schematic

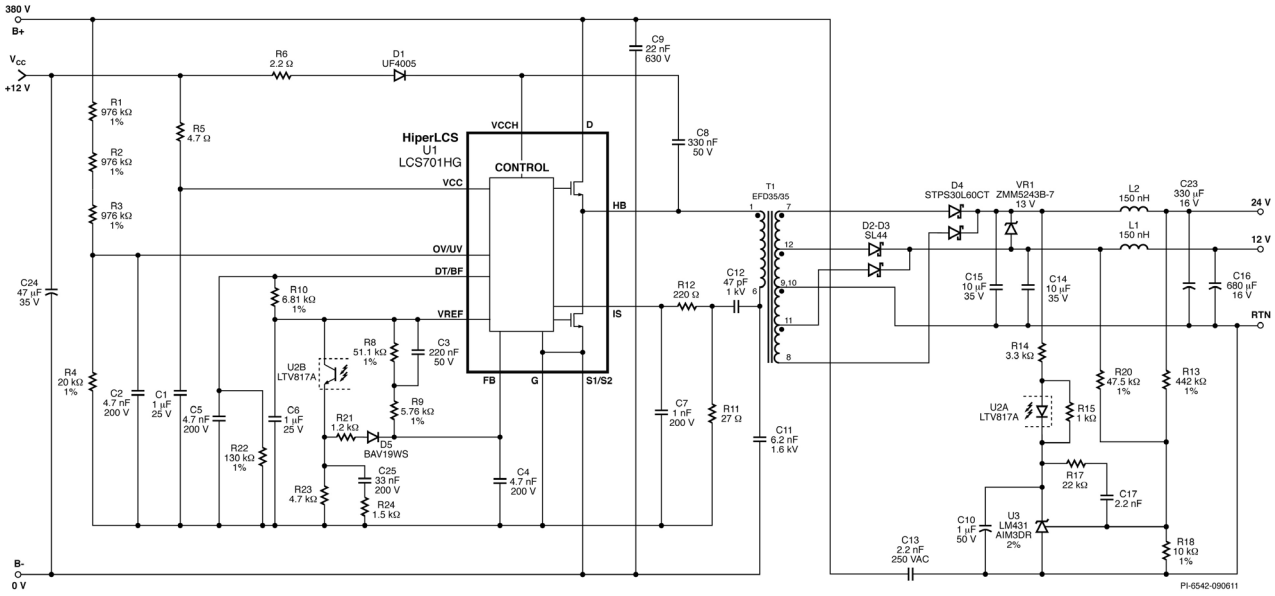

Figure 3 – Schematic.

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4 Circuit Description

The schematic in Figure 3 depicts a 12 V and 24 V, 125 W LLC DC-DC converter implemented using the LCS701HG, intended for an LCD TV application. The circuit requires +12 V and +380 V supplies to operate.

For proper operation, bulk capacitor of at least 10 μF must be used between the +380 V input (B+) and the input return (0 V), placed directly across the terminals.

4.1 Primary

Integrated circuit U1 incorporates the control circuitry, drivers and output devices necessary for an LLC resonant half-bridge converter. The HB output of U1 drives output transformer T1 via a blocking/resonating capacitor (C11). This capacitor should be rated for the operating ripple current, and the voltage rating must be chosen to withstand the voltage present during fault conditions.

Transformer T1 is designed for a leakage inductance of 100 μH. This, along with resonating capacitor C11, sets the primary series resonant frequency at ~202 kHz according to the equation:

$$f_R = \frac{1}{6.28\sqrt{L_L \times C_R}}$$

Where f_R is the series resonant frequency in Hertz, L_L is the transformer leakage inductance in Henries, and C_R is the value of the resonating capacitor (C11) in Farads.

The transformer turns ratio was set by adjusting the primary turns so that the operating frequency at nominal input voltage and full load is close to but slightly less than the previously described resonant frequency (~190 kHz). The secondary turns were chosen as a compromise between core and copper losses. AWG #42 Litz wire was used for the primary and AWG #40 Litz wire for the secondary. This combination of wire gauges provides good efficiency at 200 kHz. The number of strands for each was chosen as a balance between fit and copper losses. A 200 kHz operating frequency was found to be a good compromise between transformer size, output filter capacitance, and efficiency.

Components D1, R6, and C8 comprise the bootstrap circuit to supply the top side driver of U1. Components R5, C1, and C24 filter and bypass the +12 V input. Voltage divider R1-R4 sets the high voltage turn-on and overvoltage thresholds of U1. The voltage divider values were chosen to set the LLC turn-on point at 360 VDC and the turn-off point at 285 VDC, with the input overvoltage point at 473 VDC.

Capacitor C9 is a high frequency bypass capacitor for the +380 V input.

Capacitor C12 forms a current divider with C11, and is used to sample a portion of the primary current. Resistor R11 senses this current, and the resulting signal is filtered by R12 and C7. Capacitor C12 should be rated for the peak voltage present during fault conditions, and should use a stable, low loss dielectric such as film, SL ceramic, or NPO/COG ceramic. The capacitor used in this design is a ceramic disc with “SL” temperature characteristic, commonly used in the drivers for CCFL tubes. The values chosen set the 1 cycle (fast) current limit at 4.1 A, and the 8-cycle (slow) current limit at 2.3 A, according to the equation:

$$I_{CL} = \frac{0.5V}{\left(\frac{C12}{C11+C12}\right)(R11)}$$

I_{CL} is the 8-cycle current limit in Amperes, R11 is the current limit resistor in Ohms, and C11 and C12 are the values of the resonating and current sampling capacitors in nanofarads, respectively. For the 1-cycle current limit, substitute 0.9 V for 0.5 V in the above equation.

Resistor R12 and capacitor C7 filter primary current signal to the IS pin. Resistor R12 is set to the maximum allowable resistance of 220 Ohms. The value of C7 is set to 1 nF to avoid nuisance tripping due to noise, but not so high as to substantially affect the current limit set values as calculated above. These components should be placed close to the IS pin for maximum effectiveness. The IS pin can tolerate negative currents, so the current sense circuit does not require a complicated rectification scheme.

Resistor R10 sets the dead-time at 320 nS and maximum operating frequency for U1 at 847 kHz. The F_{MAX} input of U1 is filtered by C5. U1 is filtered by C5. The combination of R10 and R22 also selects burst mode “1” for U1. This sets the lower and upper burst threshold frequencies at 382 kHz and 437 kHz, respectively.

The FEEDBACK pin has an approximate characteristic of 2.6 kHz per μA into the FEEDBACK pin. Current driven into the FEEDBACK pin increases the operating frequency of U1, reducing the output voltage. The series combination of R8 and R9 sets the minimum operating frequency for U1, at ~124 kHz. This value is generally set to somewhat lower than the frequency required for regulation at full load and minimum bulk capacitor voltage. Resistor R8 is bypassed by C3 to provide output soft-start during start-up by initially allowing a higher current to flow into the FEEDBACK pin when the feedback loop is open. This causes the switching frequency to start high and then decrease until the output voltage is in regulation. R9 is typically set at the same value as R10 so that the initial frequency at soft-start is equal to the maximum switching frequency as set by R10. If the value of R9 is less than this, it will cause a delay before switching commences.

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Optocoupler U2 drives the U1 FEEDBACK pin through R21 which limits the maximum optocoupler current into the FEEDBACK pin. Capacitor C4 filters the FEEDBACK pin. Resistor R23 loads the optocoupler output to force it to run at a relatively high quiescent current, increasing its gain. Resistors R21 and R23 also improve large signal step response and burst mode output ripple. Diode D5 isolates R23 from the F_{MAX}/soft start network.

4.2 Output Rectification

The outputs of transformer T1 are rectified and filtered by D2-4 and C14, C15. These capacitors are X5R dielectric, carefully chosen for output ripple current rating. Standard Z5U capacitors will *not* work in this application. Output rectifier D4 is a 60 V Schottky rectifier chosen for high efficiency. Intertwining the transformer secondary halves (see transformer construction section) reduces leakage inductance between secondary halves, reducing the worst-case PIV for the 24 V output rectifiers to 57 V, allowing use of a 60 V Schottky diode with consequent higher efficiency. Additional output filtering is provided by L1-2, C16, and C23. Capacitor C16 and C23 also damp the LLC output impedance peak caused by the LLC “virtual” output series R-L and ceramic output capacitors C14 and C15. They also improve the response to fast, high amplitude load steps. Resistors R13, R18, and R20, along with the U3 reference voltage, set the output voltages of the supply. The output voltage divider is weighted such that the 12 V output is dominant, as its load is expected to be relatively constant. Error amplifier U3 drives the feedback optocoupler U2 via R14. Components C17, C25, R14, R17, and R23 determine the gain-phase characteristics of the supply. These values were chosen to provide stable operation at nominal and extreme load/input voltage combinations. Resistor R15 allows the minimum required operating current to flow in U3 when no current flow occurs in the LED of optocoupler U2. Capacitor C10 provides “soft finish” to eliminate output overshoot at turn-on. Its ESR is sufficiently high such that the output impedance of the TL431 (U3) dominates the gain-phase response.

5 PCB Layout

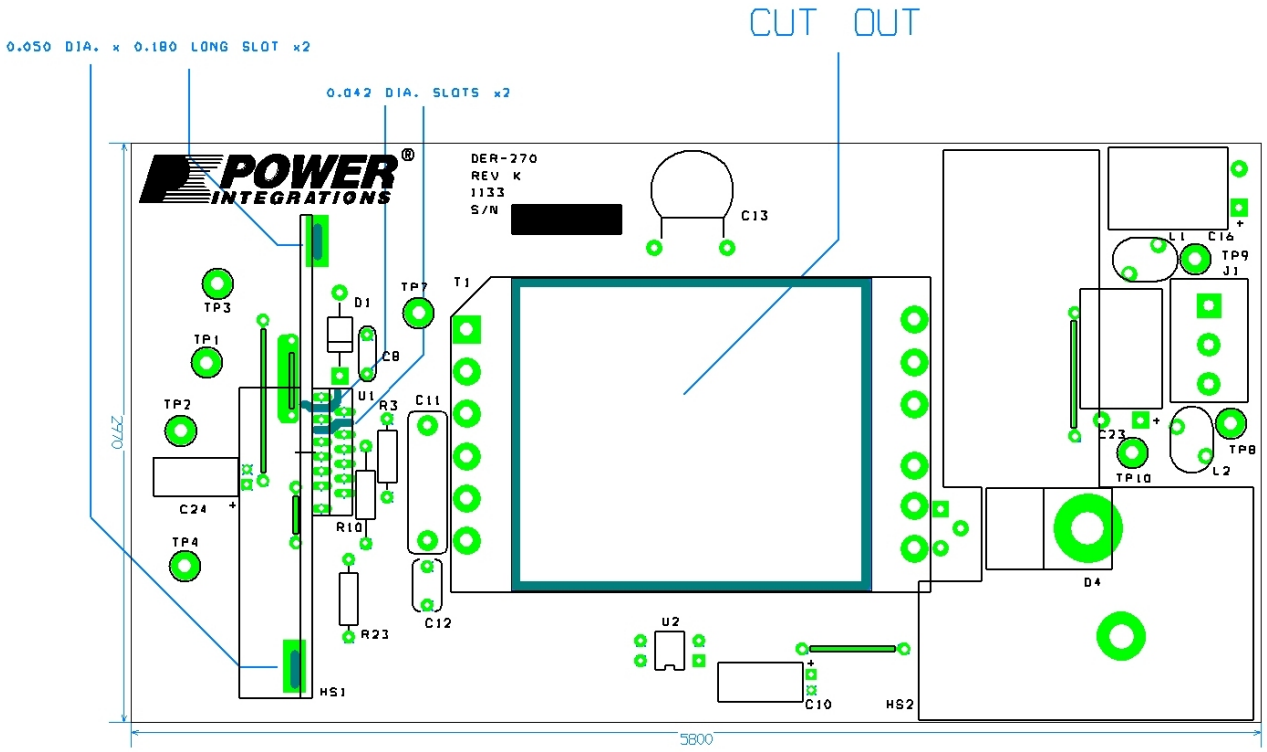

Figure 4 – Printed Circuit Layout, Top Side (board outline dimensions in thousandths of an inch).

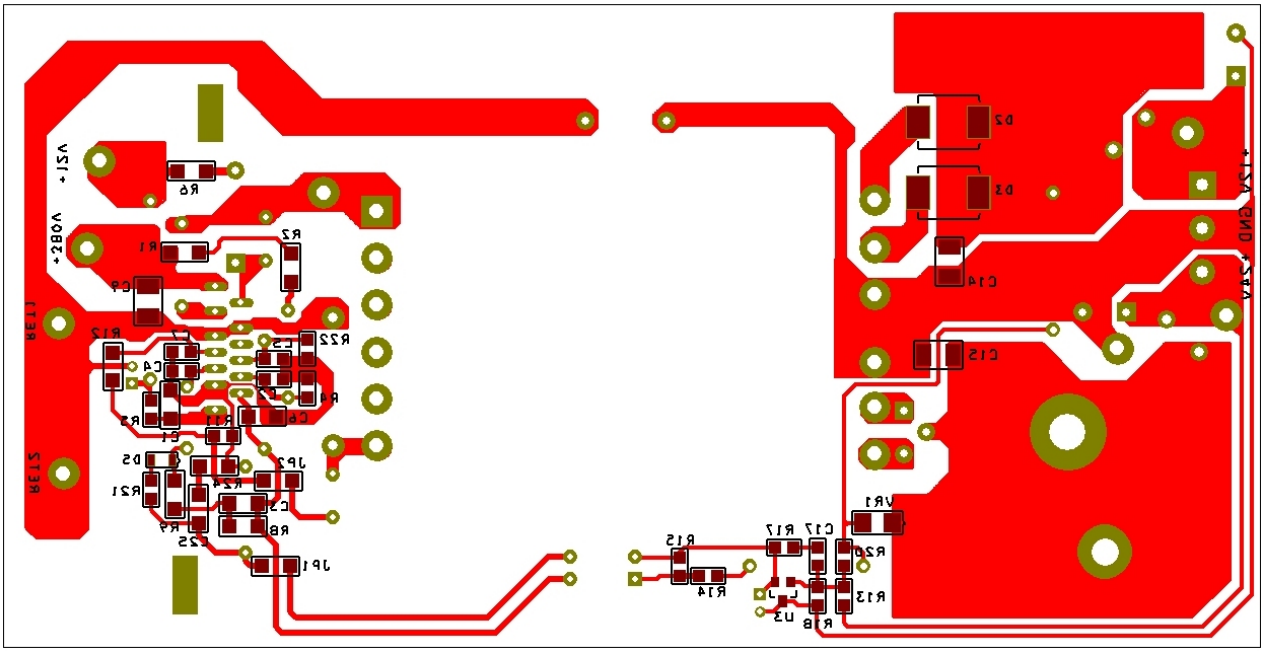

Figure 5 – Printed Circuit Layout, Bottom Side.

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6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Manufacturere
1	2	C1 C6	1 μF, 25 V, Ceramic, X7R, 1206	C3216X7R1E105K	TDK
2	3	C2 C4 C5	4.7 nF, 200 V, Ceramic, X7R, 0805	08052C472KAT2A	AVX
3	1	C3	220 nF, 50 V, Ceramic, X7R, 1206	ECJ-3YB1H224K	Panasonic
4	1	C7	1 nF, 200 V, Ceramic, X7R, 0805	08052C102KAT2A	AVX
5	1	C8	330 nF, 50 V, Ceramic, X7R	FK24X7R1H334K	TDK
6	1	C9	22 nF, 630 V, Ceramic, X7R, 1210	GRM32QR72J223KW01L	Murata
7	1	C10	1 μF, 50 V, Electrolytic, Gen. Purpose, (5 x 11)	EKMG500ELL1R0ME11D	Nippon Chemi-Con
8	1	C11	6.2 nF, 1600 V, Film	B32672L1622J000	Epcos
9	1	C12	47 pF, 1 kV, Disc Ceramic	DEA1X3A470JC1B	Murata
10	1	C13	2.2 nF, Ceramic, Y1	440LD22-R	Vishay
11	2	C14 C15	10 μF, 35 V, Ceramic, X5R, 1210	GMK325BJ106KN-T	Taiyo Yuden
12	1	C16	680 μF, 16 V, Electrolytic, Low ESR, 68 mΩ, (10 x 16)	ELXZ160ELL681MJ16S	Nippon Chemi-Con
13	1	C17	2.2 nF, 200 V, Ceramic, X7R, 0805	08052C222KAT2A	AVX
14	1	C23	330 μF, 35 V, Electrolytic, Low ESR, 68 mΩ, (10 x 16)	ELXZ350ELL331MJ16S	Nippon Chemi-Con
15	1	C24	47 μF, 35 V, Electrolytic, Gen. Purpose, (5 x 11)	EKMG350ELL470ME11D	Nippon Chemi-Con
16	1	C25	33 nF, 200 V, Ceramic, X7R, 1206	12062C333KAT2A	AVX
17	1	D1	600 V, 1 A, Ultrafast Recovery, 75 ns, DO-41	UF4005-E3	Vishay
18	2	D2 D3	40 V, 4 A, Schottky, SMD, DO-214AB	SL44-E3/57T	Vishay
19	1	D4	60 V, 30 A, Dual Schottky, TO-220AB	STPS30L60CT	ST Micro
20	1	D5	100 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV19WS-7-F	Diodes, Inc.
22	1	HS1	Heat Sink, Custom, Al, 3003, 0.62Thk		Custom
23	1	HS2	Heat Sink, DER-270-Diode, Alum 3003, 1.720" W x 2.920" H x 0.062" Thk		Custom
24	1	J1	CONN TERM BLOCK 5.08MM 3POS	ED120/3DS	On Shore Tech
25	2	JP1 JP2	0 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEY0R00V	Panasonic
26	2	L1 L2	Custom, 150 nH, ±15%, constructed on Micrometals T30-26 toroidal core		Power Integrations
27	2	NUT1 NUT2	Nut, Hex, Kep 4-40, S ZN Cr3 plating RoHS	4CKNTZR	Any RoHS Compliant Mfg.
28	1	NUT3	Nut, Hex, Kep 6-32, Zinc Plate	6CKNTZR	Any RoHS Compliant Mfg.
29	1	NUT4	Nut, Hex 2-56, SS	2CHNTS	Olander
30	2	R1 R2	976 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF9763V	Panasonic
31	1	R3	976 kΩ, 1%, 1/4 W, Metal Film	MFR-25FBF-976K	Yageo
32	1	R4	20 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF2002V	Panasonic
33	1	R5	4.7 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ4R7V	Panasonic
34	1	R6	2.2 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ2R2V	Panasonic
35	1	R8	51.1 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF5112V	Panasonic
36	1	R9	5.76 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF5761V	Panasonic
37	1	R10	6.81 kΩ, 1%, 1/4 W, Metal Film	MFR-25FBF-6K81	Yageo
38	1	R11	27 Ω, 5%, 1/4 W, Thick Film, 0805	ERJ-6GEYJ270V	Panasonic
39	1	R12	220 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ221V	Panasonic
40	1	R13	442 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF4423V	Panasonic
41	1	R14	3.3 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ332V	Panasonic
42	1	R15	1 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ102V	Panasonic
43	1	R17	22 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ223V	Panasonic

44	1	R18	10 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1002V	Panasonic
45	1	R20	47.5 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF4752V	Panasonic
46	1	R21	1.2 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ122V	Panasonic
47	1	R22	130 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1303V	Panasonic
48	1	R23	4.7 kΩ, 5%, 1/4 W, Carbon Film	CFR-25JB-4K7	Yageo
49	1	R24	1.5 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ152V	Panasonic
50	2	SCREW1 SCREW2	Screw Machine Phil 4-40 X 1/4 SS	PMSSS 440 0025 PH	Building Fasteners
51	1	SCREW3	Screw Machine Phil 6-32 X 5/16 SS	PMSSS 632 0031 PH	Building Fasteners
52	1	SCREW4	Screw Machine Phil 2-56 X 0.250" SS	2C25PPMS	Olander
53	1	T1	Transformer, EFD35/35, Horizontal, 12 pins Bobbin Bobbin Shroud Core	SNX R1608 TB21061SNX TC2106SNX ACEFD35/35BJPP95SNX	Santronics
54	1	TP1	Test Point, YEL, THRU-HOLE MOUNT	5014	Keystone
55	3	TP2 TP4 TP10	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone
56	1	TP3	Test Point, RED, THRU-HOLE MOUNT	5010	Keystone
57	1	TP7	Test Point, WHT, THRU-HOLE MOUNT	5012	Keystone
58	1	TP8	Test Point, ORG, THRU-HOLE MOUNT	5013	Keystone
59	1	TP9	Test Point, BLU, THRU-HOLE MOUNT	5127	Keystone
60	1	U1	HiperLCS, ESIP16/13	LCS701HG	Power Integrations
61	1	U2	Optocoupler, 35 V, CTR 80-160%, 4-DIP	LTV-817A	Liteon
62	1	U3	IC, REG ZENER SHUNT ADJ SOT-23	LM431AIM3/NOPB	National Semi
63	1	VR1	13 V, 5%, 500 mW, DO-213AA (MELF)	ZMM5243B-7	Diodes, Inc.
64	1	WASHER1	Washer Flat #6, SS, Zinc Plate, 0.267 OD x 0.143 ID x 0.032 Thk	620-6Z	Olander
65	2	WASHER2 WASHER3	Washer Flat #4 SS	FWSS 004	Building Fasteners
66	2	WASHER4 WASHER5	Washer Flat #2, SS, 0.149 OD x 0.089 ID x 0.016 Thk	620C2	Olander

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7 Transformer Specification

7.1 Electrical Diagram

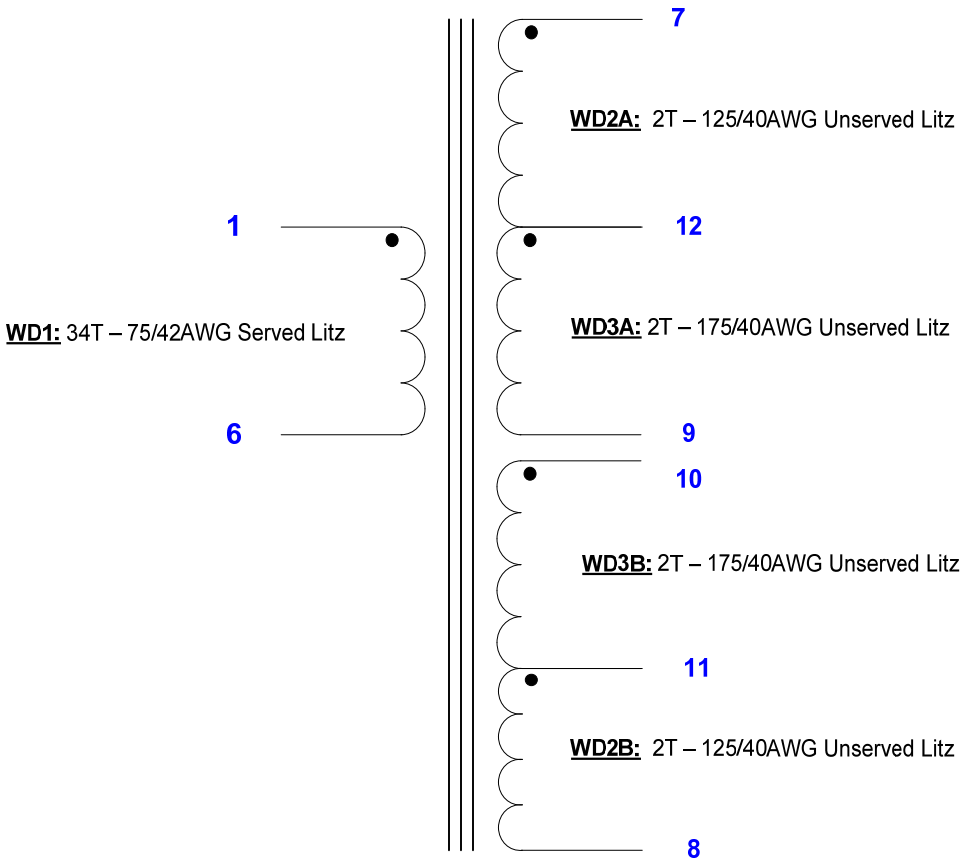

Figure 6 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from pins 1-6 to pins 7-12	3000 VAC
Primary Inductance	Pins 1-6, all other windings open, measured at 100 kHz, 0.4 V_{RMS}	580 μH, ±10%
Resonant Frequency	Pins 1-6, all other windings open	1400 kHz (Min)
Primary Leakage Inductance	Pins 1-6, with pins 7-12 shorted, measured at 100 kHz, 0.4 V_{RMS}	100 μH ±5%
Primary DCR	Pins 1-6	140 MΩ max.
Secondary DCR #1	Pins 7-12	5.1 MΩ max.
Secondary DCR #2	Pins 8-11	4.2 MΩ max.
Secondary DCR #3	Pins 7-9	8.1 MΩ max.
Secondary DCR #4	Pins 8-10	7.2 MΩ max.

7.3 Materials

Item	Description
[1]	Core Pair: Core Pair: EFD35B ungapped. Acore Ferrite ACEFD35/35BJPP95SNX or equivalent.
[2]	Bobbin: EFD35 Horizontal 12 Pins, 2 chamber, PI P/N: 25-00958-00. Santronics p/n: TB21061SNX
[3]	Bobbin Cover, EFD35, PI P/N: 25-00958-01. Santronics p/n: TC2106SNX
[4]	Tape: Polyester Film, 3M 1350F-1 or equivalent, 9.0 mm wide.
[5]	Tape: Polyester Film, 3M 1350F-1 or equivalent, 6.0 mm wide.
[6]	Litz wire: 75/#42 Single Coated, Served.
[7]	Litz wire: 125/#40 Single Coated, Unserved.
[8]	Litz wire: 175/#40 Single Coated, Unserved.
[9]	Transformer Varnish: Dolph BC-359 or equivalent.

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7.4 Transformer Build Diagram

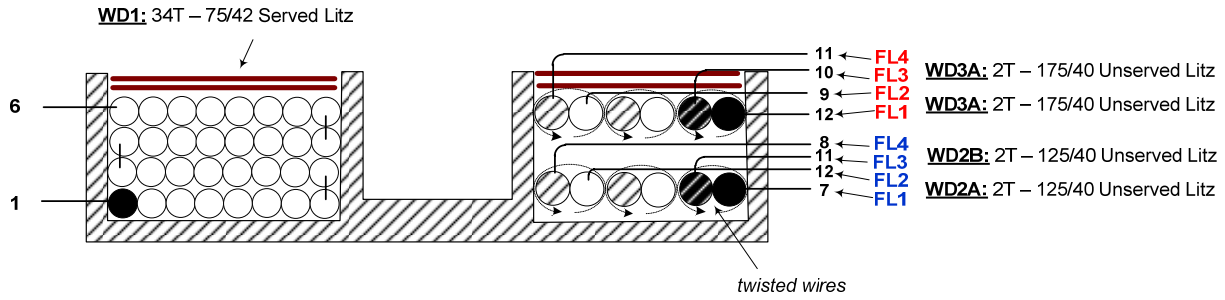
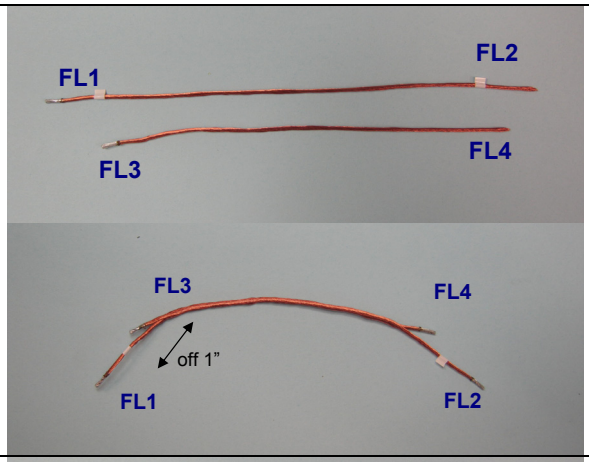
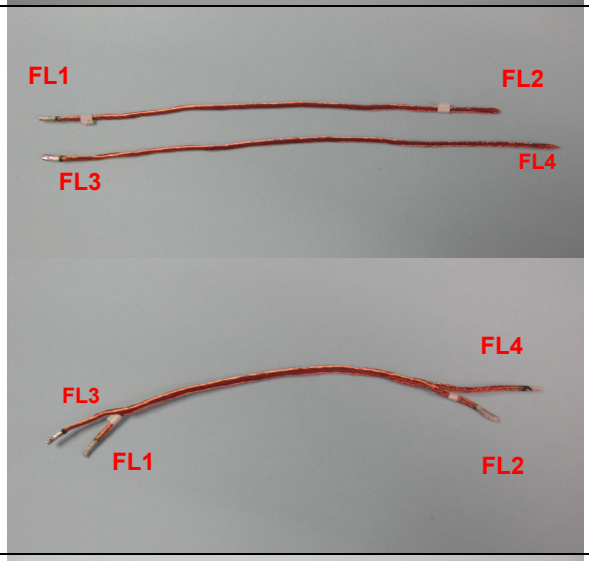
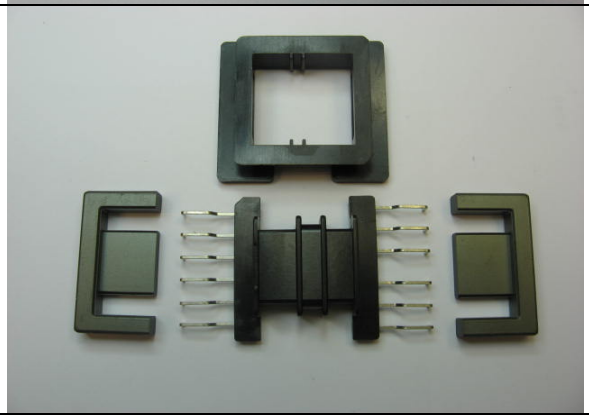


Figure 7 – Transformer Build Diagram.

7.5 Transformer Construction

Step 1: 24 V Secondary Wire Preparation	Prepare 1 strand of wire item [7] length 6.5”; tin one end, label this strand on both ends, and designate as FL1, FL2. Prepare other strand also same wire item [7] 5”; tin one end, and designate as FL3, FL4. Place these 2 strands side by side, offset~ ¾”, and twist together ~ 25 twists evenly along the length. Tin other ends for both strands. See pictures below.
Step 2: 12 V Secondary Wire Preparation	Prepare 1 strand of wire item [8] 6” length; tin one end, label this strand on both ends, and designate as FL1, FL2. Prepare other strand also same wire item [8] 6.5“; tin one end, and designate as FL3, FL4. Place these 2 strands side-by-side, offset ~ ½”, and twist together ~ 25 twists evenly along the length. Tin other ends for both strands. See pictures below.
WD1 (Primary)	Place the bobbin item [2] on the mandrel with primary side on the left side. Starting on pin 1, wind 34 turns of served Litz wire [6] in 4 layers in left-hand bobbin chamber, and finish on pin 6. Secure winding with 2 turns of tape [4].
WD2A and WD2B (24 V Secondary)	Using 24 V unserved Litz assembly prepared in step 1, start with FL1 on pin 7, and FL3 on pin 11 of bobbin [2] (see illustration). Tightly wind 2 turns in bobbin right-hand chamber. Finish with FL2 on pin 12 and FL4 on pin 8 of bobbin.
WD3A and WD3B (12 V Secondary)	Using 12 V unserved Litz assembly prepared in step 2, start with FL1 on pin 12, and FL3 on pin 10 of bobbin [2] (see illustration). Tightly wind 2 turns in bobbin right-hand chamber. Finish with FL2 on pin 9 and FL4 on pin 11 of bobbin.
Bobbin Cover	Slide bobbin cover [3] over wound bobbin as shown. Make sure cover is securely seated.
Finish	Grind core halves [1] for inductance of 580 µH ±10%. Assemble and secure core halves. Dip varnish [9].

7.6 Construction Illustrations

Step 1: **24 V Secondary** **Wire Preparation**		Prepare 1 strand of wire item [7length 6.5”; tin one end, label this strand on both ends, and designate as FL1, FL2. Prepare other strand also same wire item [7] 5”; tin one end, and designate as FL3, FL4. Place these 2 strands side-by-side, offset~ ¾”, and twist together ~25 twists evenly along the length. Tin other ends for both strands. See pictures below.
Step 2: **12 V Secondary** **Wire Preparation**		Prepare 1 strand of wire item [8] 6” length; tin one end, label this strand on both ends, and designate as FL1, FL2. Prepare other strand also same wire item [8] 6.5”; tin one end, and designate as FL3, FL4. Place these 2 strands side-by-side, offset ~ ½”, and twist together ~25 twists evenly along the length. Tin other ends for both strands. See pictures below.
Bobbin **Preparation**		

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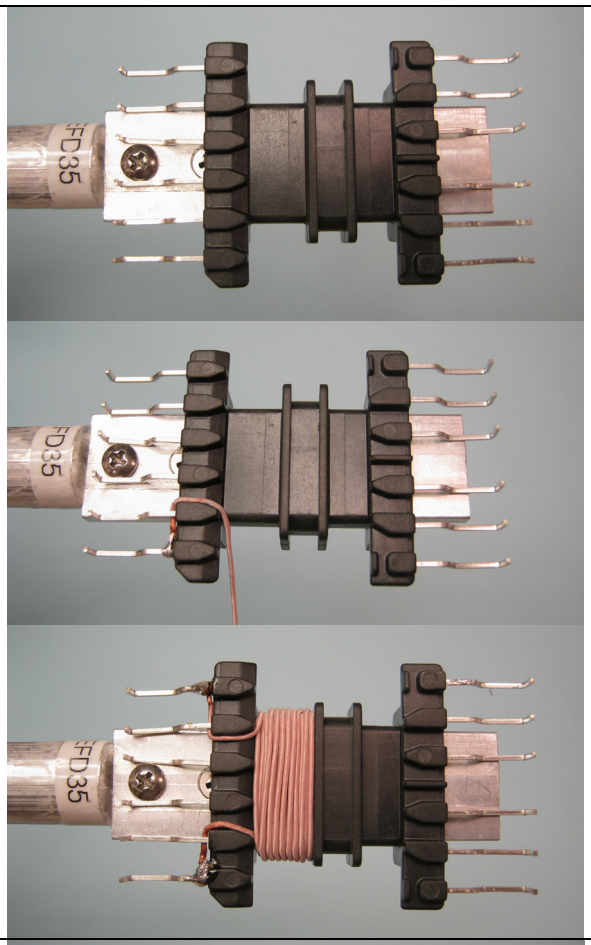
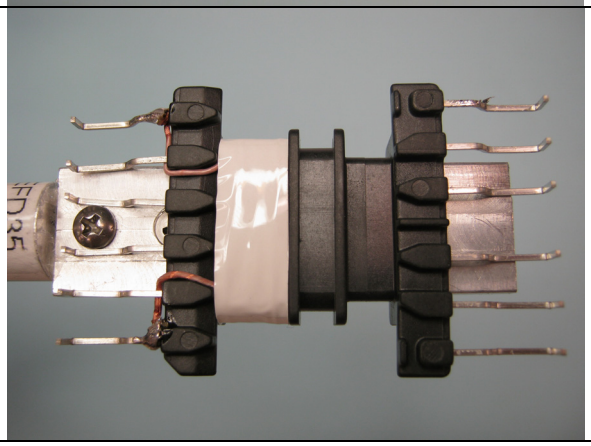
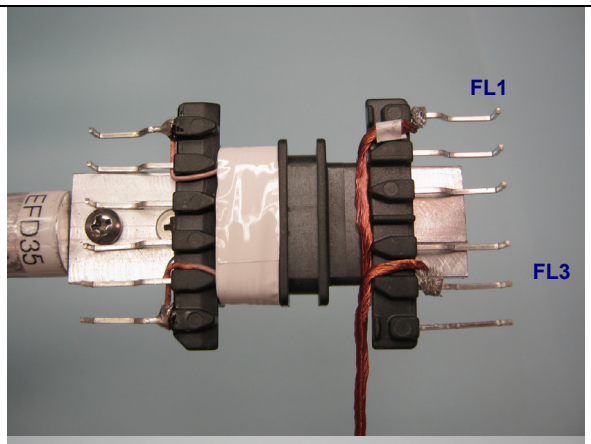
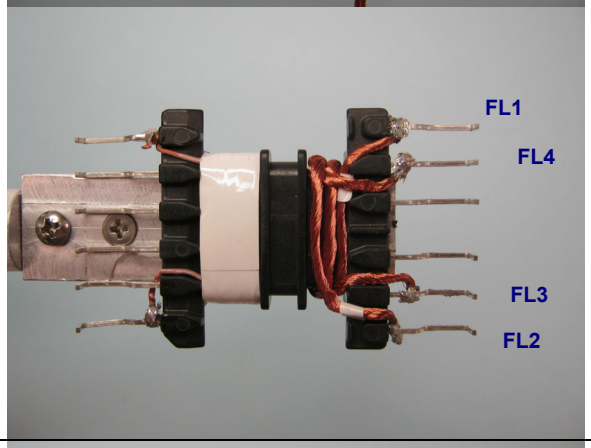
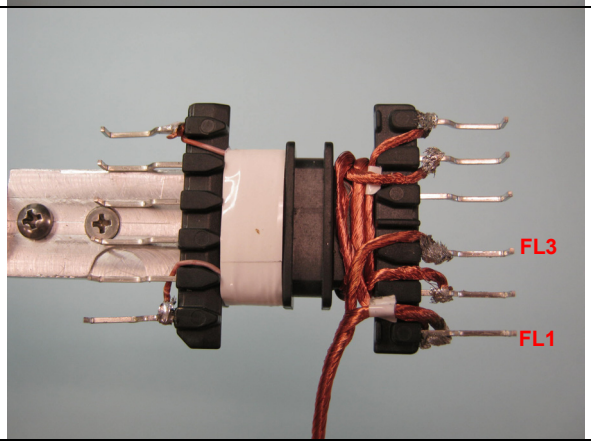
WD1 (Primary)		Place the bobbin item [2] on the mandrel with primary side on the left side. Starting on pin 1, wind 34 turns of served Litz wire [6] in 4 layers in left-hand bobbin chamber, and finish on pin 6.
WD1 (Primary) (Cont'd)		Secure winding with 2 turns of tape [4].

WD2A and WD2B (24 V Secondary)	 	Using 24 V unserved Litz assembly prepared in step 1, start with FL1 on pin 7, and FL3 on pin 11 of bobbin [2] (see illustration). Tightly wind 2 turns in bobbin right-hand chamber. Finish with FL2 on pin 12 and FL4 on pin 8 of bobbin.
WD3A and WD3B (12 V Secondary)		Using 12 V unserved Litz assembly prepared in step 2, start with FL1 on pin 12, and FL3 on pin 10 of bobbin [2] (see illustration).

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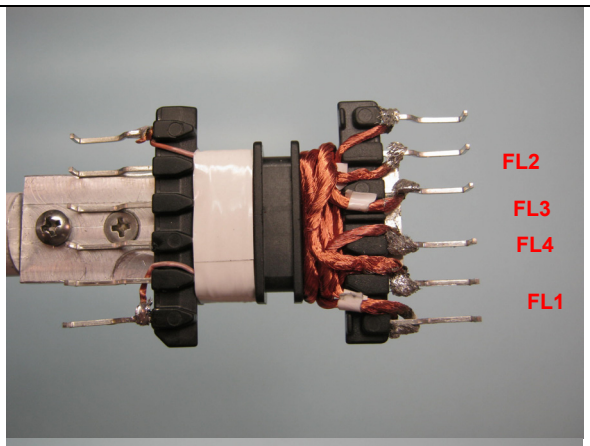
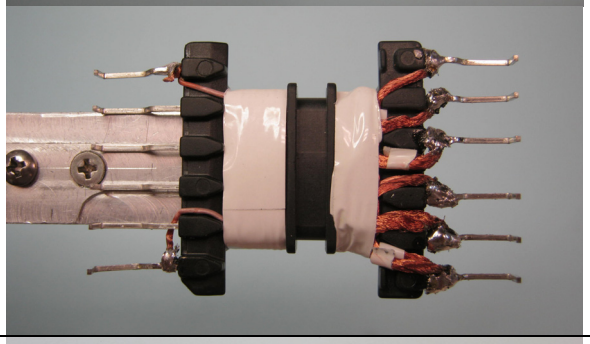
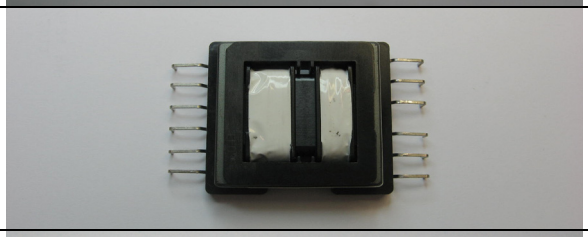
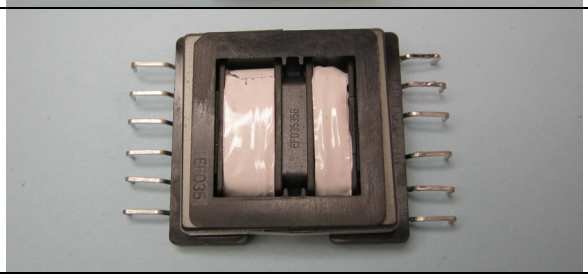
	 	Tightly wind 2 turns in bobbin right-hand chamber. Finish with FL2 on pin 9 and FL4 on pin 11 of bobbin.
Bobbin Cover		Slide bobbin cover [3] over wound bobbin as shown. Make sure cover is securely seated.
Finish		Grind core halves [1] for inductance of 580 µH ±10%. Assemble and secure core halves. Dip varnish [9].

8 Transformer Design Spreadsheet

HiperLCS_062411; Rev.1.1; Copyright Power Integrations 2011	INPUTS	INFO	OUTPUTS	UNITS	HiperLCS_062411_Rev1-1.xls; HiperLCS Half-Bridge, Continuous mode LLC Resonant Converter Design Spreadsheet
Enter Input Parameters					
Vbulk_nom			380	V	Nominal LLC input voltage
Vbrownout			280	V	Brownout threshold voltage. HiperLCS will shut down if voltage drops below this value. Allowable value is between 65% and 76% of Vbulk_nom. Set to 65% for max holdup time
Vbrownin			353	V	Startup threshold on bulk capacitor
VOV_shut			465	V	OV protection on bulk voltage
VOV_restart			448	V	Restart voltage after OV protection.
CBULK			86	uF	Minimum value of bulk cap to meet holdup time requirement; Adjust holdup time and Vbrownout to change bulk cap value
tHOLDUP			21.8	ms	Bulk capacitor hold up time
Enter LLC (secondary) outputs					**The spreadsheet assumes AC stacking of the secondaries**
VO1	24.00		24.00	V	Main Output Voltage. Spreadsheet assumes that this is the regulated output
IO1	4.00		4.00	A	Main output maximum current
VD1			0.70	V	Forward voltage of diode in Main output
PO1			96	W	Output Power from first LLC output
VO2	12.00		12.00	V	Second Output Voltage
IO2	2.40		2.40	A	Second output current
VD2	0.50		0.50	V	Forward voltage of diode used in second output
PO2			28.80	W	Output Power from second LLC output
P_LLC			125	W	Specified LLC output power
LCS Device Selection					
Device	**Auto**		**LCS701**		LCS Device
RDS-ON (MAX)			1.86	ohms	RDS-ON (max) of selected device
Coss			187	pF	Equivalent Coss of selected device
Cpri			40	pF	Stray Capacitance at transformer primary
Pcond_loss			1.3	W	Conduction loss at nominal line and full load
Tmax-hs			90	deg C	Maximum heatsink temperature
Theta J-HS			9.5	deg C/W	Thermal resistance junction to heatsink (with grease and no insulator)
Expected Junction temperature			102	deg C	Expectd Junction temperature
Ta max			50	deg C	Expected max ambient temperature
Theta HS-A			32	deg C/W	Required thermal resistance heatsink to ambient
LLC Resonant Parameter and Transformer Calculations (generates red curve)					
Po			129	W	Output from LLC converter including diode loss
Vo			24.70	V	Main Output at transformer windings (includes diode drop)
f_target	200.00		200	kHz	Desired full load switching frequency of PFC and LLC. 66 kHz to 300 kHz, recommended 250 kHz
Lpar	5		476	uH	Parallel inductance. (Lpar = Lopen - Lres for integrated transformer; Lpar = Lmag for non-integrated low-leakage transformer)
Lpri	580.00		580	uH	Primary open circuit inductance for integrated transformer; for low-leakage transformer it is sum of primary inductance and series inductor. If left blank, auto-calculation shows value necessary for loss of ZVS at 80% of Vnom
Lres	104.00		104.0	uH	Series inductance or primary leakage inductance of integrated transformer; if left blank auto-calculation is

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					for K=4
Kratio			4.6		Ratio of Lpar to Lres. Maintain value of K such that 2.1 < K < 11. Preferred Lres is such that K<7.
Cres	6.20		6.2	nF	Series resonant capacitor. Red background cells produce red graph. If Lpar, Lres, Cres, and n_RATIO_red_graph are left blank, they will be auto-calculated
Lsec	8.100		8.100	uH	Secondary side inductance of one phase of main output; measure and enter value, or adjust value until f_predicted matches what is measured ;
m			48	%	Leakage distribution factor (primary to secondary). 99% signifies most of the leakage is in primary side
n_eq			7.67		Turns ratio of LLC equivalent circuit ideal transformer
Npri	34.0		34.0		Primary number of turns; if input is blank, default value is auto-calculation so that f_predicted = f_target
Nsec	4.0		4.0		Secondary number of turns (each phase of Main output). Default value is estimate to maintain BAC<=200 mT
f_predicted			190	kHz	Expected frequency at nominal input voltage and full load; Heavily influenced by n_Ratio and primary turns
f_res			198	kHz	Series resonant frequency (defined by series inductance Lres and C)
f_brownout			132	kHz	Switching frequency at Vbrownout, full load
f_par			84	kHz	Parallel resonant frequency (defined by Lpar + Lres and C)
f_inversion			123	kHz	Min frequency, at Vbrownout and full load. Set HiperLCS minimum frequency to this value. Operation below this frequency results inoperation in gain inversion region
Vinversion			261	V	Minimum input voltage of LLC power train before low freq gain inversion point. Optimum value is equal Vbrownout
RMS Currents and Voltages					
IRMS_LLC_Primary			0.82	A	Primary winding RMS current at full load and nominal input voltage (Vbulk) and fnominal_actual
Winding 1 (Lower secondary Voltage) RMS current			5.1	A	Winding 1 (Lower secondary Voltage) RMS current
Lower Secondary Voltage Capacitor RMS current			2.0	A	Lower Secondary Voltage Capacitor RMS current
Winding 2 (Higher secondary Voltage) RMS current			1.9	A	Winding 2 (Higher secondary Voltage) RMS current
Higher Secondary Voltage Capacitor RMS current			1.2	A	Higher Secondary Voltage Capacitor RMS current
Cres_Vrms			111	V	Resonant capacitor AC RMS Voltage at full load and nominal input voltage
Virtual Transformer Trial - (generates blue curve)					
New primary turns			34.0		Trial transformer primary turns; default value is from resonant section
New secondary turns			4.0		Trial transformer secondary turns; default value is from resonant section
New Lpri			580	uH	Trial transformer open circuit inductance; default value is from resonant section
New Cres			6.1	nF	Trial value of series capacitor (if left blank calculated value chosen so f_res = f_target
New estimated Lres			104.0	uH	Trial transformer estimated Lres
New estimated Lpar			476	uH	Estimated value of Lpar for trial transformer
New estimated Lsec			8.100	uH	Estimated value of secondary leakahe inductance
New Kratio			4.6		Ratio of Lpar to Lres for trial transformer
New equivalent circuit transformer turns ratio			7.67		Estimated effective transformer turns ratio

V powertrain inversion new			262	V	Voltage on Bulk Capacitor below which ZVS is lost
f_res_trial			200	kHz	New Series resonant frequency
f_predicted_trial			192	kHz	New nominal operating frequency
IRMS_LLC_Primary			0.82	A	Primary winding RMS current at full load and nominal input voltage (Vbulk) and f_predicted_trial
Winding 1 (Lower secondary Voltage) RMS current			5.0	A	RMS current through Output 1 winding, assuming half sinusoidal waveshape
Lower Secondary Voltage Capacitor RMS current			1.9	A	Lower Secondary Voltage Capacitor RMS current
Winding 2 (Higher secondary Voltage) RMS current			3.1	A	RMS current through Output 2 winding; Output 1 winding is AC stacked on top of Output 2 winding
Higher Secondary Voltage Capacitor RMS current			1.1	A	Higher Secondary Voltage Capacitor RMS current
Transformer Core Calculations (Calculates From Resonant Parameter Section)					
Transformer Core			**EFD35/35B**		**Transformer Core**
Ae	0.57		0.57	cm^2	Enter transformer core cross-sectional area
Ve	4.57		4.57	cm^3	Enter the volume of core
Aw	60.56		60.6	mm^2	Area of window
Bw	21.00		21.0	mm	Total Width of Bobbin
Loss density			200.0	mW/cm^3	Enter the loss per unit volume at the switching frequency and BAC (Units same as kW/m^3)
MLT	5.10		5.1	cm	Mean length per turn
Nchambers			2		Number of Bobbin chambers
Wsep	7.00		7.0	mm	Winding separator distance (will result in loss of winding area)
Ploss			0.9	W	Estimated core loss
Bpkfmin			206	mT	First Quadrant peak flux density at minimum frequency.
BAC			285	mT	AC peak to peak flux density (calculated at f_predicted, Vbulk at full load)
Primary Winding					
Npri			34.0		Number of primary turns; determined in LLC resonant section
Primary gauge	42		42	AWG	Individual wire strand gauge used for primary winding
Equivalent Primary Metric Wire gauge			0.060	mm	Equivalent diameter of wire in metric units
Primary litz strands	75		75		Number of strands in Litz wire; for non-litz primary winding, set to 1
Primary Winding Allocation Factor			50	%	Primary window allocation factor - percentage of winding space allocated to primary
AW_P			20	mm^2	Winding window area for primary
Fill Factor			60%	%	% Fill factor for primary winding (typical max fill is 60%)
Resistivity_25 C_Primary			79.06	m-ohm/m	Resistivity in milli-ohms per meter
Primary DCR 25 C			137.08	m-ohm	Estimated resistance at 25 C
Primary DCR 100 C			183.69	m-ohm	Estimated resistance at 100 C (approximately 33% higher than at 25 C)
Primary RMS current			0.82	A	Measured RMS current through the primary winding
ACR_Trf_Primary			293.91	m-ohm	Measured AC resistance (at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature
Primary copper loss			0.20	W	Total primary winding copper loss at 85 C
Secondary Winding 1 (Lower secondary voltage OR Single output)					**Note - Power loss calculations are for each winding half of secondary**
Output Voltage			12.00	V	Output Voltage (assumes AC stacked windings)
Sec 1 Turns			2.00		Secondary winding turns (each phase)
Sec 1 RMS current			5.1	A	RMS current through Output 1 winding, assuming half

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(total, AC+DC)					sinusoidal waveshape
Winding current (DC component)			3.20	A	DC component of winding current
Winding current (AC RMS component)			3.96	A	AC component of winding current
Sec 1 Wire gauge			40	AWG	Individual wire strand gauge used for secondary winding
Equivalent secondary 1 Metric Wire gauge			0.080	mm	Equivalent diameter of wire in metric units
Sec 1 litz strands	175		175		Number of strands used in Litz wire; for non-litz non-integrated transformer set to 1
Resistivity_25 C_sec1			21.31	m-ohm/m	Resistivity in milli-ohms per meter
DCR_25C_Sec1			2.17	m-ohm	Estimated resistance per phase at 25 C (for reference)
DCR_100C_Sec1			2.91	m-ohm	Estimated resistance per phase at 100 C (approximately 33% higher than at 25 C)
DCR_Ploss_Sec1			0.24	W	Estimated Power loss due to DC resistance (both secondary phases)
ACR_Sec1			4.66	m-ohm	Measured AC resistance per phase(at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature . Default value of ACR is twice the DCR value at 100 C
ACR_Ploss_Sec1			0.15	W	Estimated AC copper loss (both secondary phases)
Total winding 1 Copper Losses			0.38	W	Total (AC + DC) winding copper loss for both secondary phases
Capacitor RMS current			1.2	A	Output capacitor RMS current
Co1			5.4	uF	Secondary 1 output capacitor
Capacitor ripple voltage			3.0	%	Peak to Peak ripple voltage on secondary 1 output capacitor
Output rectifier RMS Current			1.9	A	Schottky losses are a stronger function of load DC current. Sync Rectifier losses are a function of RMS current
Secondary Winding 2 (Higher secondary voltage)					**Note - Power loss calculations are for each winding half of secondary**
Output Voltage			24.00	V	Output Voltage (assumes AC stacked windings)
Sec 2 Turns			2.00		Secondary winding turns (each phase) AC stacked on top of secondary winding 1
Sec 2 RMS current (total, AC+DC)			3.2	A	RMS current through Output 2 winding; Output 1 winding is AC stacked on top of Output 2 winding
Winding current (DC component)			2.0	A	DC component of winding current
Winding current (AC RMS component)			2.5	A	AC component of winding current
Sec 2 Wire gauge			40	AWG	Individual wire strand gauge used for secondary winding
Equivalent secondary 2 Metric Wire gauge			0.080	mm	Equivalent diameter of wire in metric units
Sec 2 litz strands	125		125		Number of strands used in Litz wire; for non-litz non-integrated transformer set to 1
Resistivity_25 C_sec2			29.83	m-ohm/m	Resistivity in milli-ohms per meter
Transformer Secondary MLT			5.10	cm	Mean length per turn
DCR_25C_Sec2			3.04	m-ohm	Estimated resistance per phase at 25 C (for reference)
DCR_100C_Sec2			4.08	m-ohm	Estimated resistance per phase at 100 C (approximately 33% higher than at 25 C)
DCR_Ploss_Sec1			0.05	W	Estimated Power loss due to DC resistance (both secondary halves)
ACR_Sec2			6.52	m-ohm	Measured AC resistance per phase(at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature . Default value of ACR is twice the DCR value at 100 C
ACR_Ploss_Sec2			0.08	W	Estimated AC copper loss (both secondary halves)
Total winding 2 Copper Losses			0.13	W	Total (AC + DC) winding copper loss for both secondary halves

Capacitor RMS current			2.0	A	Output capacitor RMS current
Co2			4.5	uF	Secondary 2 output capacitor
Capacitor ripple voltage			3.0	%	Peak to Peak ripple voltage on secondary 1 output capacitor
Output rectifier RMS Current			3.2	A	Schottky losses are a stronger function of load DC current. Sync Rectifier losses are a function of RMS current
Transformer Loss Calculations					**Does not include fringing flux loss from gap**
Primary copper loss (from Primary section)			0.20	W	Total primary winding copper loss at 85 C
Secondary copper Loss			0.51	W	Total copper loss in secondary winding
Transformer total copper loss			0.71	W	Total copper loss in transformer (primary + secondary)
AW_S			20.19	mm^2	Area of window for secondary winding
Secondary Fill Factor			50%	%	% Fill factor for secondary windings; typical max fill is 60% for served and 75% for unserved Litz
Signal Pins Resistor Values					
Dead Time	350		350	ns	Dead time
Burst Mode	**1**		**1**		Select Burst Mode: 1, 2, and 3 have hysteresis and have different frequency thresholds
f_max			774	kHz	Max internal clock frequency, dependent on dead-time setting. Is also start-up frequency
f_burst_start			347.1	kHz	Lower threshold frequency of burst mode, provides hysteresis. This is switching frequency at restart after a bursting off-period
f_burst_stop			396.6	kHz	Upper threshold frequency of burst mode; This is switching frequency at which a bursting off-period stops
DT/BF pin upper divider resistor			7.62	k-ohms	Resistor from DT/BF pin to VREF pin
DT/BF pin lower divider resistor			144.9	k-ohms	Resistor from DT/BF pin to G pin
Rstart			6.50	k-ohms	Start-up resistor - resistor in series with soft-start capacitor; equivalent resistance from FB to VREF pins at startup. Use default value unless additional start-up delay is desired.
Start-up delay			0.0	ms	Start-up delay; delay before switching begins. Reduce R_START to increase delay
Rfmin			50.9	k-ohms	Resistor from VREF pin to FB pin, to set min operating frquency; This resistor plus Rstart determine f_MIN
C_softstart			0.33	uF	Softstart capacitor. Recommended values are between 0.1 uF and 0.47 uF
Ropto			1.3	k-ohms	Resistor in series with opto emitter
OV/UV pin lower resistor			22.0	k-ohm	Lower resistor in OV/UV pin divider
OV/UV pin upper resistor			3.21	M-ohm	Total upper resistance in OV/UV pin divider
LLC Capacitive Divider Current Sense Circuit					
Slow current limit			2.30	A	8-cycle current limit - check postivie half-cycles during brownout and startup
Fast current limit			4.14	A	1-cycle current limit - check positive half-cycles during startup
LLC sense capacitor			47	pF	HV sense capacitor, forms current divider with main resonant capacitor
RLLC sense resistor			28.9	ohms	LLC current sense resistor, senses current in sense capacitor
IS pin current limit resistor			220	ohms	Limits current from sense resistor into IS pin when voltage on sense R is < -0.5V
IS pin noise filter capacitor			1.0	nF	IS pin bypass capacitor; forms a pole with IS pin current limit capacitor
IS pin noise filter pole frequency			724	kHz	This pole attenuates IS pin signal

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Loss Budget					
LCS device Conduction loss			1.3	W	Conduction loss at nominal line and full load
Output diode Loss			2.8	W	Estimated diode losses
Transformer estimated total copper loss			0.71	W	Total copper loss in transformer (primary + secondary)
Transformer estimated total core loss			0.9	W	Estimated core loss
Total transformer losses			1.6	W	Total transformer losses
Total estimated losses			5.7	W	Total losses in LLC stage
Estimated Efficiency			96%	%	Estimated efficiency
PIN			130	W	LLC input power
Secondary Turns and Voltage Centering Calculator					**This is to help you choose the secondary turns - Outputs not connected to any other part of spreadsheet**
V1			24.00	V	Target regulated output voltage Vo1. Change to see effect on slave output
V1d1			0.70	V	Diode drop voltage for Vo1
N1			4.00		Total number of turns for Vo1
V1_Actaul			24.00	V	Expected output
V2			12.00	V	Target output voltage Vo2
V2d2			0.50	V	Diode drop voltage for Vo2
N2			2.00		Total number of turns for Vo2
V2_Actual			11.85	V	Expected output voltage
Separate Series Inductor (For Non-Integrated Transformer Only)					**Not applicable if using integrated magnetics - not connected to any other part of spreadsheet**
Lsep			104.00	uH	Desired inductance of separate inductor
Ae_Ind			0.53	cm^2	Inductor core cross-sectional area
Inductor turns			16		Number of primary turns
BP_fnom			153	mT	AC flux for core loss calculations (at f_predicted and full load)
Expected peak primary current			2.3	A	Expected peak primary current
BP_fmin			285	mT	Peak flux density, calculated at minimum frequency fmin
Inductor Litz gauge			43	AWG	Individual wire strand gauge used for primary winding
Equivalent Inductor Metric Wire gauge			0.055	mm	Equivalent diameter of wire in metric units
Inductor litz strands			125		Number of strands used in Litz wire
Inductor parallel wires			1		Number of parallel individual wires to make up Litz wire
Resistivity_25 C_Sep_Ind			59.8	m-ohm/m	Resistivity in milli-ohms per meter
Inductor MLT			7.00	cm	Mean length per turn
Inductor DCR 25 C			67.0	m-ohm	Estimated resistance at 25 C (for reference)
Inductor DCR 100 C			89.8	m-ohm	Estimated resistance at 100 C (approximately 33% higher than at 25 C)
ACR_Sep_Inductor			143.6	m-ohm	Measured AC resistance (at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature
Inductor copper loss			0.10	W	Total primary winding copper loss at 85 C

9 Output Inductor Specification

9.1 Electrical Diagram

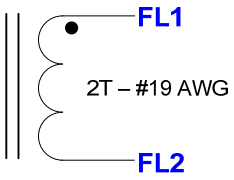

Figure 8 – Inductor Electrical Diagram.

9.2 Electrical Specifications

Inductance	Pins FL1-FL2, all other windings open, measured at 100 kHz, 0.4 V_{RMS}	150 nH ±15%

9.3 Material List

Item	Description
[1]	Powdered Iron Toroidal Core: Micrometals T30-26
[2]	Magnet wire: 19 AWG Solderable Double Coated

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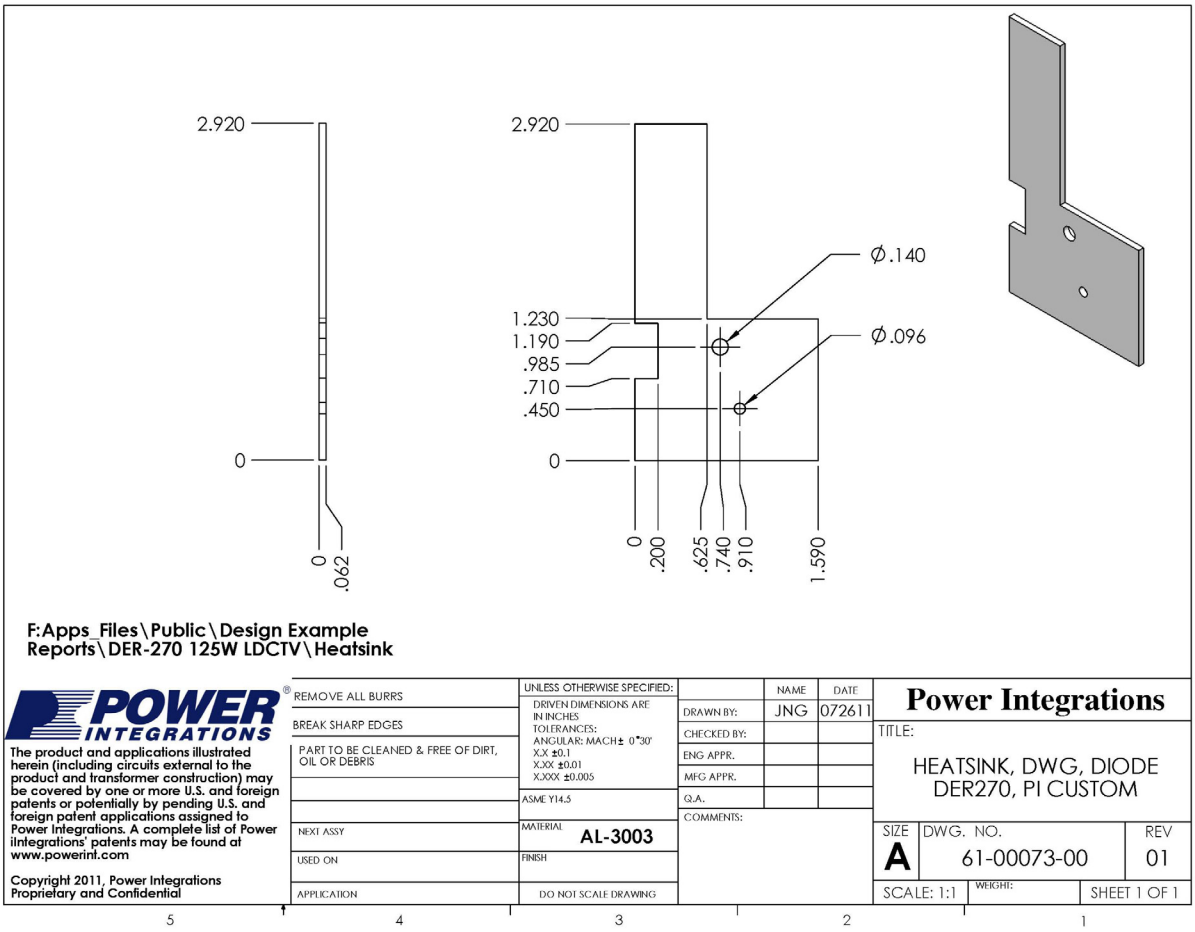
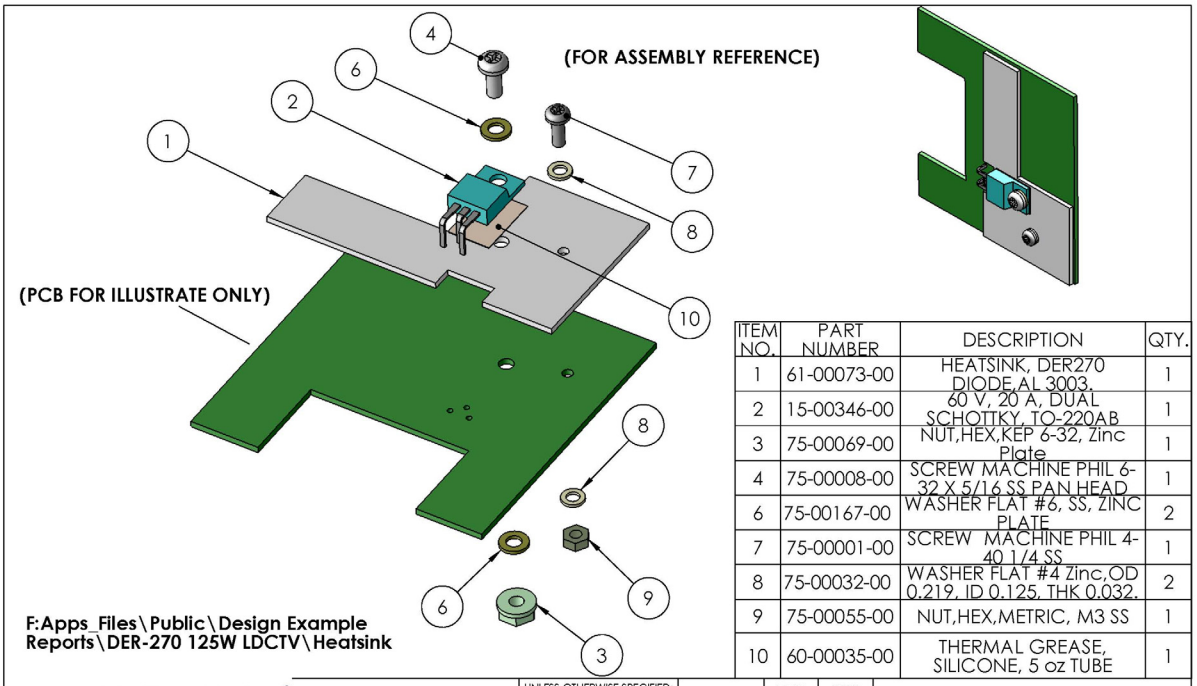
10 Heat Sink Assemblies

10.1 Diode Heat Sink

10.1.1 Diode Heat Sink Drawing



10.1.1 Diode Heat Sink Assembly Drawing



ITEM NO.	PART NUMBER	DESCRIPTION	QTY.
1	61-00073-00	HEATSINK, DER270 DIODE,AL 3003,	1
2	15-00346-00	60 V, 20 A, DUAL SCHOTTKY, TO-220AB	1
3	75-00069-00	NUT,HEX,KEP 6-32, Zinc Plate	1
4	75-00008-00	SCREW MACHINE PHIL 6-32 X 5/16 SS PAN HEAD	1
6	75-00167-00	WASHER FLAT #6, SS, ZINC PLATE	2
7	75-00001-00	SCREW MACHINE PHIL 4-40 1/4 SS	1
8	75-00032-00	WASHER FLAT #4 Zinc,OD 0.219, ID 0.125, THK 0.032,	2
9	75-00055-00	NUT,HEX,METRIC, M3 SS	1
10	60-00035-00	THERMAL GREASE, SILICONE, 5 oz TUBE	1

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BREAK SHARP EDGES
PART TO BE CLEANED & FREE OF DIRT, OIL OR DEBRIS
NEXT ASSY
USED ON
APPLICATION

UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN INCHES
TOLERANCES:
ANGULAR: MACH± 0°30'
X.X ±0.1
X.XX ±0.01
X.XXX ±0.005
ASME Y14.5
MATERIAL
FINISH
DO NOT SCALE DRAWING

	NAME	DATE
DRAWN BY:	JNG	072611
CHECKED BY:		
ENG APPR.		
MFG APPR.		
Q.A.		
COMMENTS:		

Power Integrations

TITLE: HEATSINK, ASSY, DIODE DER270-PI CUSTOM

SIZE	DWG. NO.	REV
A	61-00073-02	01
SCALE: 1:4	WEIGHT:	SHEET 1 OF 1

5 4 3 2 1

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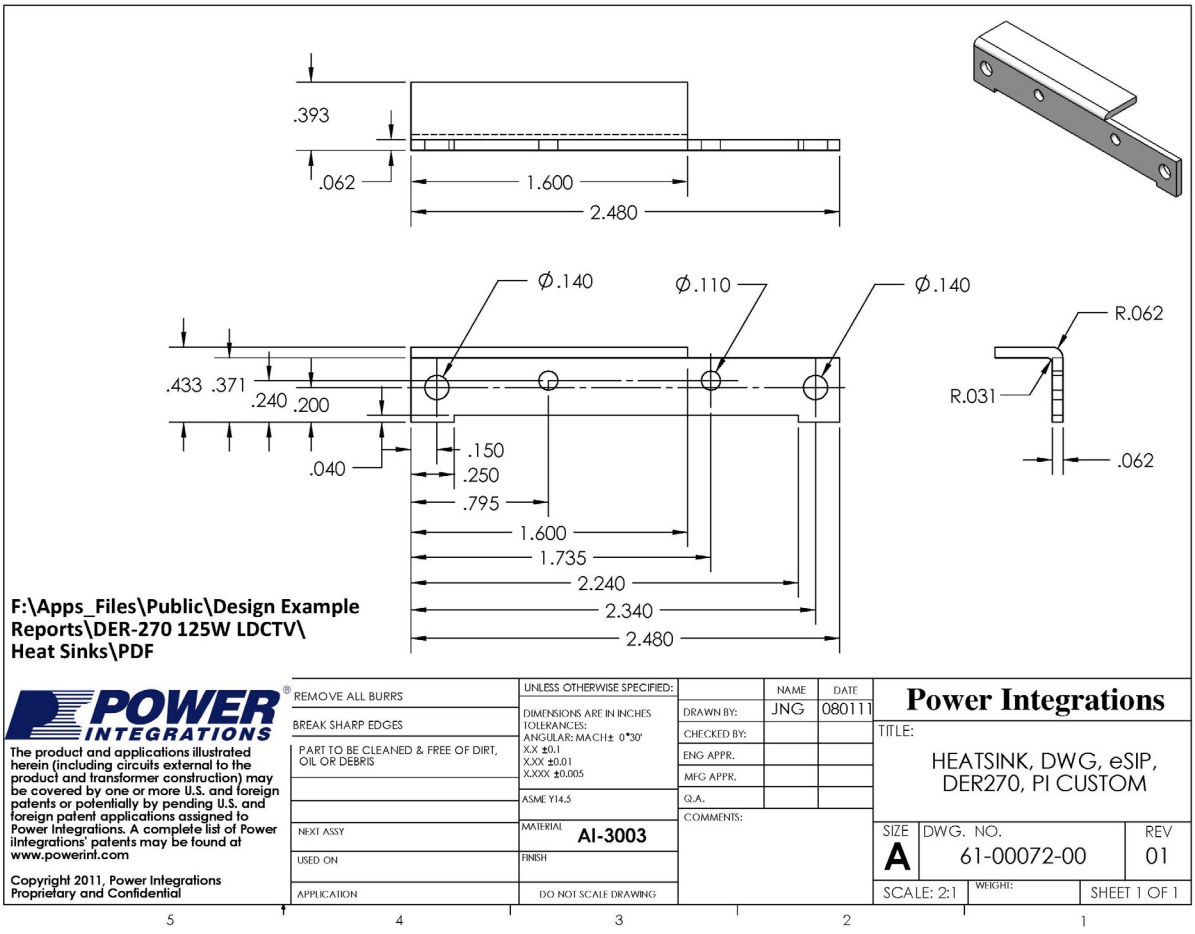
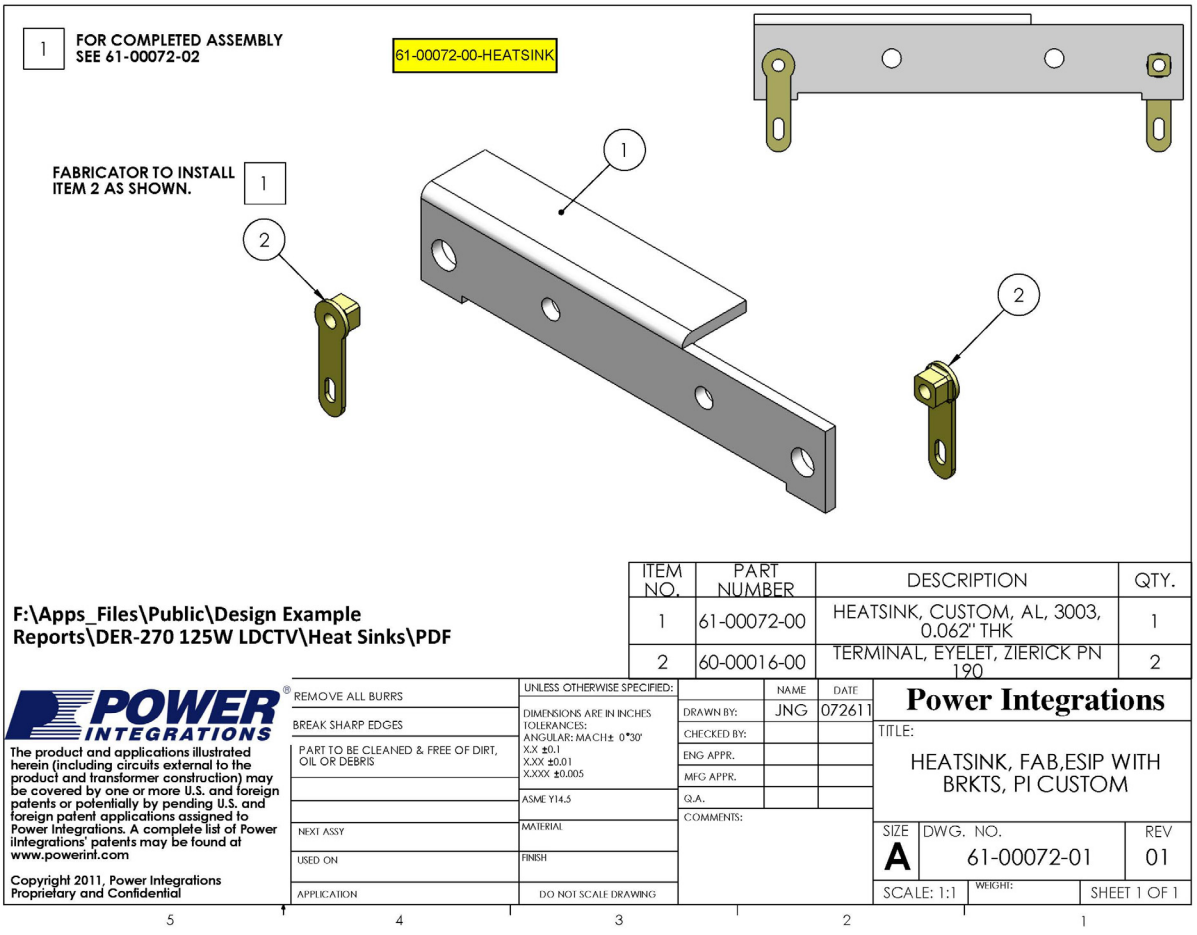
10.2 HiperLCS Heat Sink

10.2.1 HiperLCS Heat Sink Drawing



10.2.1 HiperLCS Heat Sink Fabrication Assembly Drawing



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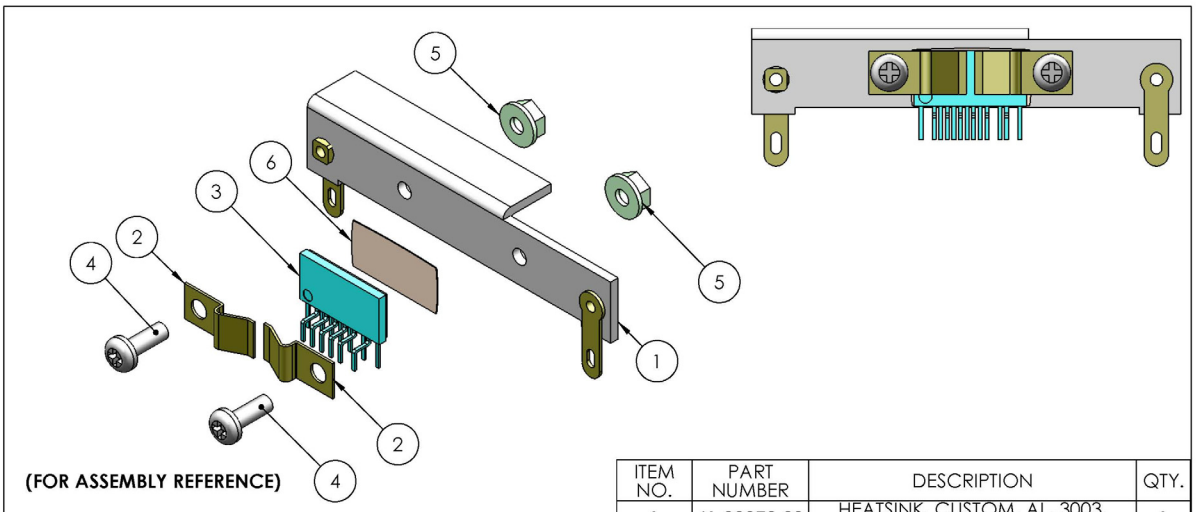
10.2.1 HiperLCS and Heat Sink Assembly Drawing



ITEM NO.	PART NUMBER	DESCRIPTION	QTY.
1	61-00072-00	HEATSINK, CUSTOM, AL, 3003, 0.062" THK	1
2	60-00037-00	EDGE CLIP 14.3mm L x 6.35mm W	2
3	10-00513-00	HiperLCS,LC701HG,ESIP16/13	1
4	75-00001-00	SCREW MACHINE PHIL 4-40 1/4 SS	2
5	75-00068-00	NUT,HEX,KEP 4-40, S ZN CR3 PLATE	2
6	66-00035-00	THERMALLY SILICONE ,GREASE, 5 OZ TUBE	1

F:\Apps_Files\Public\Design Example Reports\DER-270 125W LDCTV\Heat Sinks\PDF

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DIMENSIONS ARE IN INCHES
TOLERANCES:
ANGULAR: MACH ± 0°30'
X.X ±0.1
X.XX ±0.01
X.XXX ±0.005
ASME Y14.5
MATERIAL
FINISH
DO NOT SCALE DRAWING

	NAME	DATE
DRAWN BY:	JNG	072611
CHECKED BY:		
ENG APPR.		
MFG APPR.		
Q.A.		

COMMENTS:

Power Integrations

TITLE: HEATSINK, ASSY, ESIP WITH BRKTS, DER270, PI CUSTOM

SIZE A | DWG. NO. 61-00072-02 | REV 01

SCALE: 1:2 | WEIGHT: | SHEET 1 OF 1

5 4 3 2 1

11 Performance Data

11.1 Efficiency – 100%, 50%, 20% and 10% load

11.1.1 Efficiency Data

P_{IN}	V_{OUT1}	I_{OUT1}	V_{OUT2}	I_{OUT2}	P_{OUT}	Efficiency (%)
133	24.12	4	12.02	2.4	125.328	94.23
66.8	24.17	2	12.02	1.2	62.764	93.96
28.59	24.19	0.8	12.02	0.48	25.1216	87.87
15.46	24.19	0.4	12.02	0.24	12.5608	81.25
8.86	24.19	0.2	12.01	0.12	6.2792	70.87
5.01	24.21	0.08	12.02	0.05	2.5378	50.65
3.52	24.17	0.04	12.02	0.02	1.2072	34.30
0.326	24.86	0	11.98	0	0	

11.2 Output Cross Regulation

To obtain the data shown below, one output was adjusted to maximum load, while the other was varied between zero load and the maximum load consistent with a maximum total output power of 125 W.

11.2.1 Cross Regulation Data

Cross Regulation 1				Cross Regulation 2			
V_{OUT1}	I_{OUT1}	V_{OUT2}	I_{OUT2}	V_{OUT1}	I_{OUT1}	V_{OUT2}	I_{OUT2}
24.14	4	12.01	2.4	24.14	4	12.01	2.4
24.25	2	12	2.4	24.09	4	12.03	1.5
24.31	1	11.99	2.4	24.05	4	12.04	1
24.37	0.5	11.99	2.4	24	4	12.04	0.5
24.41	0.25	11.98	2.4	23.94	4	12.05	0.2
24.46	0.1	11.98	2.4	23.9	4	12.06	0.1
24.49	0.05	11.97	2.4	23.85	4	12.06	0.05
24.55	0.02	11.97	2.4	23.8	4	12.07	0.02
24.57	0.01	11.96	2.4	23.78	4	12.07	0.01
24.8	0	11.94	2.4	20.32	4	12.45	0

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11.3 Start and Shutdown Bulk Voltage

11.3.1 Bulk Voltage Start and Shutdown Data (Maximum Load)

With +12 VDC applied to the VCC input, start-up voltage was 356 VDC, output shutdown occurred at 283 VDC.

12 Waveforms

12.1 Half Bridge Voltage and Current, Normal Operation

Measured at 380 VDC input.

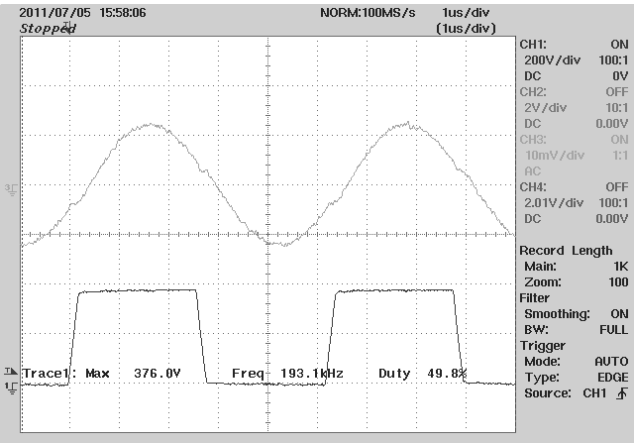

Figure 9 – Primary V_{IN}, Full Load.
Upper: Primary Current, 1 A / div.
Lower: Primary Voltage, 100 V, 2 μs / div.

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12.2 Output Voltage Start-up Profile

Figures 10 to 14 were taken using a passive resistor load.

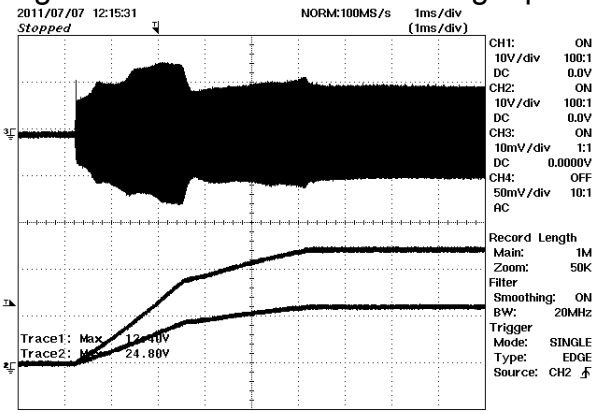

Figure 10 – Full load Start-up, Resistive Load.
Upper: Primary Current, 1 A / div.
Lower: Output Voltage, 10 V,
2 ms / div.

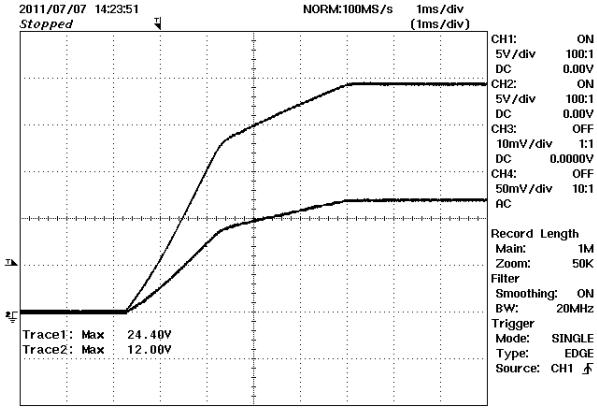

Figure 11 – No-load Output Voltage at Start-up,
5 V, 1 ms / div.

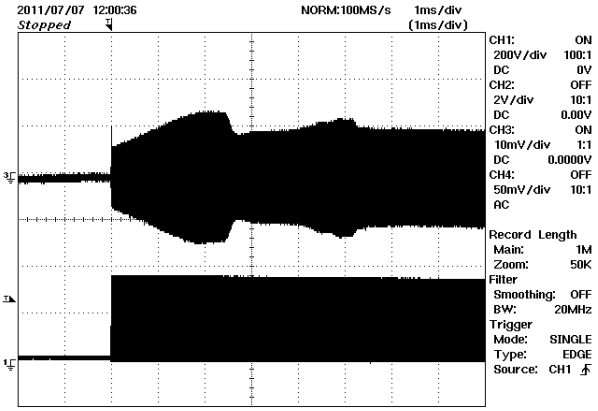

Figure 12 – Full Load Startup, Resistive Load.
Upper: Primary Current, 1 A / div.
Lower: Primary Voltage, 200 V,
1 ms / div.

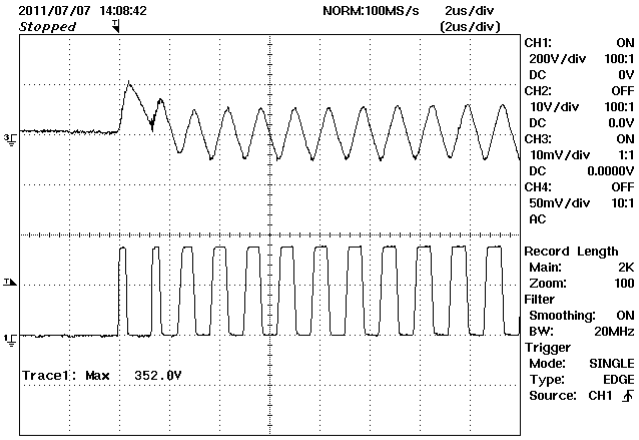

Figure 13 – Full Load Startup Showing Initial Current Spike, Resistive Load.
Upper: Primary Current, 1 A / div.
Lower: Primary Voltage, 200 V,
2 μs / div.

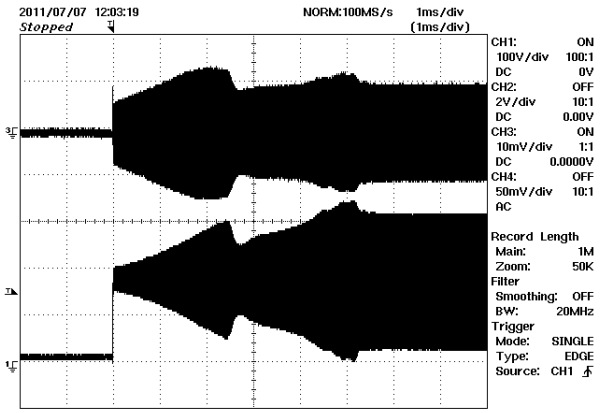

Figure 14 – Full Load Start-up, Resistive Load
Upper: Primary Current, 1 A / div.
Lower: Resonating Capacitor Voltage,
100 V, 1 ms / div.

12.3 Output Brown-Out

Figures 15 to 17 taken by switching off input voltage supply and triggering oscilloscope on rise of primary current.

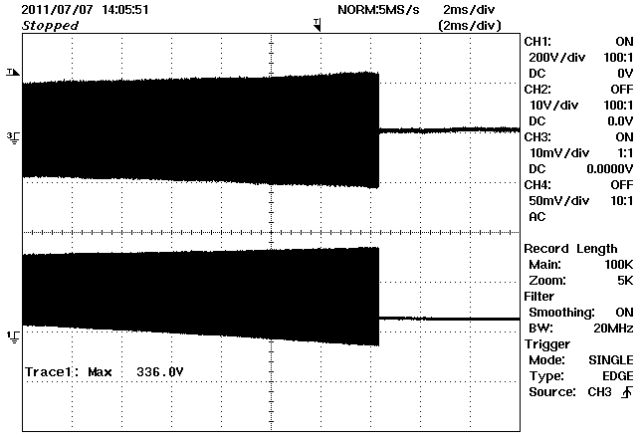

Figure 15 – Output Brown-Out.
Upper: Primary Current, 2 A / div.
Bottom: Primary Voltage,
200 V, 2 ms / div.

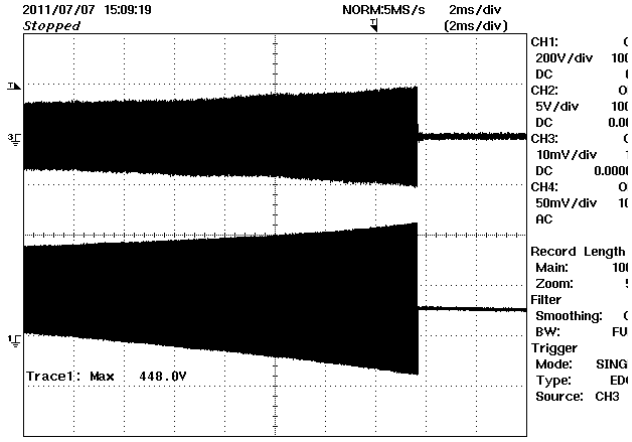

Figure 16 – Output Brown-Out.
Upper: Primary Current, 2 A / div.
Lower: Resonating Capacitor Voltage,
200 V, 2 ms / div.

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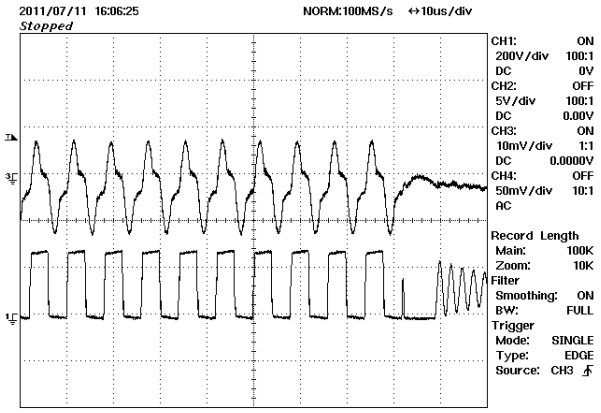

Figure 17 – Output Brown-Out.
Upper: Primary Current, 2 A / div.
Lower: Primary Voltage,
200 V, 10 μs / div.
Minimum Frequency Before Shutdown
~125 kHz.

12.4 Output Diode Peak Reverse Voltage

The following waveforms were measured at full load and 380/420 VDC input.

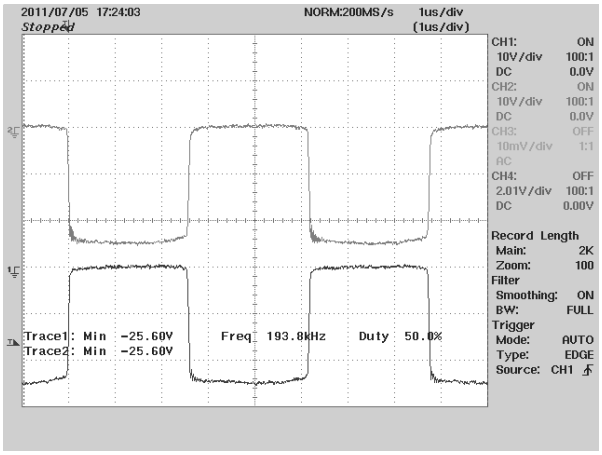

Figure 18 – 12 V Output Diode Peak Reverse Voltage, 380 VDC Input, 10 V, 1 μs / div.

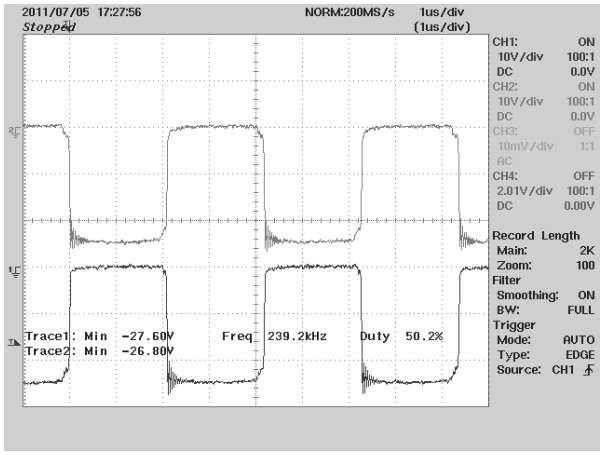

Figure 19 – 12 V Output Diode Peak Reverse Voltage, 420 VDC Input, 10 V, 1 μs / div.

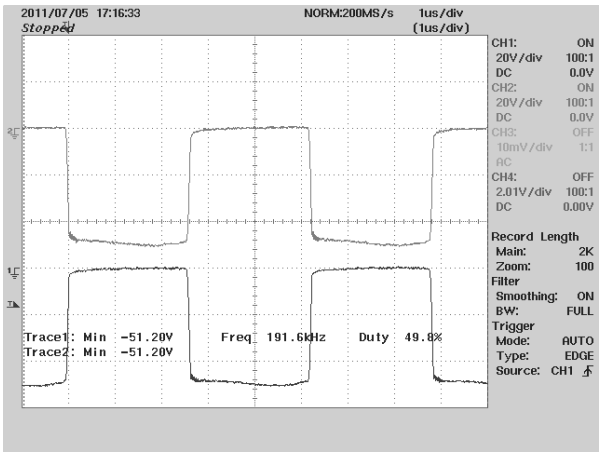

Figure 20 – 24 V Output Diode Peak Reverse Voltage, 380 VDC Input, 20 V, 1 μs / div.

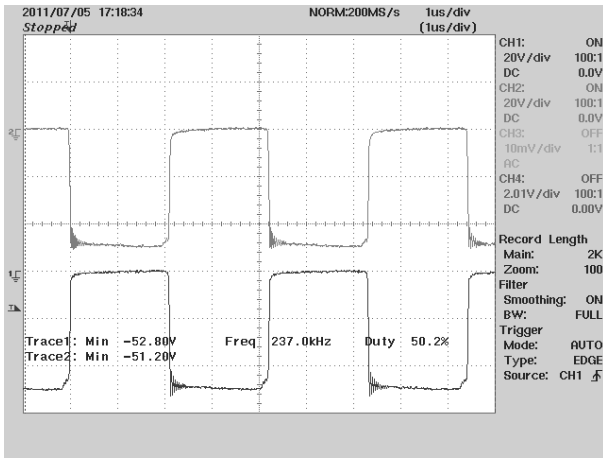

Figure 21 – Output Diode Peak Reverse Voltage, 420 VDC Input, 20 V, 1 μs / div.

12.5 Short-Circuit

For tests shown below, the supply output was shorted with a mercury displacement relay at 125 W load, 380 VDC input. The oscilloscope was set to trigger on current rise.

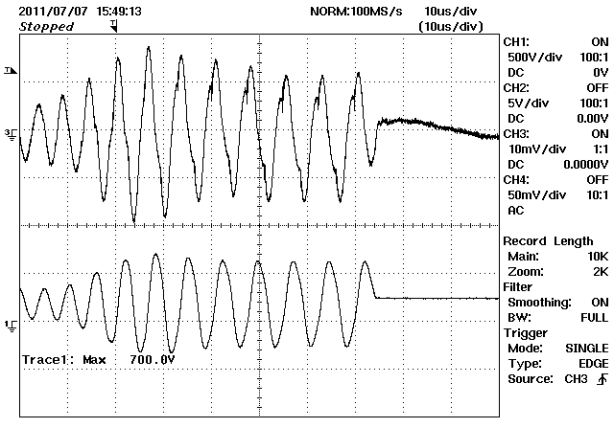

Figure 22 – Primary Waveforms During 12 V Output Short-Circuit.
Upper: Primary Current, 2 A / div.
Lower: Resonating Capacitor Voltage,
500 V, 10 μs / div.

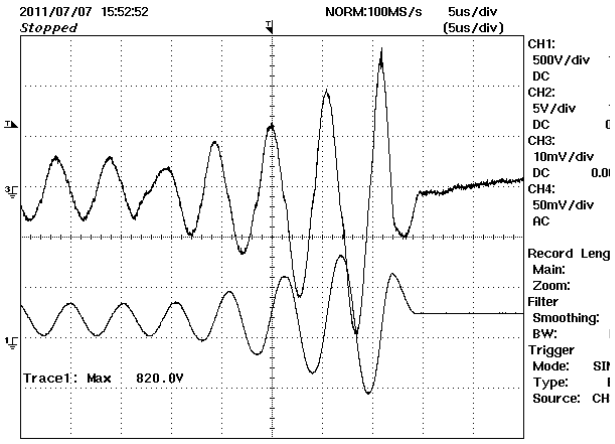

Figure 23 – Primary Waveforms During 24 V Output Short-Circuit.
Upper: Primary Current, 2 A / div.
Lower: Resonating Capacitor Voltage,
500 V, 5 μs / div.

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12.6 Output Ripple Measurements

12.6.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 1.0 μF/50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

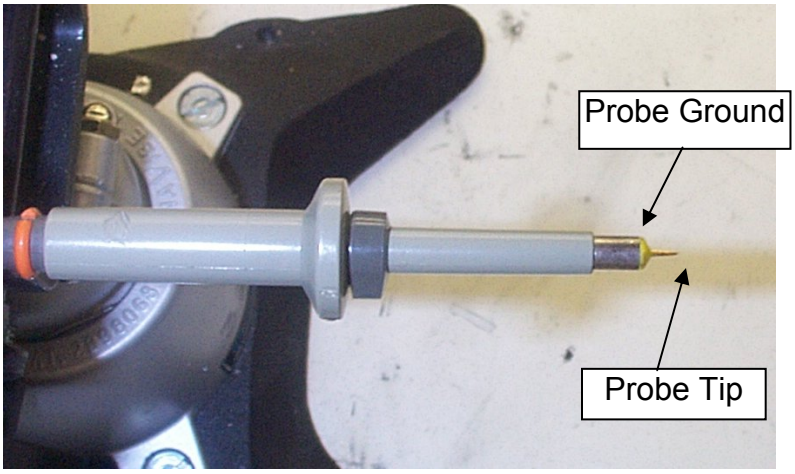

Figure 24 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

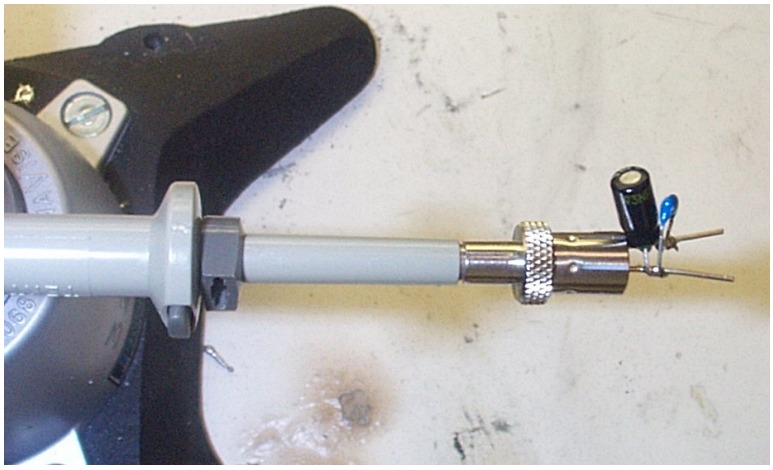

Figure 25 – Oscilloscope Probe with Probe Master (www.probemaster.com) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

12.6.2 Output Ripple Measurement Results

The Figures below show the output behavior with both outputs unloaded, a condition that will not normally occur in the application. With zero load on both outputs, the supply runs in burst mode to stay in regulation. The burst mode in the LCS device is optimized for this purpose, and cannot be relied on for low no-load power consumption, as the supply may not enter burst mode at no-load and nominal input voltage when optimized for efficiency.

The initial spike at the beginning of each burst period is due to the primary resonating capacitor discharging in the slack time between burst cycles. This spike happens with any LLC converter operating in burst mode. The 12 V voltage spike as shown in Figure 28 can be reduced if necessary by using a filter capacitor (C16) that has lower ESR.

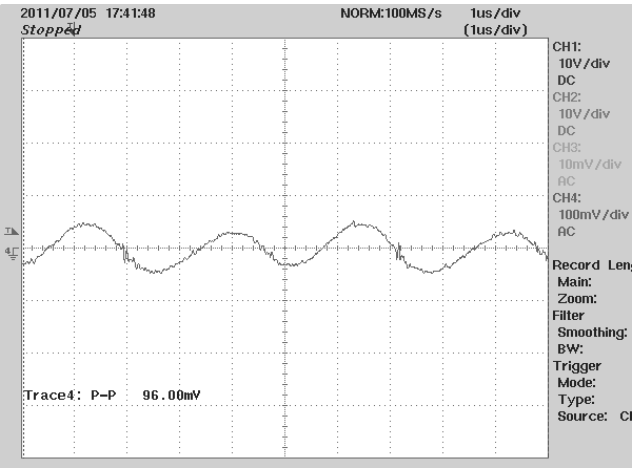

Figure 26 – 12 V Ripple, 380 VDC Input, 100% Load. Output Ripple Voltage, 100 mV / div. 1 μs / div.

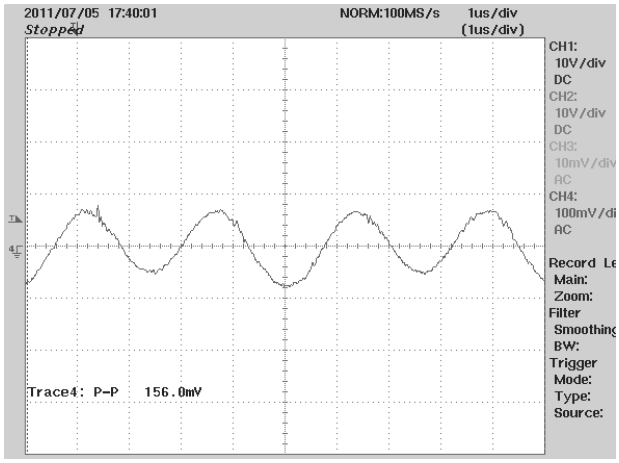

Figure 27 – 24 V Ripple, 380 VDC Input, 100% Load. Output Ripple Voltage, 100 mV / div. 1 μs / div.

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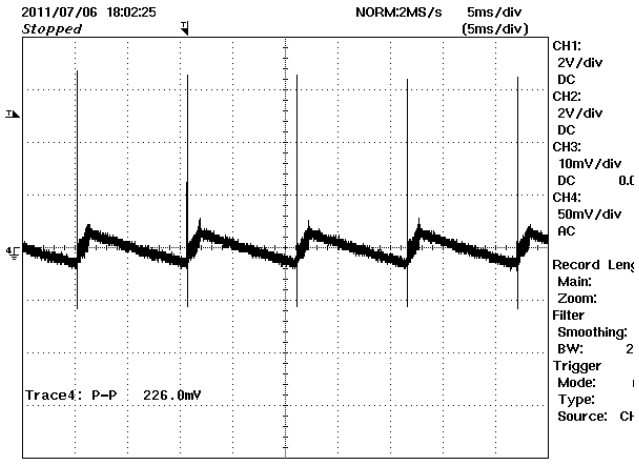

Figure 28 – 12 V Output Ripple Voltage, Both Outputs at Zero Load, 50 mV / div., 5 ms / div. Power Supply is in Burst Mode.

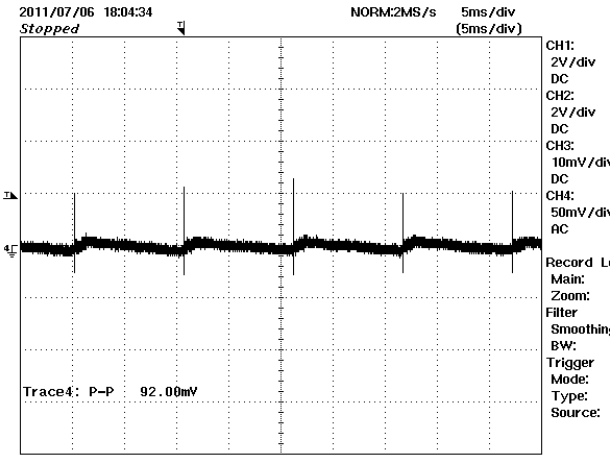

Figure 29 – 24 V Output Ripple Voltage, Both Outputs at Zero Load, 50 mV / div., 5 ms / div. Power Supply is in Burst Mode.

12.7 Output Load Step Response

For the Figures below, the measuring oscilloscope was set to averaging mode, and triggered on the rising edge of the output current step. This averaged out the output ripple, which otherwise would have obscured the transient response.

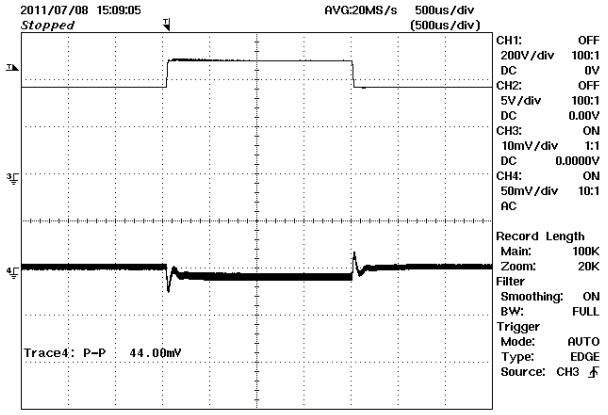

Figure 30 – 12 V Output Load Step Response.
75% to 100% to 75% Load Step on 12 V Output.
Upper: 12 V Load Current, 2 A / div.
Lower: 12 V Output Response, 50 mV, 500 μs / div.

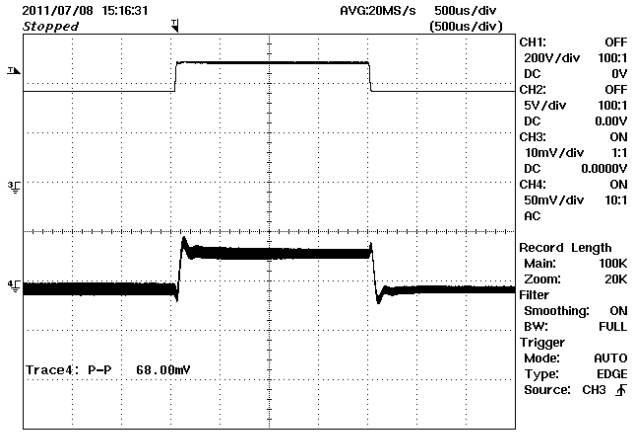

Figure 31 – 24 V Output Load Step Response.
75% to 100% to 75% Load Step on 12 V Output.
Upper: 12 V Load Current, 2 A / div.
Lower: 24 V Output Response, 500 mV, 500 μs / div.

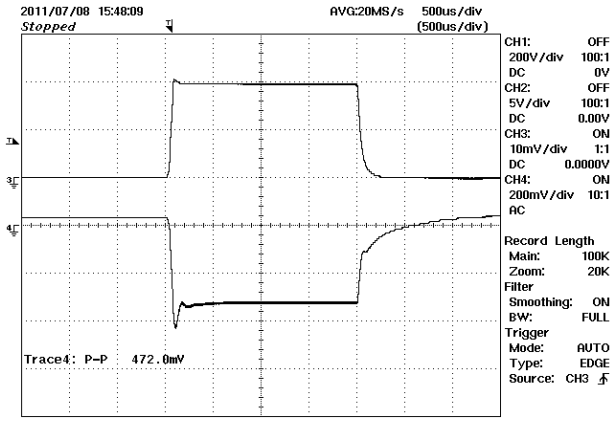

Figure 32 – 24 V Output Load Step Response.
1% to 100% to 1% Load Step on 24 V Output.
Upper: 24 V Load Current, 2 A / div.
Bottom: 24 V Output Response, 200 mV, 500 μs / div.

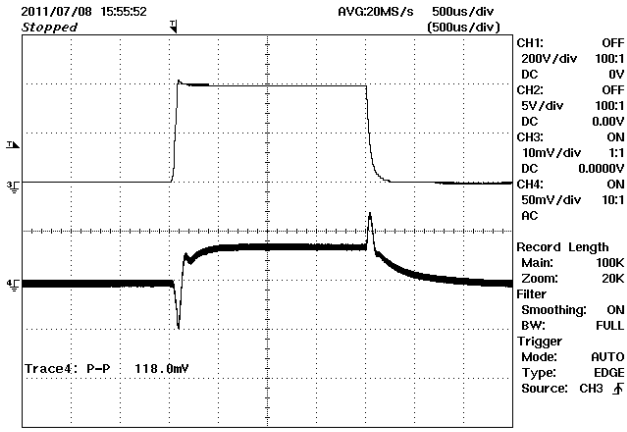

Figure 33 – 12 V Output Load Step Response.
1% to 100% to 1% Load Step on 24 V Output.
Upper: 24 V Load Current, 2 A / div.
Lower: 12 V Output Response, 50 mV, 500 μs / div.

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13 Temperature Measurements

13.1 Conditions: 380 VDC, Full Load, 1 Hour Soak.

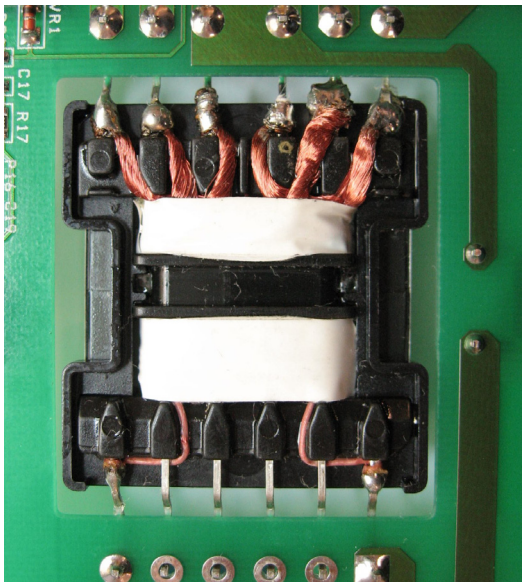

Figure 34 – Transformer (T1).
Visible Light Bottom View.

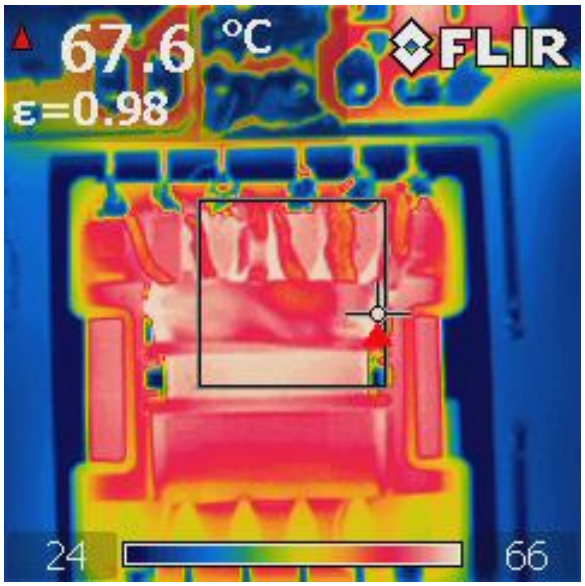

Figure 34 – Transformer (T1).
Thermal Bottom View, Full Load, Room Temperature.

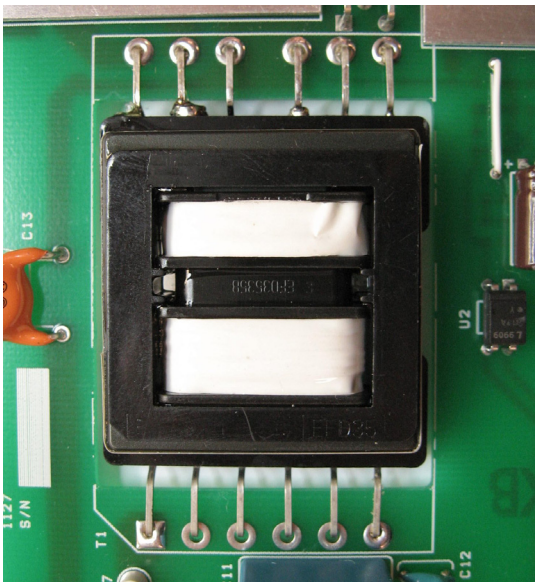

Figure 36 – Transformer (T1).
Visible Light Top View.

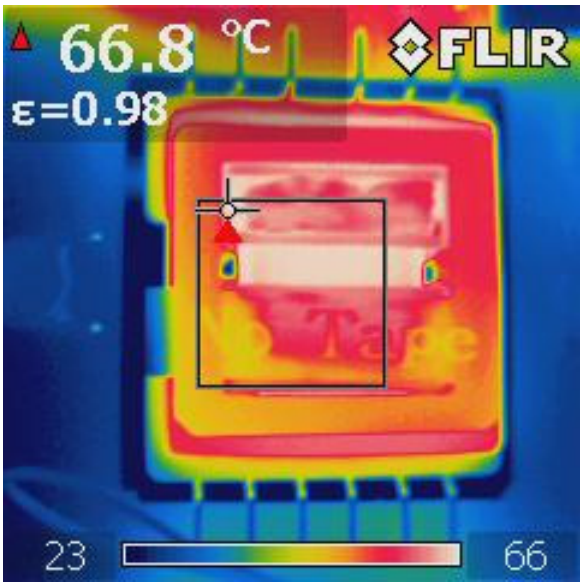

Figure 37 – Transformer (T1).
Thermal Top View, Full Load, Room Temperature.

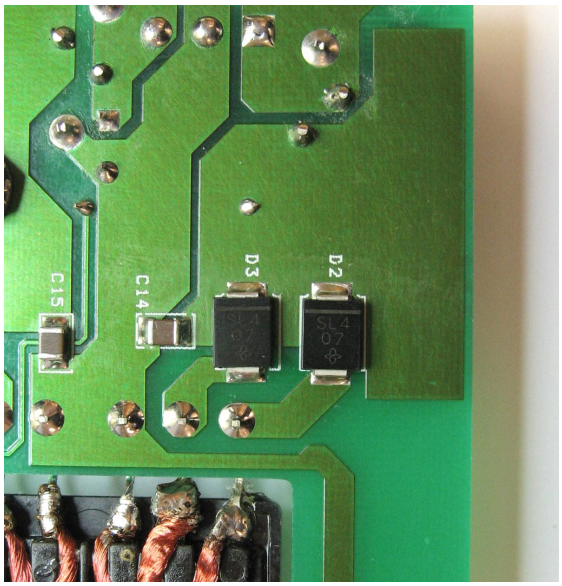

Figure 38 – 12 V Output Rectifiers (D2-D3). Visible Light View.

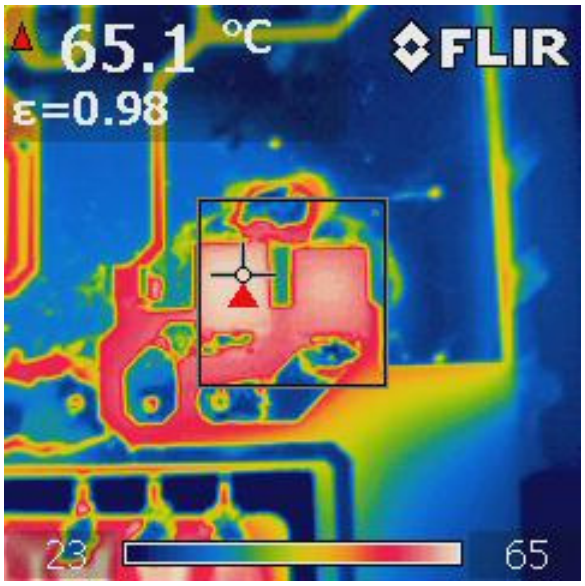

Figure 39 – 12 V Output Rectifiers (D2-D3). Full Load Thermal View, Room Temperature.

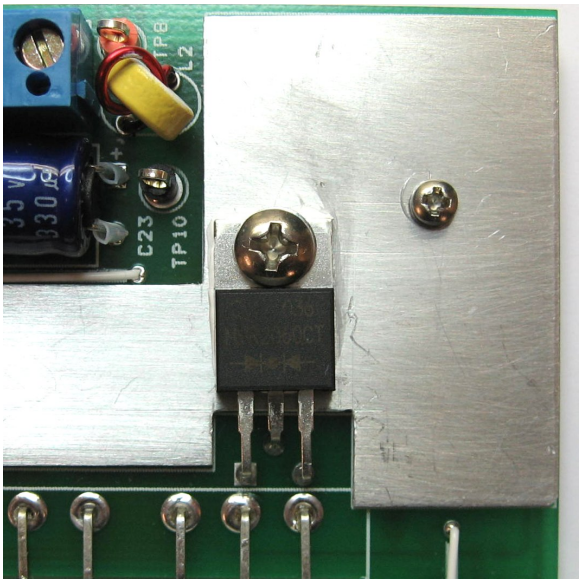

Figure 40 – 24 V Output Rectifier (D4). Visible Light View.

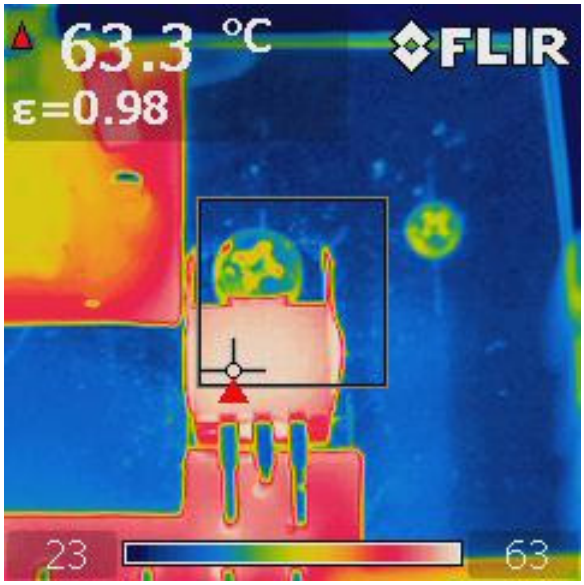

Figure 41 – 24 V Output Rectifier (D4). Full Load, Thermal View, Room Temperature.

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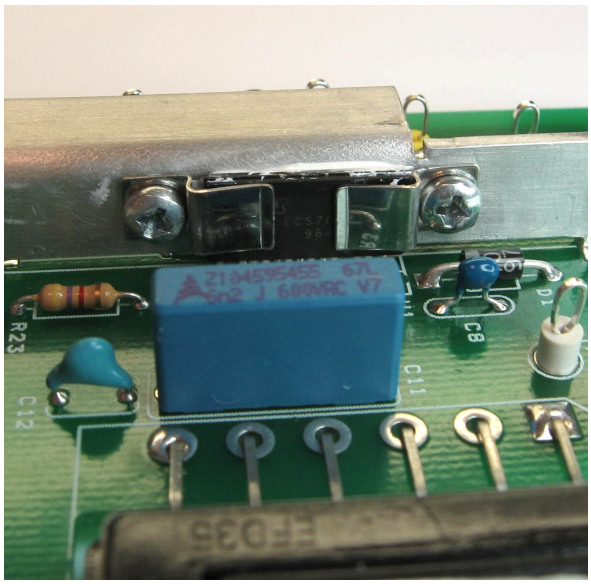

Figure 42 – HiperLCS (U1).
Visible Light View.

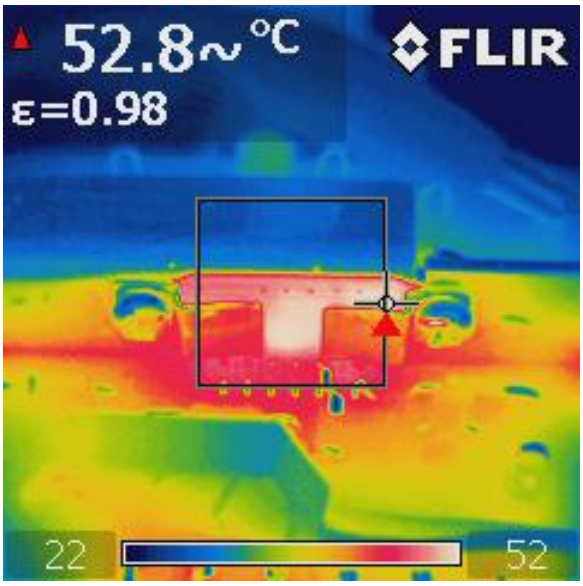

Figure 43 – Full Load HiperLCS (U1).
Thermal View, Room Temperature.

14 Gain-Phase Measurement

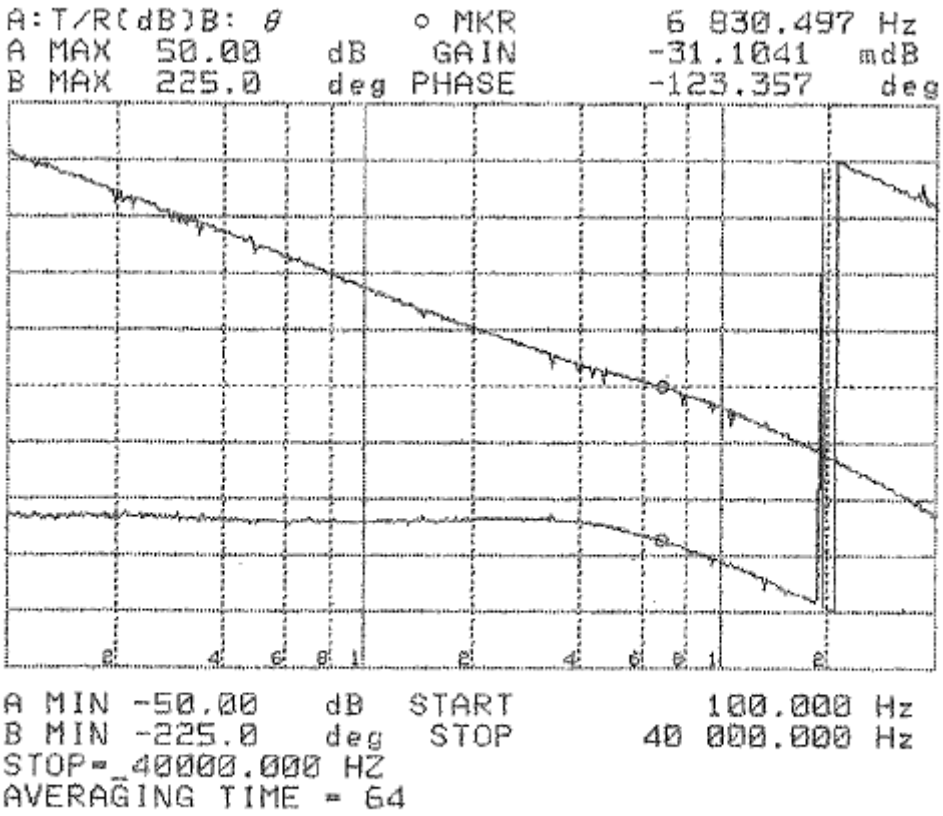

Figure 44 – Gain-Phase Response, Full Load, 380 VDC Input. Gain Crossover Frequency is 6.8 kHz, Phase Margin is 57 Degrees.

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15 Revision History

Date	Author	Revision	Description and Changes	Reviewed
13-Sep-11	RH	1.0	Initial Release	Apps & Mktg

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