Power MOSFET
Electrical Characteristics

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  - $dv/dt$ Capability of the Body Diode
## Static Characteristics

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Unit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate leakage current</td>
<td>$I_{GSS}$</td>
<td>μA</td>
<td>The leakage current that occurs when the specified voltage is applied across gate and source with drain and source short-circuited</td>
</tr>
<tr>
<td>Drain cut-off current</td>
<td>$I_{DSS}$</td>
<td>μA</td>
<td>The leakage current that occurs when a voltage is applied across drain and source with gate and source short-circuited</td>
</tr>
<tr>
<td>Drain-source breakdown voltage</td>
<td>$V_{(BR)DSS}$</td>
<td>V</td>
<td>The maximum voltage that the device is guaranteed to block between drain and source</td>
</tr>
<tr>
<td></td>
<td>$V_{(BR)DSX}$</td>
<td>V</td>
<td>$V_{(BR)DSS}$: With gate and source short-circuited</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$V_{(BR)DSX}$: With gate and source reverse-biased</td>
</tr>
<tr>
<td>Gate threshold voltage</td>
<td>$V_{th}$</td>
<td>V</td>
<td>$V_{th}$ stands for &quot;threshold voltage.&quot; $V_{th}$ is the gate voltage that appears when the specified current flows between source and drain.</td>
</tr>
<tr>
<td>Drain-source on-resistance</td>
<td>$R_{DS (ON)}$</td>
<td>Ω</td>
<td>The resistance across drain and source when the MOSFET is in the &quot;on&quot; state</td>
</tr>
<tr>
<td>Forward transfer admittance</td>
<td>$</td>
<td>Y_{fs}</td>
<td>$</td>
</tr>
</tbody>
</table>
## Dynamic Characteristics

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
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</tr>
</thead>
<tbody>
<tr>
<td>Capacitances</td>
<td>$C_{iss}$ $C_{rss}$ $C_{oss}$</td>
<td>pF</td>
<td>$C_{iss}$ is the input capacitance, $C_{rss}$ is the reverse transfer capacitance, and $C_{oss}$ is the output capacitance. Capacitances affect the switching performance of a power MOSFET.</td>
</tr>
<tr>
<td>Effective output capacitance</td>
<td>$C_{o(er)}$</td>
<td>pF</td>
<td>Effective output capacitance calculated from $E_{ossr}$ which is needed to charge $C_{oss}$</td>
</tr>
<tr>
<td>Gate resistance</td>
<td>$r_g$</td>
<td>Ω</td>
<td>The internal gate resistance of a MOSFET</td>
</tr>
<tr>
<td>Switching time</td>
<td>$t_r$ $t_{on}$ $t_f$ $t_{off}$</td>
<td>ns</td>
<td>$t_r$ is the rise time, $t_{on}$ is the turn-on time, $t_f$ is the fall time, and $t_{off}$ is the turn-off time.</td>
</tr>
<tr>
<td>MOSFET dv/dt capability</td>
<td>dv/dt</td>
<td>V/ns</td>
<td>The resistance across drain and source when the MOSFET is in the &quot;on&quot; state</td>
</tr>
</tbody>
</table>
Capacitance characteristics

- A power MOSFET, the gate is insulated by a thin silicon oxide.
- **Capacitances**
  - Gate-Drain
    - gate-drain capacitance $C_{gd}$
    - The structure of the gate electrode
  - Gate-Source
    - gate-source capacitance $C_{gs}$
    - The structure of the gate electrode
  - Drain-Source terminal
    - drain-source capacitance $C_{ds}$
    - vertical p-n junction.
Capacitance characteristics

- **Input capacitance**
  \[ C_{iss} = C_{gd} + C_{gs} \]

- **Output capacitance**
  \[ C_{oss} = C_{ds} + C_{gd} \]

- **Reverse transfer capacitance**
  \[ C_{rss} = C_{gd} \]
Effective output capacitance

- $C_{o(er)}$ is the effective output capacitance

$$\frac{C_{o(er)} \times V_{DS}^2}{2} = \int_0^{V_{DS}} C(v) \times vdv$$

$$C_{o(er)} = \frac{2}{V_{DS}^2} \int_0^{V_{DS}} C(v) \times vdv$$

- $C(v)$ is a function of the VDS-dependent output capacitance $Coss$.

- Super-junction MOSFETs have a large output capacitance
- Switching loss occurs at the turn-on and turn-off of the MOSFET due to the charging and discharging of the output capacitance
Switching characteristics

- Power MOSFETs are majority-carrier devices
- Faster and capable of switching at higher frequencies
Switching Time

- $t_{d(\text{on})}$: Turn-on delay time
  - gate-source voltage rises over 10% of $V_{GS}$ until the drain-source voltage reaches 90% of $V_{DS}$

- $t_r$: Rise time
  - drain-source voltage to fall from 90% to 10% of $V_{DS}$

- $t_{\text{on}}$: Turn-on time
  - $t_{d(\text{on})} + t_r$

- $t_{d(\text{off})}$: Turn-off delay time
  - gate-source voltage drops below 90% of $V_{GS}$ until the drain-source voltage reaches 10% of $V_{DS}$

- $t_f$: Fall time
  - drain-source voltage to rise from 10% to 90% of $V_{DS}$

- $t_{\text{off}}$: Turn-off time
  - $t_{d(\text{off})} + t_f$
MOSFET dv/dt capability

- The equivalent circuit for a MOSFET consists of one MOSFET in parallel with a parasitic BJT (bipolar junction transistor)
  - If the BJT turns ON, it cannot be turned off since the gate has no control over it. This phenomenon is known as ‘latchup’, which can lead to device destruction.

- Drain-source voltage is raised sharply with fast switch
  - High dv/dt causes a current i go through Parasitic capacitance C to charge R_b
    - If the voltage drop exceeds the base-emitter forward voltage (VBE) of the parasitic NPN transistor, it is forced into conduction.
## Charge Characteristics

<table>
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<tr>
<td>Total gate charge</td>
<td>$Q_g$</td>
<td>nC</td>
<td>The amount of charge to apply voltage (from zero to designated voltage) to gate</td>
</tr>
<tr>
<td>Gate-source charge 1</td>
<td>$Q_{gs1}$</td>
<td>nC</td>
<td>The amount of charge required for a MOSFET to begin to turn on (before dropping drain-source voltage)</td>
</tr>
<tr>
<td>Gate-drain charge</td>
<td>$Q_{gd}$</td>
<td>nC</td>
<td>As the MOSFET begins to turn on, the drain-source voltage begins to fall, charging the gate-drain capacitance. The gate-source voltage stops increasing and reaches the Miller plateau. From this point to the ending point of Miller plateau is known as the gate-drain charge period.</td>
</tr>
<tr>
<td>Gate switch charge</td>
<td>$Q_{sw}$</td>
<td>nC</td>
<td>The amount of charge stored in the gate capacitance from when the gate-source voltage has reached $V_{th}$ until the end of the Miller plateau</td>
</tr>
<tr>
<td>Output charge</td>
<td>$Q_{oss}$</td>
<td>nC</td>
<td>Drain-source charge</td>
</tr>
</tbody>
</table>
Gate charge

- A power MOSFET turn on, a current flows to the gate, charging the gate-source and gate-drain capacitances.
- The gate charge ($Q_{gs} + Q_{gd}$) is the bare minimum charge required to switch the device on.
  - $Q_g = C \times V$ and $I_g = C \times \frac{dv}{dt}$, the $Q_g = \text{Time} \times \text{current}$
  - $Q_g = i_g \times t$
# Source-Drain Characteristics

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</tr>
</thead>
<tbody>
<tr>
<td>Reverse drain current (DC)</td>
<td>$I_{DR}$</td>
<td>A</td>
<td>The maximum current that can flow to the body diode of a MOSFET in the forward direction.</td>
</tr>
<tr>
<td>Reverse drain current (pulsed)</td>
<td>$I_{DRP}$</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>Diode forward voltage</td>
<td>$V_{DF}$</td>
<td>V</td>
<td>Drain-source voltage that appears when a current is applied to the body diode of a MOSFET in the forward direction.</td>
</tr>
<tr>
<td>Reverse recovery time</td>
<td>$t_{rr}$</td>
<td>ns</td>
<td>The time $t_{rr}$ and the amount of charge $Q_{rr}$ required for the reverse recovery current to reach zero during the reverse recovery operation of the body diode under the specified test conditions. The peak current during this period is $I_{rr}$.</td>
</tr>
<tr>
<td>Diode reverse recovery charge</td>
<td>$Q_{rr}$</td>
<td>μC</td>
<td></td>
</tr>
<tr>
<td>Diode peak reverse recovery current</td>
<td>$I_{rr}$</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>Diode dv/dt capability</td>
<td>$dv/dt$</td>
<td>V/ns</td>
<td>The maximum voltage ramp allowed during the reverse recovery time of the diode.</td>
</tr>
</tbody>
</table>
Body Diode Characteristics

- MOSFET has a equivalent diode structure between source and drain
- Reverse breakdown voltage is same as drain-source voltage $V_{DSS}$
Peak diode recovery is defined in datasheet with allowed $V_{DS}$ $dv/dt$ capability.

Body diode enters the reverse recovery state and exceeded the peak rate. This causes the drain-source voltage to increase sharply. Gate-source terminals may become higher than the threshold voltage.

- High $dv/dt$ causes a current $i$ go through Parasitic capacitance $C$ to charge $R_b$, causes the parasitic NPN transistor to turn on.
- If the drain-source voltage $V_{DS}$ is high, the parasitic NPN transistor might enter secondary breakdown.
- Diode might suffer a catastrophic failure.