MP6976

High-Frequency, CCM/DCM Flyback Ideal Diode with Integrated 100V/10mΩ MOSFET and No Auxiliary Winding Requirement

DESCRIPTION

The MP6976 is a fast turn-off, intelligent rectifier for flyback converters that integrates a 100V/10mΩ MOSFET. It can replace a diode rectifier for higher efficiency and power density. The chip regulates the internal power MOSFET's forward voltage drop (V_{FWD}) to 40mV [1] and turns off before the drain-to-source voltage (V_{DS}) reverses.

The MP6976 can generate its own supply voltage without the need for auxiliary winding, which makes it suitable for charger applications with a low output voltage (V_{OUT}), or for high-side (HS) adapter applications. The internal ringing detection circuitry prevents the MP6976 from falsely turning on during discontinuous conduction mode (DCM) or quasi-resonant (QR) operations.

The MP6976 is available in an SOIC-8 package.

FEATURES

- Integrated 100V/10mΩ MOSFET
- Wide Output Voltage (V_{OUT}) Range Down to 0V
- No Need for Auxiliary Winding for High-Side (HS) or Low-Side (LS) Rectification
- Ringing Detection Prevents False Turn-On during Discontinuous Conduction Mode (DCM)
- Compatible with Energy Star
- 110μA Quiescent Current ($I_{Q(VDD)}$)
- Supports DCM, Continuous Conduction Mode (CCM), and Quasi-Resonant (QR) Operation
- Available in an SOIC-8 Package

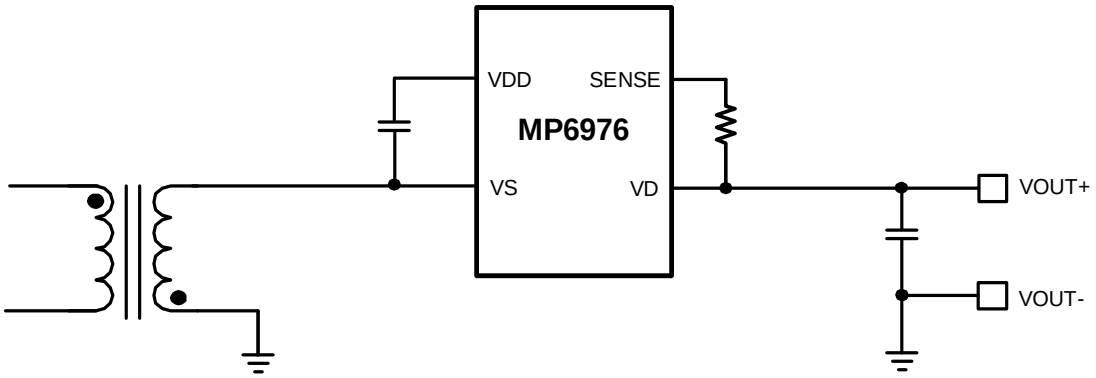
APPLICATIONS

- Laptop Adapters
- QC and USB PD Chargers
- High-Efficiency Flyback Converters

Note:

1) Related issued patent: US Patent US8, 067,973; US8,400,790. CN Patent ZL201010504140.4. Other patents pending.

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number	Package	Top Marking	MSL Rating
MP6976GS*	SOIC-8	*See Below*	2

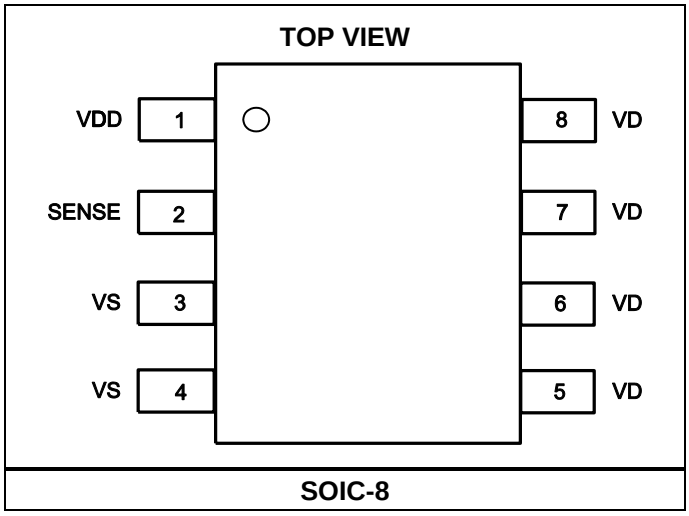
* For Tape & Reel, add suffix -Z (e.g. MP6976GS-Z).

TOP MARKING

MP6976
LLLLLLLL
MPSYWW

MP6976: Part number
LLLLLLLL: Lot number
MPS: MPS prefix
Y: Year code
WW: Week code

PACKAGE REFERENCE



PIN FUNCTIONS

Pin #	Name	Description
1	VDD	**Linear regulator output.** The VDD pin supplies power to the device.
2	SENSE	**MOSFET drain-source voltage sensing.** The SENSE pin senses the MOSFET drain voltage and is also the linear regulator input.
3, 4	VS	**MOSFET source.** The VS pin is the MOSFET's source as well as a reference for VDD.
5, 6, 7, 8	VD	**MOSFET drain.**

ABSOLUTE MAXIMUM RATINGS (2)

VDD to VS .....-0.3V to +14V
VD to VS .....-1.5V to +100V
SENSE to VS .....-1V to +180V
Continuous drain current (T_C = 25°C) 14.9A
Continuous drain current (T_C = 100°C) 9.42A
Pulsed drain current (3) 50A
Maximum power dissipation (4) 1.7W
Single-pulse avalanche energy (5) 200mJ
Junction temperature .....150°C
Lead temperature (solder) .....260°C
Storage temperature ..... -55°C to +150°C

ESD Ratings

Human body model (HBM) ..... ±1200V
Charged device model (CDM) ..... ±2000V

Recommended Operation Conditions (6)

VDD to VS .....4.5V to 13V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (7) θ_{JA} θ_{JC}

SOIC-8..... 70 ..... 32... °C/W

Notes:

2) Exceeding these ratings may damage the device.
3) Repetitive rating: Pulse width = 100µs, duty cycle limited by maximum junction temperature.
4) T_A = 25°C. The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient, temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) – T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
5) E_{AS} is tested starting at T_J = 25°C, L = 1mH, I_{AS} = 20A, V_{DD} = 50V, and V_{GS} = 10V.
6) The device is not guaranteed to function outside of its operating conditions.
7) Measured on JESD51-7, a 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{DD} = 6.7V, T_J = -40°C to about +125°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-to-source breakdown voltage	$V_{(BR)DSS}$	T_J = 25°C, V_{DS} = 100V, VDD and SENSE pins shorted to VS	100			V
V_{DD} under-voltage lockout (UVLO) rising threshold			4	4.2	4.4	V
V_{DD} UVLO hysteresis			0.1	0.24	0.38	V
V_{DD} maximum charging current	I_{VDD}	V_{DD} = 5.5V, SENSE = 30V	35	63	90	mA
Operating current	I_{CC}	f_{SW} = 100kHz		4	6	mA
Quiescent current	$I_{Q(VDD)}$	V_{DD} = 7V		110	135	µA
Control Circuitry						
Forward regulation voltage (V_S - V_D) (8)	V_{FWD}		25	40	55	mV
Turn-on threshold (V_{DS})	V_{DRV_ON}		-115	-80	-57	mV
Turn-off threshold (V_S - V_D) (8)	V_{DRV_OFF}		-6	3	12	mV
Turn-on delay (9)	t_{D_ON}			20		ns
Turn-off delay (8)	t_{D_OFF}			25		ns
Turn-on blanking time	t_{B_ON}		0.75	1.1	1.45	µs
Turn-off blanking threshold (V_{DS})	V_{B_OFF}		2		3	V
Turn-off threshold during minimum on time (V_{DS})				1.8		V
Turn-on slew rate detection time (9)				30		ns
Power MOSFET						
Drain-to-source on resistance	$R_{DS(ON)}$	I_D = 2A, T_J = 25°C		10	13.5	mΩ
Input capacitance	C_{ISS}	V_{DS} = 50V, V_{GS} = 0V, f = 1MHz		1800		pF
Output capacitance	C_{OSS}			530		pF
Reverse transfer capacitance	C_{RSS}			10		pF
Source-to-Drain Diode Characteristics						
Source-to-drain diode forward voltage	V_{SD}	I_S = 8A, V_{GS} = 0V		0.8	1.2	V
Reverse recovery time	t_{RR}	I_F = 20A, dI/dt = 100A/µs		33		ns
Diode reverse charge	Q_{RR}	I_F = 20A, dI/dt = 100A/µs		41		nC

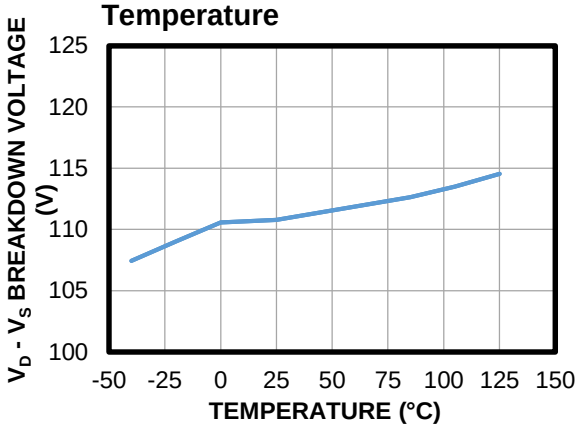
Notes:

8) Guaranteed by characterization.
9) Guaranteed by design.

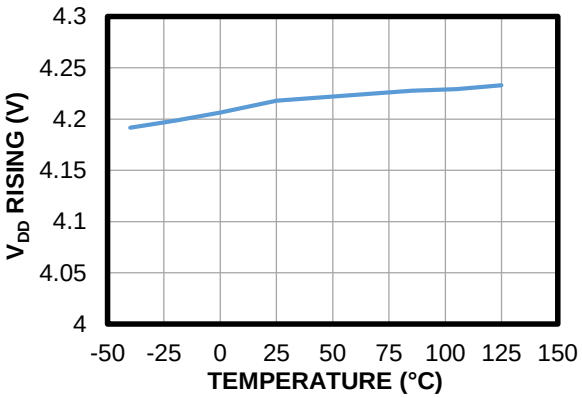
TYPICAL CHARACTERISTICS

V_{DD} = 6.7V, unless otherwise noted.

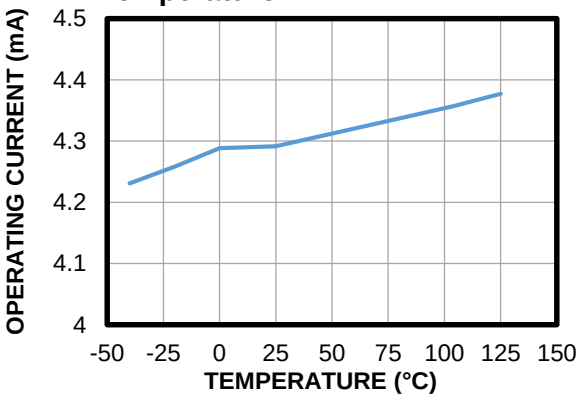
V_D - V_S Breakdown Voltage vs. Temperature



V_{DD} Rising vs. Temperature

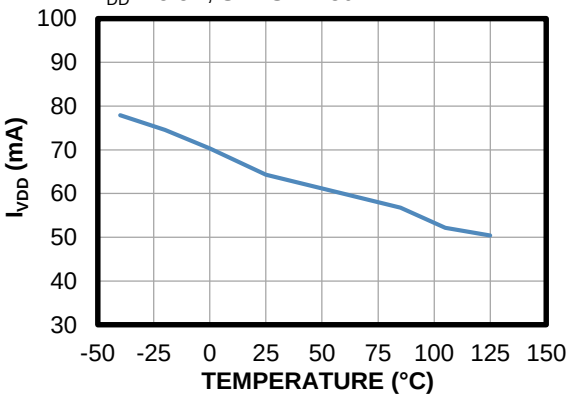


Operating Current vs. Temperature

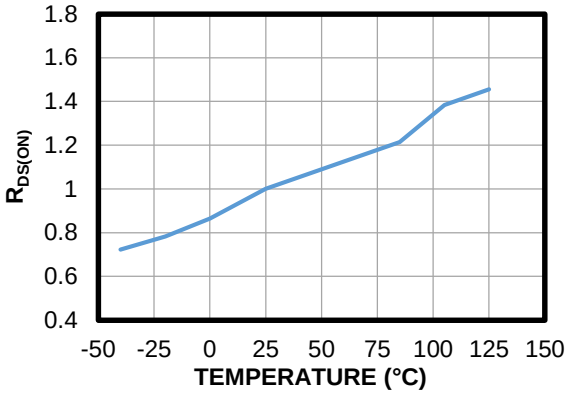


V_{DD} Maximum Charging Current vs. Temperature

V_{DD} = 5.5V, SENSE = 30V



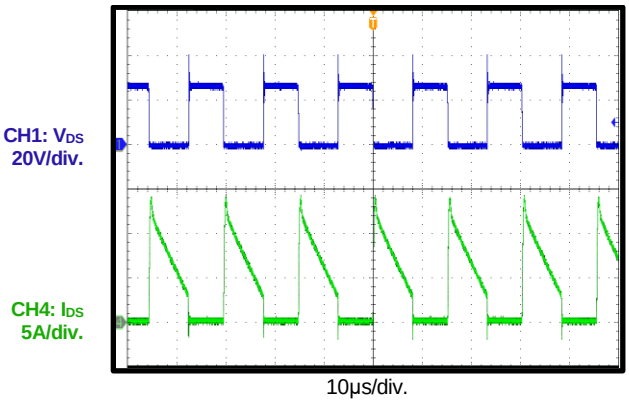
Normalized Drain-to-Source On Resistance vs. Temperature



TYPICAL PERFORMANCE CHARACTERISTICS

Operation in 48W Flyback Application

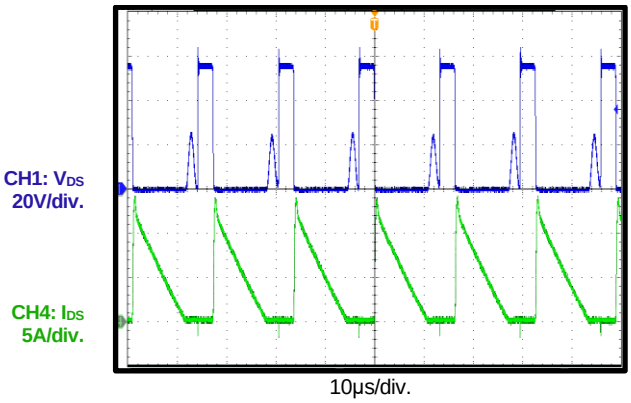
V_{IN} = 90V_{AC}, I_{OUT} = 4A



10µs/div.

Operation in 48W Flyback Application

V_{IN} = 265V_{AC}, I_{OUT} = 4A



10µs/div.

FUNCTIONAL BLOCK DIAGRAM

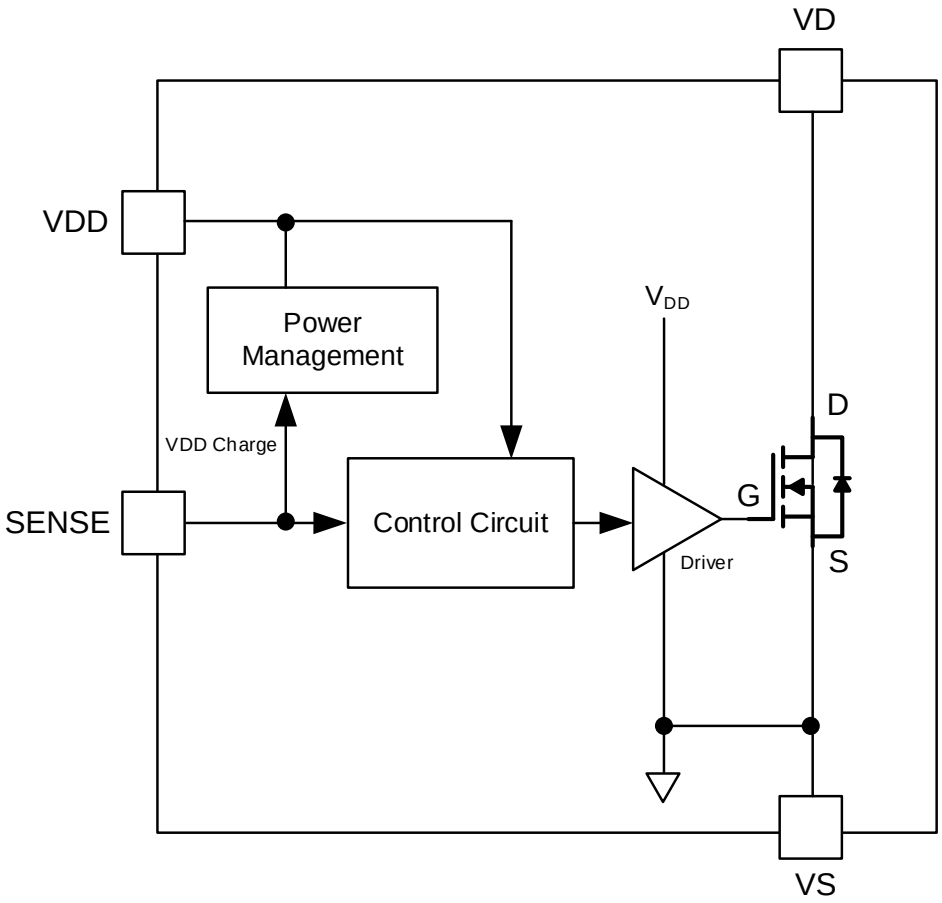


Figure 1: Functional Block Diagram

OPERATION

The MP6976 supports discontinuous conduction mode (DCM), continuous conduction mode (CCM), as well as quasi-resonant (QR) operation in flyback converters. The control circuitry controls the gate in forward mode and turns the gate off when the synchronous rectification (SR) MOSFET current drops to 0A.

VDD Generation

SENSE is the linear regulator's input, and VDD is the regulator's output. The VDD pin supplies power to the MP6976, and is regulated at 6.7V.

If SENSE is below 4.7V, then a 40mA current source from SENSE charges up the VDD voltage (V_{DD}). If SENSE exceeds 4.7V, then the linear regulator's maximum charging current is limited to the V_{DD} maximum charging current (I_{VDD}) to charge the external capacitor at VDD.

Start-Up and Under-Voltage Lockout (UVLO)

When V_{DD} exceeds the V_{DD} under-voltage lockout (UVLO) rising threshold, the MP6976 exits UVLO and is enabled. Once V_{DD} drops below the V_{DD} UVLO falling threshold, the MP6976 enters sleep mode, and the gate driver voltage (V_{GS}) remains low.

Turn-On Phase

When the drain-to-source voltage (V_{DS}) drops to about 2V, a turn-on timer begins. If V_{DS} reaches the turn-on threshold (V_{DRV_ON}) from 2V within the slew rate detection time, then the MOSFET turns on after a turn-on delay (t_{D_ON}) (see Figure 2). If V_{DS} reaches V_{DRV_ON} after the timer ends, then the gate voltage (V_{GS}) remains off. This turn-on timer prevents the MP6976 from falsely turning on due to ringing from DCM or QR operation.

Turn-On Blanking

The control circuitry contains a blanking function. When the MOSFET turns on, the control circuit ensures that the on state lasts for a specific time period. The turn-on blanking time (t_{B_ON}) prevents an accidental turn-off due to ringing. However, if V_{DS} reaches the turn-off threshold within the turn-on blanking time, V_{GS} is pulled low immediately.

Conduction Phase

Once V_{DS} exceeds the forward voltage drop ($-V_{FWD}$) according to the decrease of the switching current, the MP6976 lowers V_{GS} to increase the synchronous MOSFET's on resistance. With this control scheme, V_{DS} is adjusted to be approximately equal to $-V_{FWD}$, even when the current through the MOSFET is fairly low. This function is especially vital for CCM as it keeps V_{GS} low when the synchronous MOSFET turns off, thereby boosting the turn-off speed.

Turn-Off Phase

If V_{DS} rises high enough to trigger the turn-off threshold ($-V_{DRV\_OFF}$), the gate voltage is pulled to 0V after a very short turn-off delay (t_{D_OFF}) (see Figure 2).

Turn-Off Blanking

After V_{GS} is pulled to 0V by V_{DS} reaching $-V_{DRV\_OFF}$, a turn-off blanking time is applied. During this blanking time, the gate driver signal latches off. The turn-off blanking time is removed when V_{DS} exceeds the turn-off blanking threshold (V_{B_OFF}) (see Figure 2).

Figure 2 shows the turn-on and turn-off timing diagram.

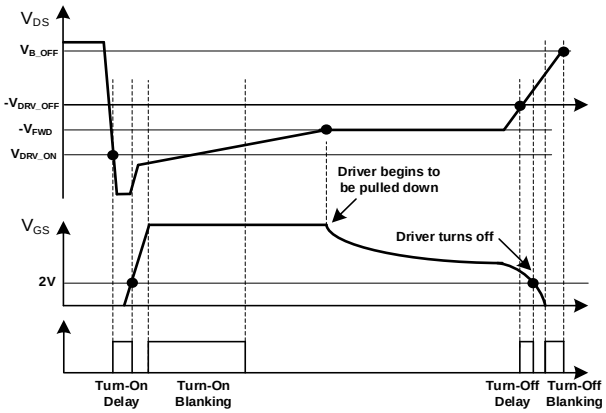


Figure 2: Turn-On/Turn-Off Timing Diagram

APPLICATION INFORMATION

Slew Rate Detection

During DCM, the demagnetizing ringing may bring V_{DS} below 0V. If V_{DS} reaches V_{DRV_ON} during the ringing period, an SR controller without slew rate detection may turn on the MOSFET by mistake. This not only increases power loss, but may also lead to shoot-through if the primary-side MOSFET turns on within the minimum on time.

The ringing slew rate is always significantly lower than it is when the primary MOSFET is completely turned off. A false turn-on can be prevented using slew rate detection. When the slew rate is too small, V_{DS} drops from 2V to V_{DRV_ON} for a period exceeding the slew rate detection time. In this scenario, the IC does not turn on the gate even when V_{DS} reaches V_{DRV_ON} (see the Turn-On Phase section on page 8).

Selecting the External Resistor on SENSE

Over-voltage (OV) conditions can damage the device; therefore, the application design must guarantee safe operation, especially on the high-voltage pin.

One common OV condition occurs when the SR MOSFET's body diode turns on. In this scenario, the SENSE pin's voltage drop may exceed the negative rating.

It is recommended to place an external resistor between SENSE and the MOSFET drain. The resistance is typically recommended to be between 100Ω and 300Ω. This value varies on a case-by-case basis. Note that a higher-value resistor may compromise the VDD supply and slow down the slew rate for V_{DS} detection.

Typical System Implementations

Figure 3 shows the typical system IC implementation for low-side (LS) rectification.

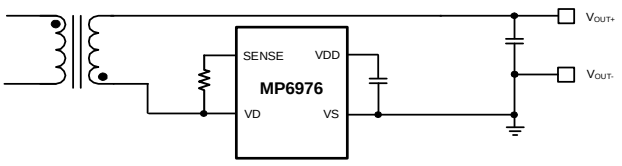


Figure 3: Low-Side Rectification

Figure 4 shows the typical system IC implementation for high-side (HS) rectification.

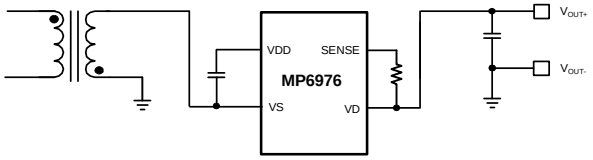


Figure 4: High-Side Rectification

Setting the Maximum Output Current

The MP6976's temperature rise threshold limits the maximum output current (I_{OUT}) that the device can handle. The temperature rise is determined by the device's power loss. For a universal input adapter, the MP6976's recommended rated I_{OUT} is about 3A. For certain designs, the MP6976's power loss can be calculated, so the maximum I_{OUT} can be calculated as well.

The MP6976's power loss can be calculated based on different causes, including controller consumption and integrated MOSFET conduction loss. If the MP6976 operates in CCM, the integrated MOSFET's reverse-recovery loss must also be considered. The controller power loss ($P_{LOSS\_CONTROLLER}$) can be calculated using Equation (1):

$$P_{LOSS\_CONTROLLER} = V_{SENSE\_P} \times I_{DD} \quad (1)$$

Where I_{DD} is the MP6976's current, and V_{SENSE_P} is the corresponding plateau voltage in SENSE when the SR turns off.

The SR conduction power loss ($P_{LOSS\_SR\_CONDUCTION}$) can be estimated using Equation (2):

$$P_{LOSS\_SR\_CONDUCTION} = f_{sw} \times \int_{0}^{t_{S\_ON}} V_{SR\_SD}(t) \times I_{SR\_SD}(t)\,dt \quad (2)$$

Where f_{SW} is the SR switching frequency, t_{S_ON} is the SR on period, V_{SR_SD} is the voltage drop from the SR, and I_{SR_SD} is the current flowing from the SR.

The SR reverse-recovery power loss ($P_{LOSS\_SR\_RR}$) can be calculated using Equation (3):

$$P_{LOSS\_SR\_RR} = \frac{1}{2} \times V_{DS} \times I_{RR} \times t_F \times f_{SW} \quad (3)$$

Where I_{RR} is the peak reverse current, and t_F is the reverse current fall time.

The device's total power loss (P_{LOSS}) is the sum of the above losses. If an RC snubber is used, the power loss caused by this snubber must also be taken into consideration.

The junction and case temperature rises can be calculated using the junction-to-ambient thermal resistance (θ_{JA}) and junction-to-case thermal resistance (θ_{JC}). The junction temperature must be within the absolute maximum rating (typically 150°C). ΔT_{JA} can be calculated using Equation (4):

$$\Delta T_{JA} = P_{LOSS} \times \theta_{JA} \quad (4)$$

ΔT_{JC} can be calculated using Equation (5):

$$\Delta T_{JC} = P_{LOSS} \times \theta_{JC} \quad (5)$$

To lower the temperature, the thermal resistance can be reduced using the following methods:

1. Connect a thicker copper layer to VD and VS.
2. Add additional vias to the PCB for thermal dissipation.
3. Add heatsinks for thermal dissipation.

The real maximum I_{OUT} can be set by combining the real tested data.

Design Example

Figure 5 shows a layout example for a HS application of a flyback power supply, which is a single layer with a through-hole transformer. R2 and C2 comprise the internal MOSFET's RC snubber network. The sensing loop (SENSE to the MOSFET drain) is optimized and kept separate from the power loop. The VDD decoupling capacitor (C1) is placed beside VDD.

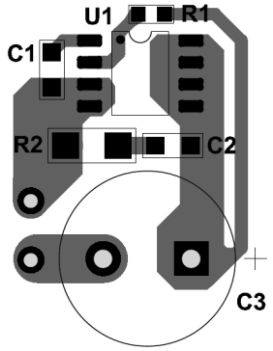


Figure 5: Layout Example in a Flyback High-Side Application

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 5 on page 10 and Figure 6, and follow the guidelines below:

1. Connect the SENSE pin to different positions for an adjustable turn-off time during the fast transients in CCM. In general, the further the junction point is from VD, the earlier the SR turns off (see Figure 6).

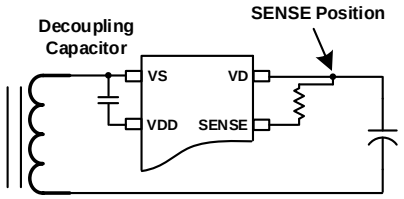


Figure 6: Voltage Sensing for VD/SENSE

2. Keep the IC out of the power loop to prevent the sensing loop and power loop from interrupting each other.
3. Place a decoupling ceramic capacitor from VDD to VS, close to the IC, for adequate filtering.

TYPICAL APPLICATION CIRCUIT

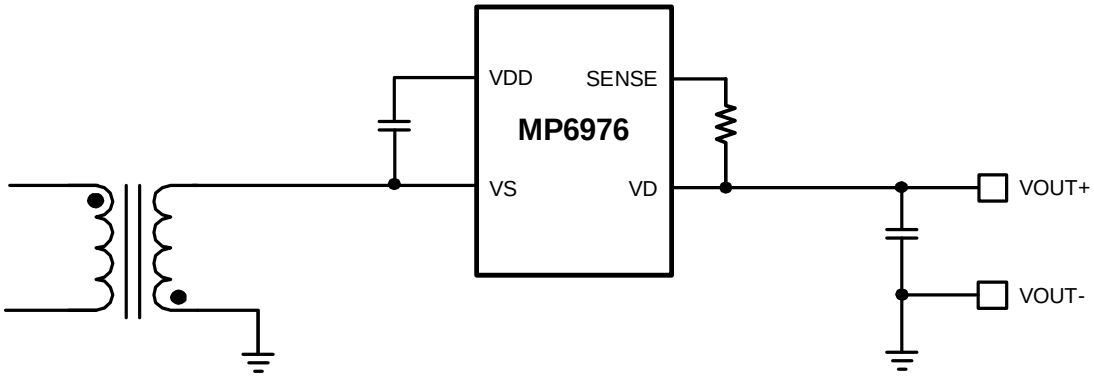
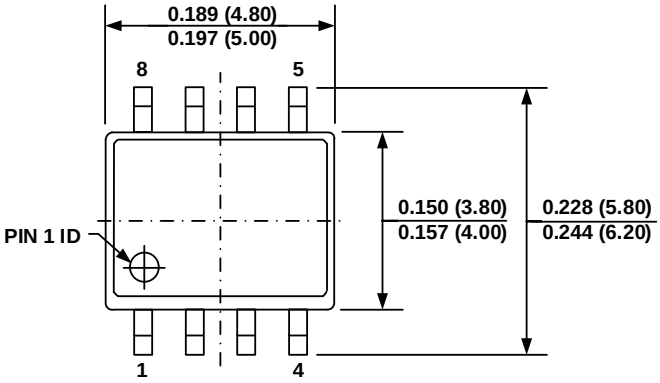


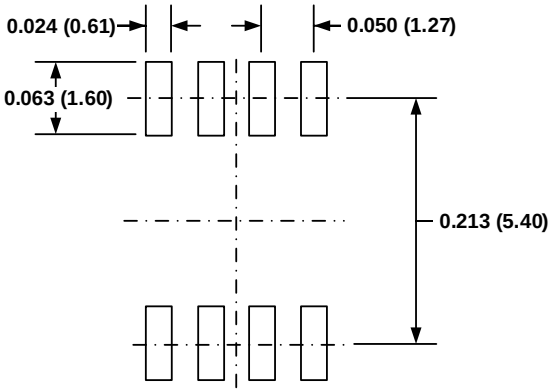
Figure 7: Typical Application Circuit

PACKAGE INFORMATION

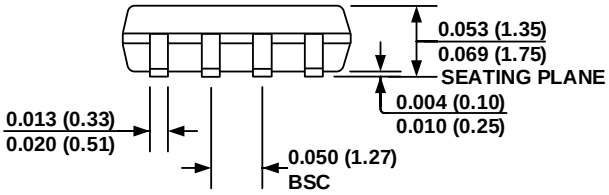
SOIC-8



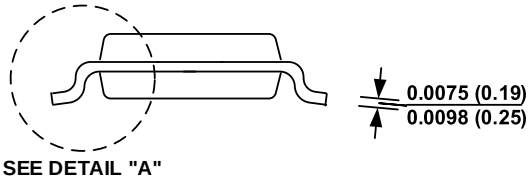
TOP VIEW



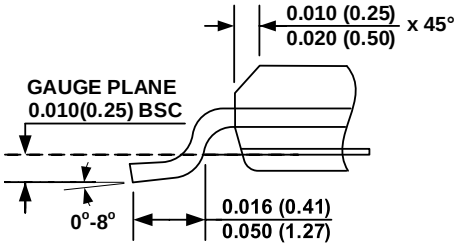
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW

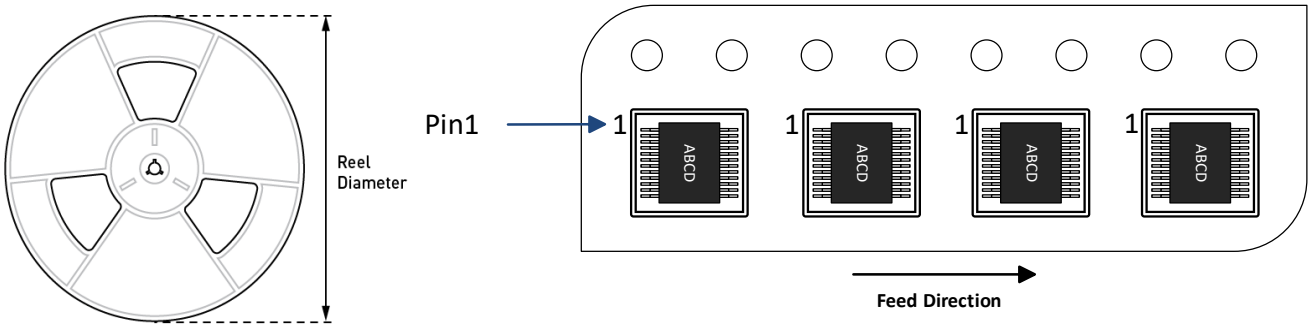


DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSIONS IN BRACKET ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6976GS-Z	SOIC-8	2500	100	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	7/13/2022	Initial Release	-