



FEATURES

The MP6972 is available in an SOIC-8 package.

- Integrated 100V/17mΩ MOSFET
- Optimized Efficiency for Low-Side Rectification
- Ringing Detection Prevents False Turn-On during DCM Operations
- Compatible with Energy Star
- 110μA Quiescent Current
- Supports DCM, CCM, and Quasi-Resonant Operations
- Wide Output Range Down to 0V
- Available in an SOIC-8 Package

- Laptop Adapters
- QC and USB PD Chargers
- High-Efficiency Flyback Converters

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ORDERING INFORMATION

Part Number	Package	Top Marking	MSL Rating
MP6972GS*	SOIC-8	See Below	2

* For Tape & Reel, add suffix -Z (e.g. MP6972GS-Z).

TOP MARKING

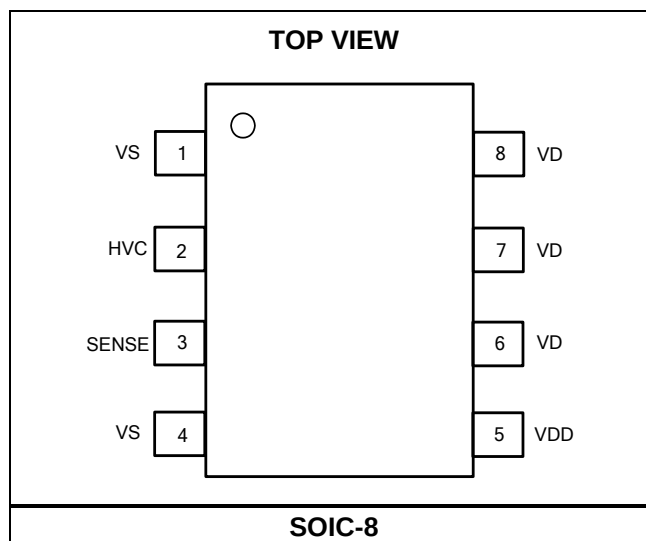
MP6972

LLLLLLLL

MPSYWW

MP6972: Part number
 LLLLLLLL: Lot number
 MPS: MPS prefix
 Y: Year code
 WW: Week code

PACKAGE REFERENCE



PIN FUNCTIONS

Pin #	Name	Description
1, 4	VS	MOSFET source. VS is also used as a reference for VDD.
2	HVC	HV linear regulator input.
3	SENSE	MOSFET drain voltage sensing.
5	VDD	Linear regulator output. VDD is the power supply of IC.
6, 7, 8	VD	MOSFET drain.

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

VDD to VS	-0.3V to +14V
VD to VS	-1.5V to +100V
SENSE, HVC to VS	-1V to +180V
Continuous drain current (T _C = 25°C)	12.8A
Continuous drain current (T _C = 100°C)	8.1A
Pulsed drain current ⁽²⁾	50A
Maximum power dissipation ⁽³⁾	1.8W
Junction temperature	150°C
Lead temperature (solder)	260°C
Storage temperature	-55°C to +150°C

ESD Rating

Charged device model (CDM) ±2000V

Recommended Operation Conditions ⁽⁴⁾

VDD to VS	4.5V to 13V
Operating junction temp (T _J)	-40°C to +125°C

Thermal Resistance ⁽⁵⁾	θ_{JA}	θ_{JC}
SOIC-8.....	67	30... °C/W

Notes:

- 1) Exceeding these ratings may damage the device.
- 2) Repetitive rating: Pulse width = 100μs, duty cycle limited by maximum junction temperature.
- 3) T_A = 25°C. The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA} , and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA} . Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 4) The device is not guaranteed to function outside of its operating conditions.
- 5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

VDD = VDD_HVC, TJ = -40°C to +125°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
VDD regulation voltage	V _{DD_SEN}	SENSE = 30V, HVC = 0V	4.6	5	5.4	V
	V _{DD_HVC}	SENSE = 0V, HVC = 12V	6.3	6.7	7	V
VDD UVLO rising			4.0	4.2	4.4	V
VDD UVLO hysteresis			0.1	0.24	0.38	V
VDD charging current	I _{VDD_SEN}	VDD = V _{DD_SEN} - 0.1V, SENSE = 30V, HVC = 0V, C _{DD} = 1μF	20	38	55	mA
	I _{VDD_HVC}	VDD = V _{DD_HVC} - 0.1V, SENSE = 0V, HVC = 12V, C _{DD} = 1μF	20	38	62	mA
		VDD = V _{DD_HVC} - 0.1V, SENSE = 0V, HVC = 30V, C _{DD} = 1μF	35	64	95	mA
Operating current	I _{CC}	f _{SW} = 100kHz	1.6	2.4	4	mA
Quiescent current	I _{Q(VDD)}	V _{DD} = 7V		110	135	μA
Control Circuitry Section						
Forward regulation voltage (VS-VD) ⁽⁶⁾	V _{FWD}		25	40	55	mV
Turn-on threshold (VDS)			-115	-80	-57	mV
Turn-off threshold (VS-VD) ⁽⁶⁾			-6	3	+12	mV
Turn-on delay ⁽⁷⁾	t _{D_ON}			20		ns
Turn-off delay ⁽⁶⁾	t _{D_OFF}			25		ns
Turn-on blanking time	t _{B-ON}		0.8	1.2	1.55	μs
Turn-off blanking threshold (VDS)	V _{B-OFF}		2	2.5	3	V
Turn-off threshold during minimum on time (VDS)			1.2	1.8	2.5	V
Turn-on slew rate detection time ⁽⁷⁾				30		ns
Power Switch Section ⁽⁸⁾						
Drain-source breakdown voltage ⁽⁶⁾	V _{(BR)DSS}		100			V
Single-pulse avalanche energy ⁽⁶⁾	E _{AS}	V _{PS} = 50V, V _{GS} = 0V, L = 1.0mH,		100		mJ
Drain-source on resistance	R _{DS(ON)}	V _{GS} = 6.7V, I _D = 2A		17	21.3	mΩ
Input capacitance ⁽⁷⁾	C _{ISS}	V _{DS} = 40V, V _{GS} = 0V, f = 1MHz		1925		pF
Output capacitance ⁽⁷⁾	C _{OSS}			307		pF
Reverse transfer capacitance ⁽⁷⁾	C _{RSS}			20		pF
Source-Drain Diode Characteristics						
Source-drain diode forward voltage	V _{SD}	I _S = 8A, V _{GS} = 0V		0.8	1.2	V
Reverse recovery time ⁽⁷⁾	t _{RR}	I _F = 10A, dI/dt = 100A/μs		78.8		ns
Diode reverse charge ⁽⁷⁾	Q _{RR}			105.6		nC

Notes:

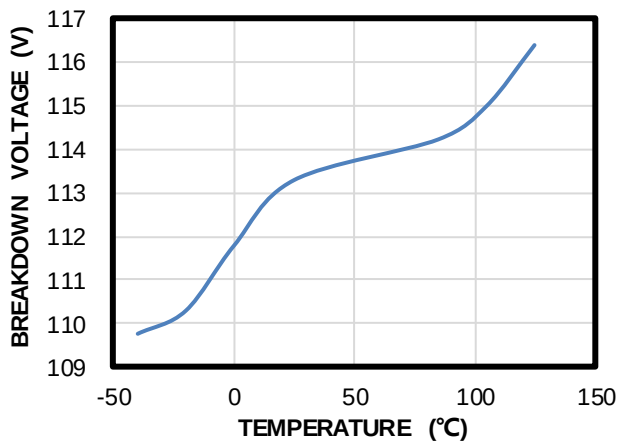
6) Guaranteed by characterization.

7) Guaranteed by design.

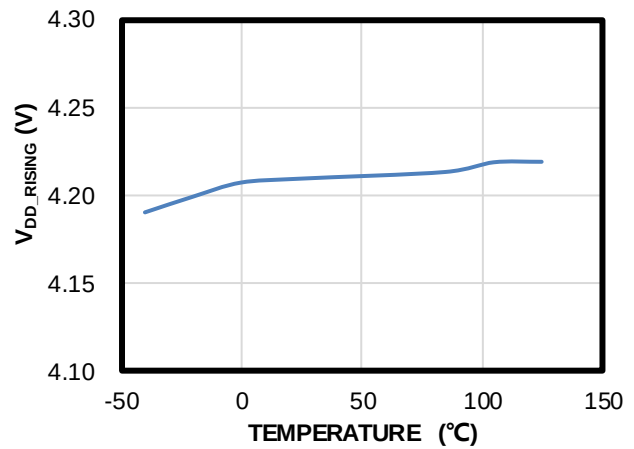
8) TJ = 25°C.

TYPICAL CHARACTERISTICS

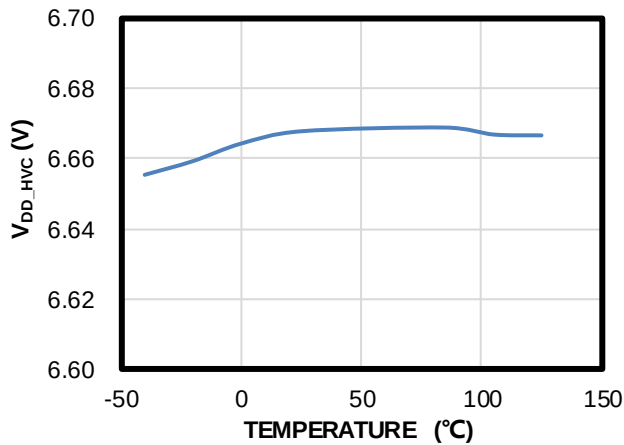
VD-VS Breakdown Voltage vs. Temperature



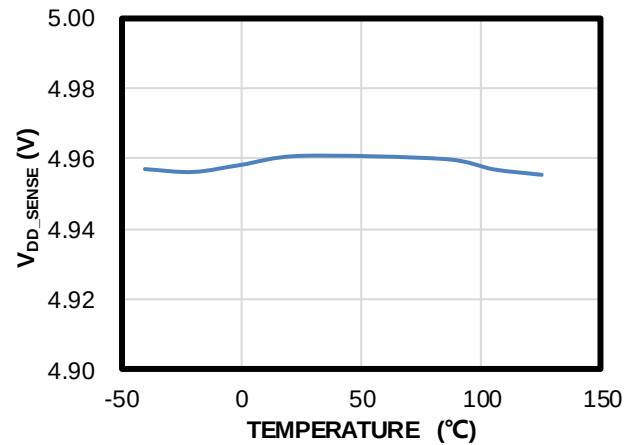
VDD Rising vs. Temperature



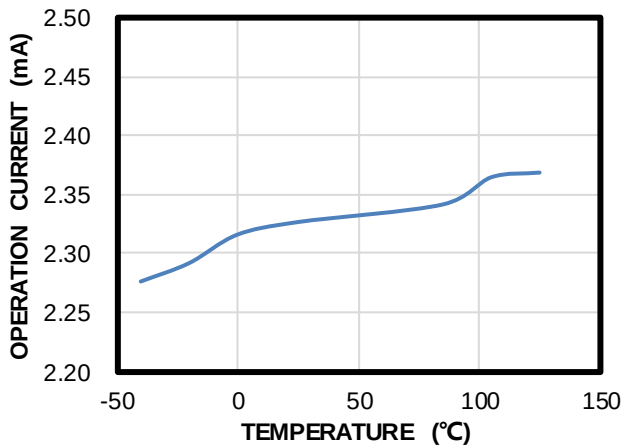
VDD Regulation Voltage vs. Temperature (HVC = 12V)



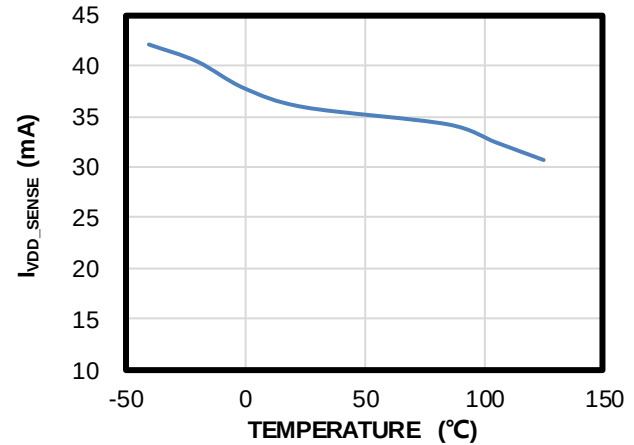
VDD Regulation Voltage vs. Temperature (SENSE = 30V)



Operation Current vs. Temperature (V_{DD} = 6.7V)

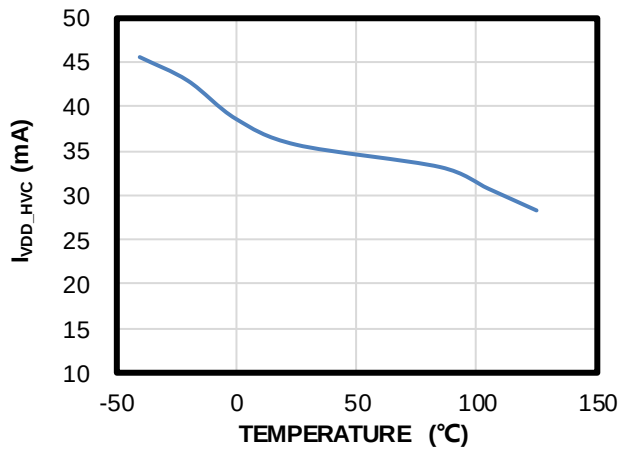


VDD Charging Current vs. Temperature (SENSE = 30V)

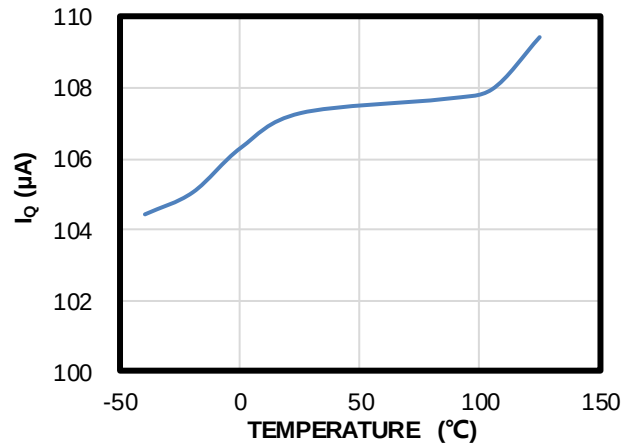


TYPICAL CHARACTERISTICS *(continued)*

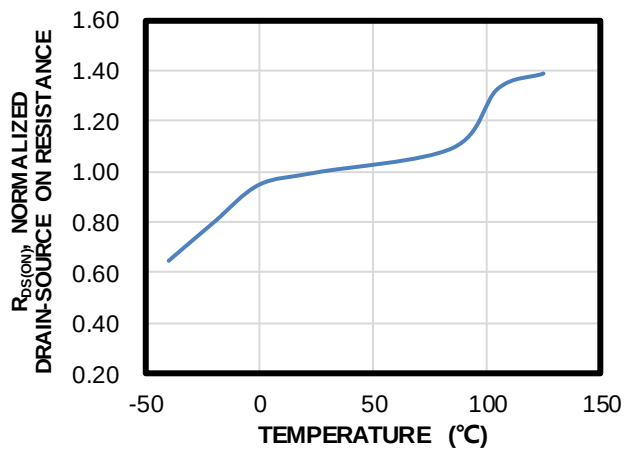
VDD Charging Current vs. Temperature (HVC = 12V)



Quiescent Current vs. Temperature ($V_{DD} = 7V$)



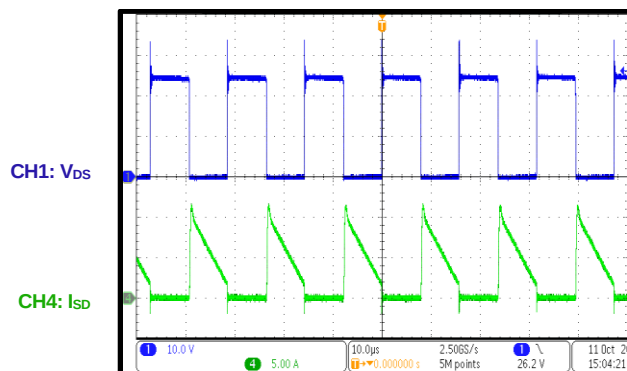
$R_{DS(ON)}$ vs. Temperature



TYPICAL PERFORMANCE CHARACTERISTICS

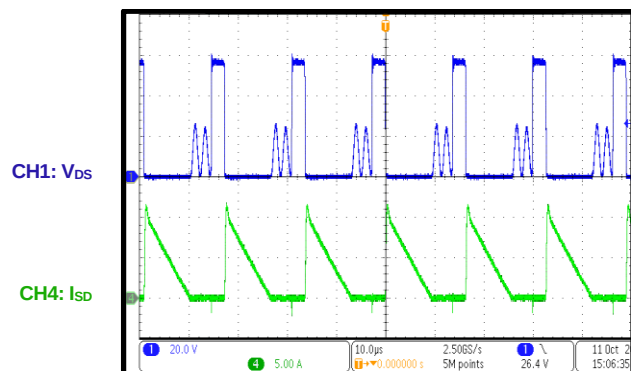
Operation in 30W Flyback Application

$V_{IN} = 90V_{AC}$, $I_{OUT} = 2.5A$



Operation in 30W Flyback Application

$V_{IN} = 265V_{AC}$, $I_{OUT} = 2.5A$



FUNCTIONAL BLOCK DIAGRAM

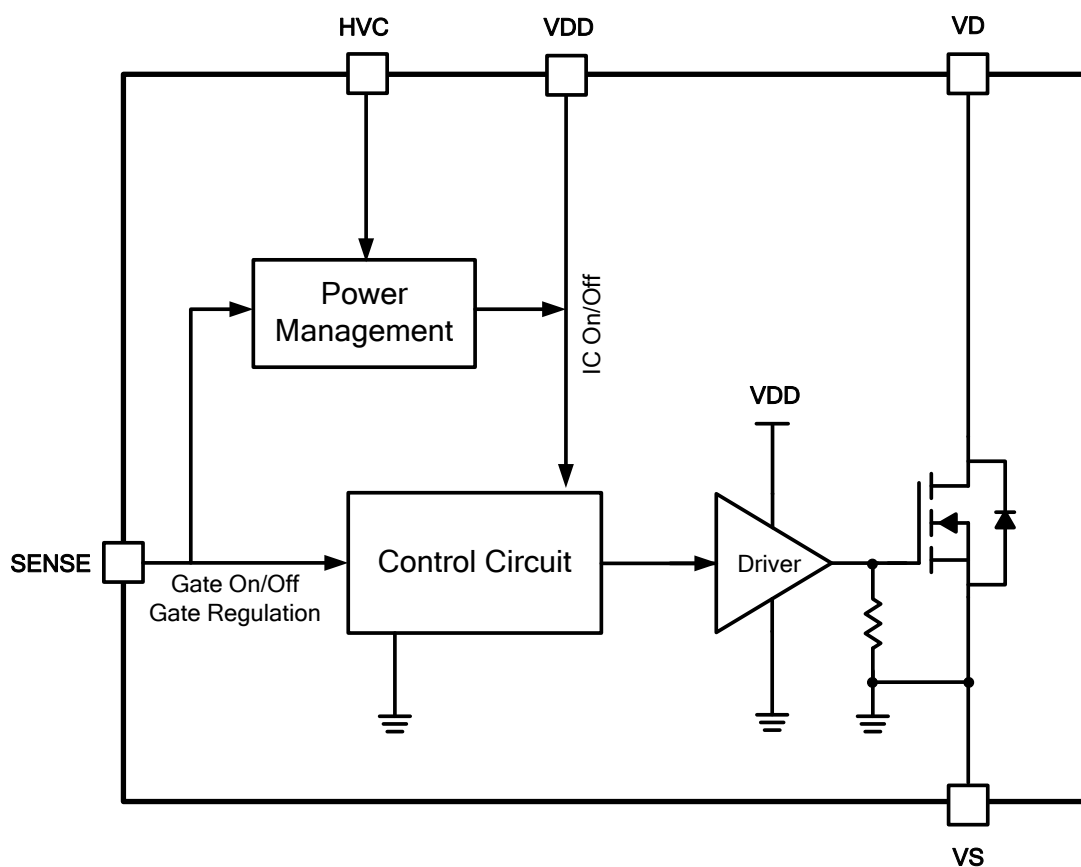


Figure 1: Functional Block Diagram

OPERATION

The MP6972 supports operation in discontinuous conduction mode (DCM) and continuous conduction mode (CCM), as well as for quasi-resonant (QR) flyback converters. The control circuitry controls the gate in forward mode and turns the gate off when the synchronous rectification (SR) MOSFET current drops to zero.

VDD Generation

The external capacitor at VDD supplies power to the IC. First, SENSE charges the capacitor via a current source with I_{VDD_SEN} . When $UVLO < V_{DD} < V_{DD_SENSE}$ (5V), both HVC and SENSE are allowed to charge VDD. When V_{DD} exceeds V_{DD_SENSE} , HVC charges VDD alone via a current source with I_{VDD_HVC} .

If $V_{HVC} < 5.7V$, VDD is regulated at V_{DD_SENSE} (5V). When $5.7V < V_{HVC} < 6.7V$, VDD is regulated at $V_{HVC} - 0.7V$ (internal current-dependent forward diode voltage drop). When $V_{HVC} > 6.7V$, VDD is clamped at V_{DD_HVC} (6.7V).

Start-Up and Under-Voltage Lockout (UVLO)

When V_{DD} exceeds the VDD UVLO rising threshold (4.2V), the MP6972 exits under-voltage lockout (UVLO) and is enabled. Once V_{DD} drops below 4.0V, the MP6972 enters sleep mode and V_{GS} is kept low.

Turn-On Phase

When V_{DS} drops to $\sim 2V$, a turn-on timer begins. If V_{DS} reaches the turn-on threshold ($-80mV$) from 2V within the turn-on slew rate detection time (30ns), the MOSFET turns on after a turn-on delay (t_{D_ON}), which is typically 20ns (see Figure 2). If V_{DS} crosses the turn-on threshold after the timer ends, the gate voltage remains off. This turn-on timer prevents the MP6972 from falsely turning on due to ringing in DCM or quasi-resonant operations.

Turn-On Blanking

The control circuitry contains a blanking function. When the MOSFET turns on, the control circuit ensures that the on state lasts for a specific period of time. The turn-on blanking time (t_{B_ON}) is $\sim 1.2\mu s$ to prevent an accidental turn-off due to ringing. However, if V_{DS} reaches 1.8V within the turn-on blanking time, then V_{GS} is pulled low immediately.

Conduction Phase

Once V_{DS} exceeds the forward voltage drop, which is $-V_{FWD}$ ($-40mV$), according to the decrease of the switching current, the MP6972 lowers the gate voltage level to enlarge the on resistance of the synchronous MOSFET.

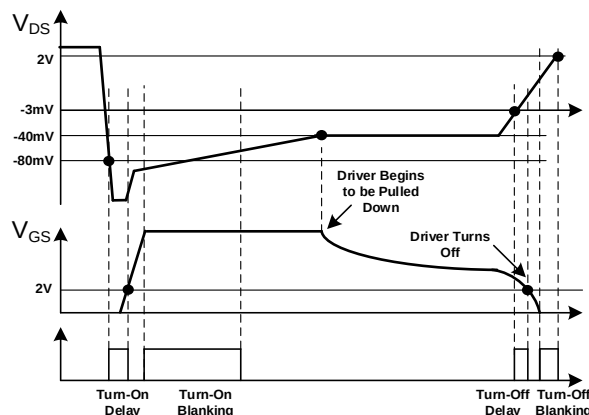


Figure 2: Turn-On/Turn-Off Timing Diagram

With this control scheme, V_{SD} is adjusted to be approximately equal to V_{FWD} even when the current through the MOSFET is fairly low. This function keeps the driver voltage at a very low level when the synchronous MOSFET is turned off, which boosts the turn-off speed and is especially important to CCM operation.

Turn-Off Phase

When V_{DS} rises to trigger the turn-off threshold ($-3mV$), the gate voltage is pulled to zero after a short turn-off delay (t_{D_OFF}), typically 25ns (see Figure 2).

Turn-Off Blanking

After the gate driver (V_{GS}) is pulled to zero by V_{DS} reaching the turn-off threshold ($-3mV$), a turn-off blanking time is applied, during which the gate driver signal is latched off. The turn-off blanking is removed when V_{DS} exceeds V_{B_OFF} (2V) (see Figure 2).

APPLICATION INFORMATION

Slew Rate Detection

During DCM operation, the demagnetizing ringing may bring V_{DS} below 0V. If V_{DS} reaches the turn-on threshold during the ringing, SR controllers without slew rate detection may turn on the MOSFET by mistake. This not only increases power loss, but may also lead to shoot-through if the primary-side MOSFET is turned on within the minimum on time of the SR controller.

The falling slew rate of the ringing is always much less than when the primary MOSFET is off; this false turn-on situation can be prevented by slew rate detection. When the slew rate is below the threshold, the IC does not turn on the gate even when V_{DS} reaches the turn-on threshold. For more details, see the Turn-On Phase section on page 9.

External Resistor on SENSE and HVC

Over-voltage (OV) conditions may lead to the device malfunctioning or even being damaged, so the application design must be careful to guarantee safe operation, especially on the high-voltage pin.

One common OV condition occurs when the body diode of the SR MOSFET is turned on, as the forward voltage drop may exceed the negative rating on the SENSE pin. In this case, it is recommended to place an external resistor between SENSE and the MOSFET drain. The resistance is typically recommended to be between 100Ω and 300Ω.

On the other hand, this resistor also cannot be too large, because it may slow down the V_{DS} detection slew rate. In general, it is not recommended to use a resistor greater than 300Ω, but this should be checked for each case based on the slew rate conditions.

In applications where the HVC may suffer from negative voltage bias (e.g. in the high-side set-up without auxiliary winding), there should also be a same resistor placed on the HVC externally.

Typical System Implementations

Figure 3 shows the typical system IC implementation in low-side rectification. The MP6972 is directly supplied by the output.

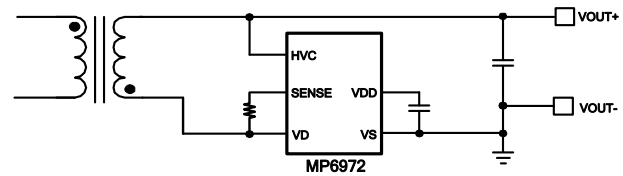


Figure 3: Low-Side Rectification

Maximum Output Current

The allowed temperature rise for the MP6972 limits the maximum output current the device can handle. The temperature rise is determined by the device's power loss. The MP6972's recommended rated output current for a typical universal input adapter is 2.5A. For certain designs, the power loss of the MP6972 can be calculated, so the maximum output current can be deduced.

The MP6972's power loss can be separated into several parts, including controller consumption and integrated MOSFET conduction loss. If the MP6972 works in continuous conduction mode (CCM), reverse-recovery loss of the integrated MOSFET must also be considered. Each part of the loss can be calculated based on Equation (1), Equation (2), and Equation (3), respectively:

$$P_{\text{LOSS_CONTROLLER}} = V_{\text{HVC}} \times I_{\text{DD}} \quad (1)$$

$$P_{\text{LOSS_SR_CONDUCTION}} = f_{\text{SW}} \times \int_0^{t_{\text{S_ON}}} V_{\text{SR_SD}}(t) \times I_{\text{SR_SD}}(t) dt \quad (2)$$

$$P_{\text{LOSS_SR_RR}} = \frac{1}{2} \times V_{\text{DS}} \times I_{\text{RR}} \times t_{\text{RR}} \times f_{\text{SW}} \quad (3)$$

Where I_{DD} is the MP6972's current, V_{HVC} is the voltage on HVC pin, $t_{\text{S_ON}}$ is the SR on period, $V_{\text{SR_SD}}$ is the voltage drop from the SR, $I_{\text{SR_SD}}$ is the current flowing from the SR, I_{RR} is the peak reverse current, and t_{RR} is the reverse-recovery time.

The MP6972's total loss (P_{LOSS}) is the sum of the above losses. If an RC snubber is used, the power loss caused by this snubber must also be taken into consideration.

The junction and case temperature rises can be calculated with the junction-to-ambient thermal resistance (θ_{JA}) and junction-to-case thermal

$$\Delta T_{1A} = P_{\text{LOSS}} \times \theta_{1A} \quad (4)$$

$$\Delta T_{JC} = P_{LOSS} \times \theta_{JC} \quad (5)$$

Design Example

Figure 4: Layout Example in Flyback Low-Side Application

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 4 and Figure 5, and follow the guidelines below:

1. Connect the SENSE pin to a different position for an adjustable turn-off time during the fast transients in CCM. The further the junction point is from VD, the earlier the SR turns off (see Figure 5).
2. Keep the IC out of the power loop to prevent the sensing loop and power loop from interrupting each other.

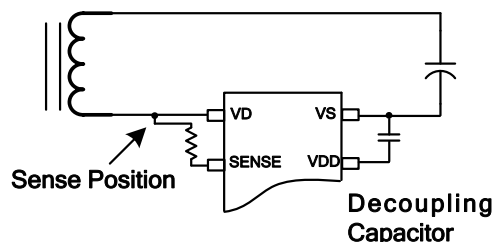
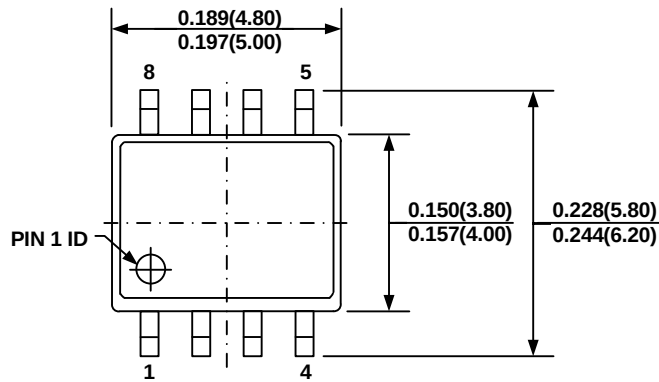


Figure 5: Voltage Sensing for VD/SENSE

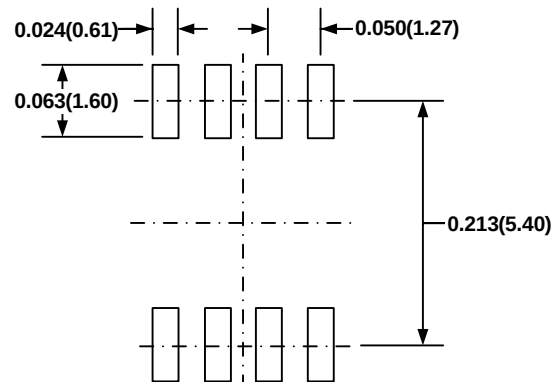
3. Place a decoupling ceramic capacitor between VDD and VS, close to the IC, for adequate filtering.

PACKAGE INFORMATION

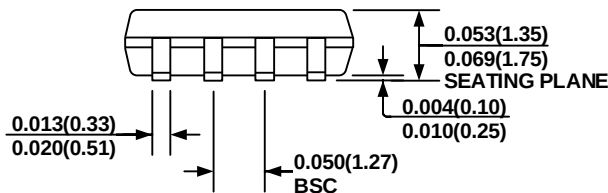
SOIC-8



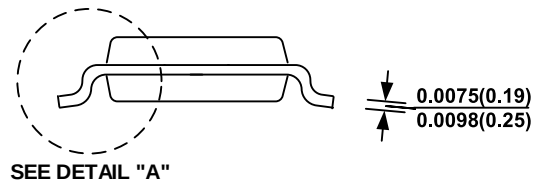
TOP VIEW



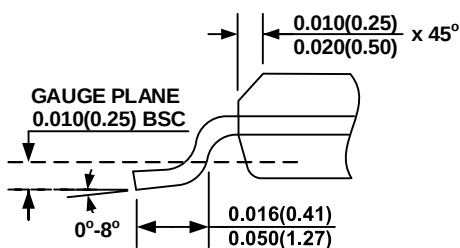
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW

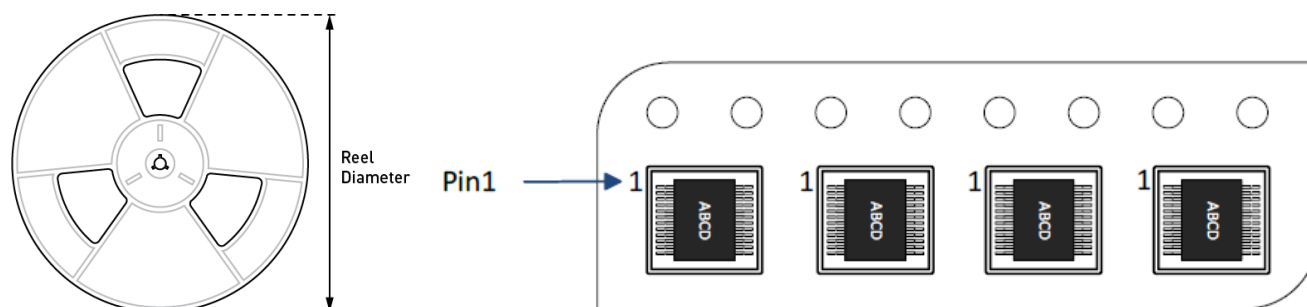


DETAIL "A"

NOTE:

- 1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- 5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
- 6) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6972GS-Z	SOIC-8	2500	100	N/A	13in	12mm	8mm

Revision History

Revision #	Revision Date	Description	Pages Updated
1.0	7/14/2020	Initial Release	-

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